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INSTRUCTION MANUAL

RADAR TIMING GENERATOR

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1.0 INTRODUCTION

This manual covers the theory and operation of the Radar Timing Generator (RTG) which replaces the Observatory's original radar timing system. The RTG (Fig 1.1) is a peripheral for the Radar Interface (RI), providing the timing pulses for the RI's A-to-D converters. Computer control of the RTG is provided through the RI (or through a spectral modem, the RS232 to RI232 Converter). The RTG's main functions are to generate "TXIPP" pulses to trigger the transmitter as well as "RDIPP" and "Gate Width" pulses to trigger the RI's analog-to-digital converters. It also provides a "Cal" pulse to activate a noise generator for on-line receiver calibration.

2.0 RELATED DOCUMENTATION

2.1 Radar Interface Instruction Manual (Manual No. 8609), Electronics Dept, Arecibo Observatory

2.2 Radar Multiplexer Instruction Manual (Manual No. 8611), Electronics Dept, Arecibo Observatory

2.3 Adage Interface Instruction Manual (Manual No. 8306), Electronics Dept, Arecibo Observatory. Describes the earlier data-taking interface.

2.4 RS-232 to RI-232 Converter Instruction Manual (Manual No. 8803), Electronics Dept., Arecibo Observatory

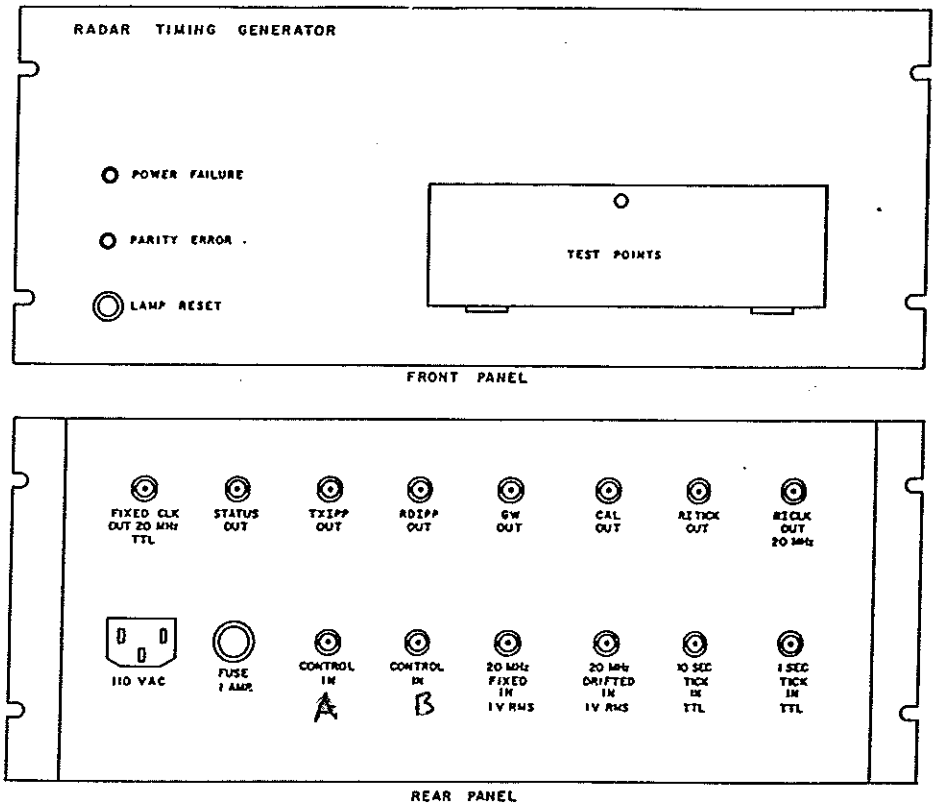

FIGURE 1.1 RADAR TIMING GENERATOR FRONT AND REAR PANEL VIEWS

3.0 GENERAL DESCRIPTION

The Radar Timing Generator (RTG) generates the following signals:

a. The Transmitter IPP (TXIPP): The transmitter's RF gate is triggered by the trailing edge of this 20 microsecond pulse, after the klystron beam current is fully on.

b. The Receiver Delayed IPP (RDIPP): Lags behind the TXIPP by a delay, "gate delay", normally programmed to be the roundtrip delay of radar echo. This Receiver Delayed IPP (leading edge) is the start pulse that enables the digitizers in the Radar Interface. For continuous sampling (as opposed to radar sampling) only a single RDIPP pulse is produced after a start request.

c. The Gate Width pulse: used to trigger the A-to-D converters in the Radar Interface. The GW period (intersample period) is programmable down to 0.1 usec. The GW pulse train is resynchronized to the leading edge of every RDIPP (and thus only at the start when in continuous mode).

d. The Calibration Pulse: a pulse used to gate on a receiver calibration source, usually a noise generator. The Cal pulse follows the RDIPP by a programmable delay and has a programmable length. In the continuous sampling mode only a single cal pulse is produced.

The TXIPP is derived from a fixed time base (the "20 MHz Fixed Clk" input), but for Doppler correction, the RDIPP, GW, and CAL can be driven from a separate "drifted" time base (the "20 MHz Drifted Clk" input). See figures 3.1 (timing diagram) and figure 3.2 (simplified block diagram).

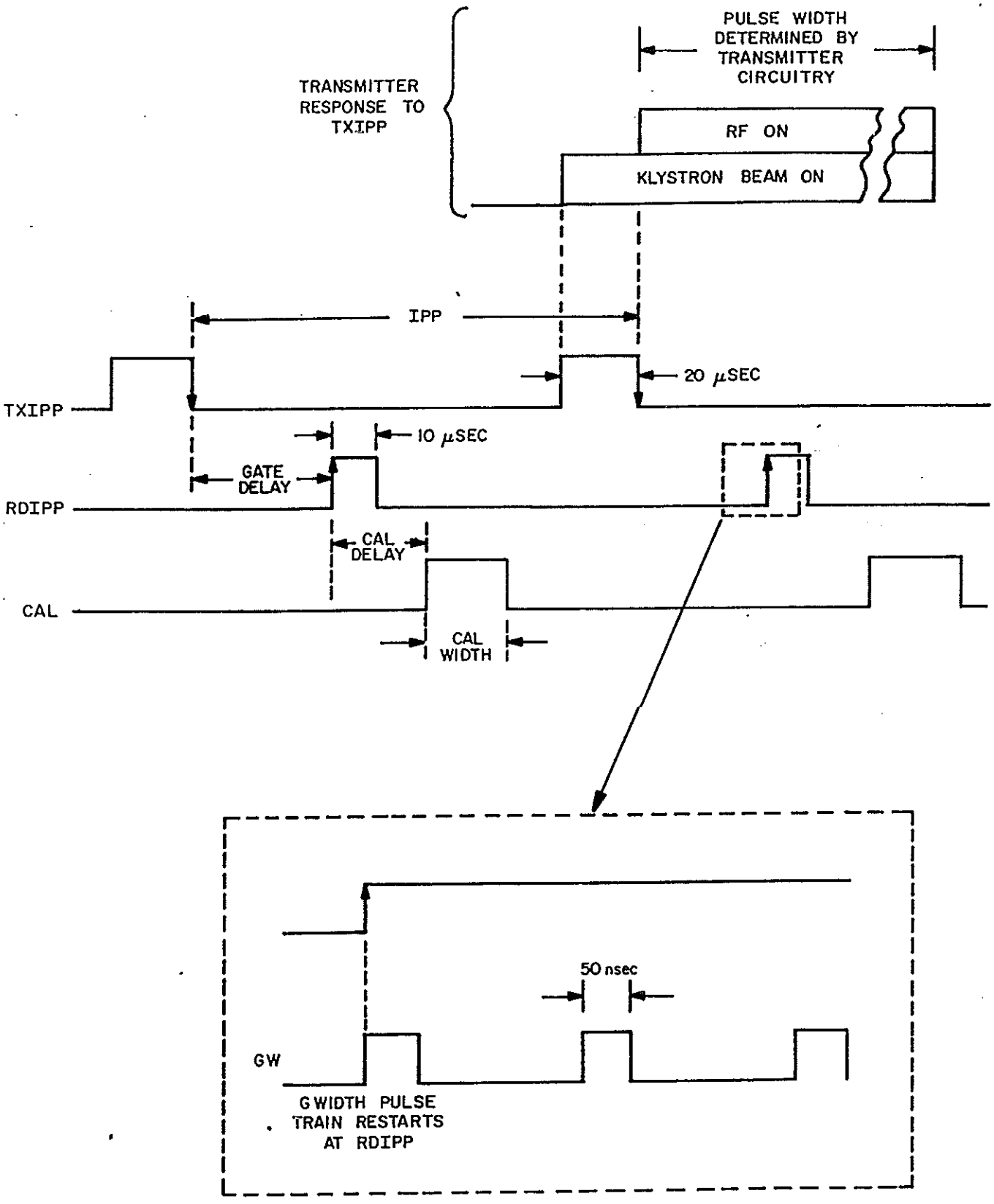

FIGURE 3.1 RADAR TIMING GENERATOR TIMING DIAGRAM (RADAR MODE)

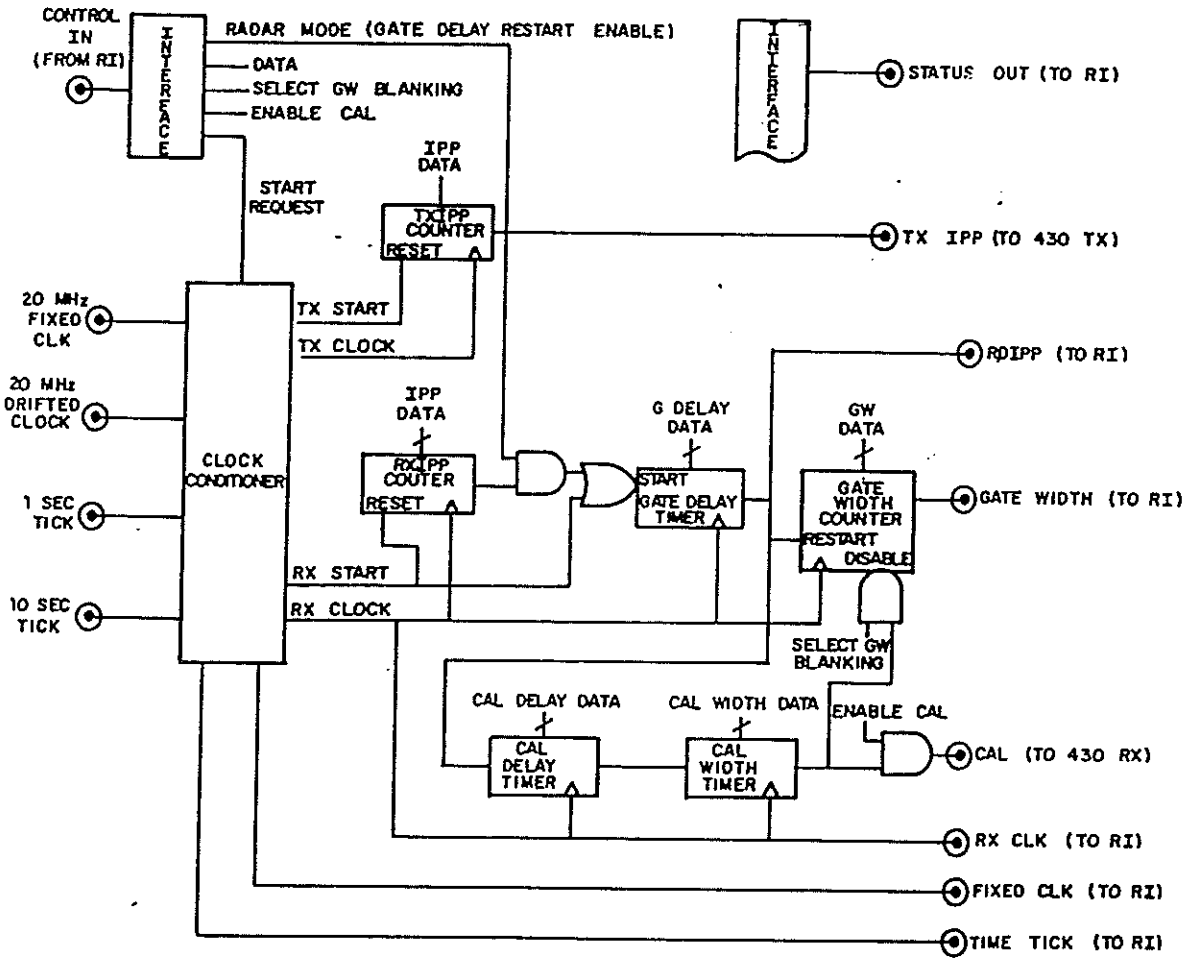

FIGURE 3.2 RADAR TIMING GENERATOR SIMPLIFIED BLOCK DIAGRAM

3.1 Gatewidth Blanking Mode

In this mode the cal circuit is used to blank the GW pulses. This enables the experiments to sample two windows, separated by what would normally have been the cal pulse. Meanwhile, the normal cal output jack can be disabled.

4.0 SOFTWARE REQUIREMENTS

The RTG operates only under computer control, by way of the Radar Interface or the RS-232 to RI-232 Converter (see fig. 4.1). There are no front (or rear) panel controls other than a push button switch to reset the indicator lamps for parity error and power failure. The corresponding status bits are latched separately and are cleared only by the computer.

To use the RTG, one first loads it with 10 consecutive data words (see table 4.1). The RTG is normally connected to Serial Port 01 of the RI, so words destined for the RTG are sent to the RI after selecting its Serial Port 01.

Once the timing data have been loaded, a command word (see fig 4.2) must be sent to enter the data, to select the mode(s), and to start the RTG. (This first command word actually completes the loading but further command words do not disturb the data).

4.1 Data Words

Table 4.1 shows the data word format. Each of the five timing parameter requires a word for its sixteen LSB's and another word for its sixteen MSB's. In all cases the units are tenths of microseconds.

4.2 Command Word

Table 4.2 shows the command word fields. The use of the data verification request is discussed in 7.1.

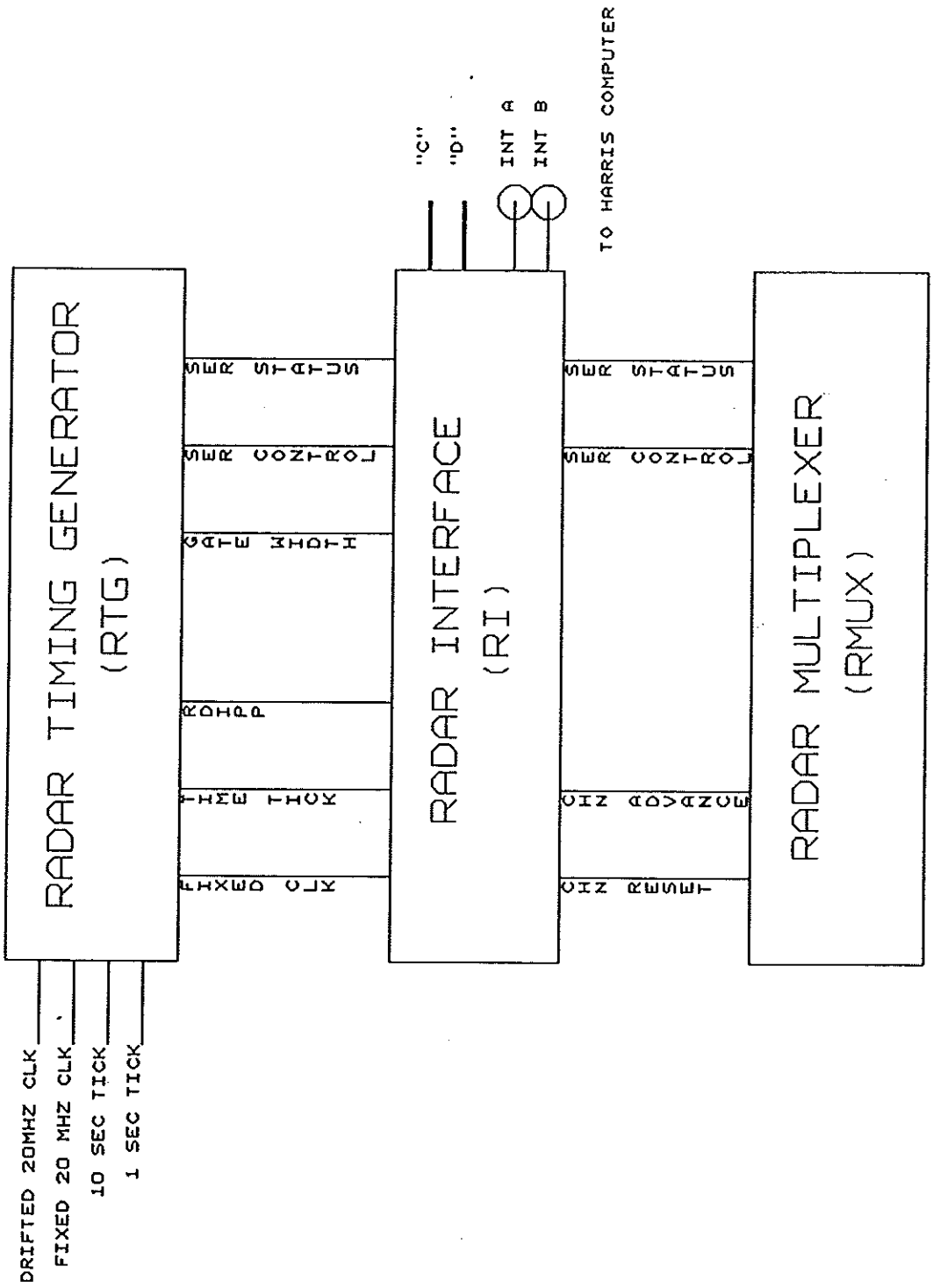

FIGURE 4.1 INTERCONNECTIONS BETWEEN THE RI, RTG, & RMUX

TABLE 4.1 DATA WORD FORMATS (RI to RTG)

Data Word	Bit 23	Bits 22-16	Bits 15-0
1st	0	x	IPP 16 LSB's
2nd	0	x	IPP 16 MSB's
3rd	0	x	GDELAY 16 LSB's
4th	0	x	GDELAY 16 MSB's
5th	0	x	GWIDTH 16 LSB's
6th	0	x	GWIDTH 16 MSB's
7th	0	x	CALDELAY 16 LSB's
8th	0	x	CALDELAY 16 MSB's
9th	0	x	CALWIDTH 16 LSB's
10th	0	x	CALWIDTH 16 MSB's

TABLE 4.2 COMMAND WORD FORMAT RTG)

Bit(s)	Description
23	Set to 1 to indicate Command Word
19	0: NOP 1: Update unit with new timing data
15,14	0: NOP 1: Select Radar Sampling Mode 2,3: Select Continuous Sampling Mode
13,12	0: NOP 1: Select drifted clock for receiver timing (RXCLK) 2,3: Select fixed clock for receiver timing (RXCLK)
11,10	0: NOP 1: Enable Cal output 2,3: Disable Cal output
9,8	0: NOP 1: Select one second tick 2,3: Select ten second tick
7,6	0: NOP 1: Select gatewidth blanking mode 2,3: Select normal gatewidth mode
5	0: NOP 1: Clear power failure error flags
4	0: NOP 1: Clear error flags
3,2	0: NOP 1: Arm for automatic start at next tick 2,3: Start immediately
1,0	0: NOP 1: Request Status 2,3: Verification Request

4.3 Status Word

Table 4.3 shows the status bits. If the power failure flag (bit 23) is HI the generator has lost its data and it must be reloaded and restarted. Note: If the failure error flag will not reset, the lithium battery needs to be changed. The parity error flag indicates defective transmission of data from the RI to the RTG. The mismatch error flags (bits 15-19) are discussed in 7.4. All error flags can be reset via the command word.

4.3.1 Status Request

To request status from the RTG requires the following procedure:

1. Send a command word to the RI to (a) Select port 01 (the RTG) and to (b) clear the serial data flag.
2. Send the RTG status request command as data to the RI.
3. Read the RTG status word from the RI.

4.3.2 Data Verification Request

The procedure of the data verification request is the same as for status request - see section 7.1.

TABLE 4.3 STATUS WORD FORMAT (RTG TO RI)

Bit(s)	Description
0	20 MHz Fixed CLK not present at rear panel
1	20 MHz Drifted CLK not present at rear panel
2	10 Sec tick not present at rear panel
3	1 Sec tick not present at rear panel
4	Drifted (not fixed) Rcvr time base selected
5	1 Sec (not 10 sec) time tick selected
6	Radar Sampling Mode (not continuous) selected
7	Gatewidth Blanking mode selected
8	Parity error flag (defective data rcvd from RI)
9	TXIPP output is dead
10	RDIPP output is dead
11	Gatewidth output is dead
12	Cal output is dead
13	RICLK output is dead
14	TICK output is dead
15	Q1RXIPP v.s. Q1TXIPP mismatch error flag*
16	Q1RXIPP v.s. Q1GDELAY mismatch error flag*
17	Q1RXIPP v.s. Q1GWIDTH mismatch error flag*
18	Q1RXIPP v.s. Q1CALDELAY mismatch error flag*
19	Q1RXIPP v.s. Q1CALWIDTH mismatch error flag*
20	always low (spare)
21	Cal output enabled
22	Power supply voltage error flag (over/under voltage)
23	Power failure error flag (indicates timing data has been lost)

*indicates error only when running timing tests (see section 7.4).

5.0 SPECIFICATIONS

5.1 Programmability

Function	Lower Limit	Upper Limit	Resolution
IPP	100 usec	429 sec	0.1 usec
Gate Delay	0.2 usec	IPP	0.1 usec
Gate Width	0.1 usec	IPP	0.1 usec
Cal Delay	0.1 usec	IPP	0.1 usec
Cal Width	0.1 usec	IPP	0.1 usec

Note: TXIPP is derived from the 20 MHz fixed clock input. The other functions, RDIPP thru Cal width, are derived either all from the 20 MHz variable (drifted) clock input or all from the 20 MHz fixed clock.

5.2 Output Levels: TTL, capable of driving 50 ohm loads (SN74S140 Drivers).

5.3 Clock Inputs: 50 ohm internal termination ac coupled. 1V RMS Sinewave, ac coupled with internal 50 ohm termination.

5.4 Time Tick Inputs: TTL, ac coupled, 50 ohm internal termination.

5.5 Control Input: TTL, differential input, 50 ohm internal termination.

5.6 Status Output: TTL, capable of driving 50 ohm load (SN74S140 driver).

5.7 Power requirement: 25 watts.

6.0 THEORY OF OPERATION

Figure 6.1 is a detailed block diagram of the RTG. The five interior modules clocked by RXCLK form a synchronous state machine. When the fixed clock option is selected (via the command word), RXCLK is identical to TXCLK and all six modules run synchronously.

Basic operation is illustrated by Figure 6.2, a simplified schematic diagram of the receiver timing section. The IPP counter fires the Delay Timer which, in turn, fires the Cal Delay timer/ Cal Width Timer. The gate width counter is restarted after every gate delay. (Although the GW never stops, the term "restart" is used here instead of "resync" in order to avoid confusion with the synchronous logic design philosophy used throughout the RTG).

Note that when the fixed clock is selected, the RXIPP counter is not used; the gate delay/gate width/cal modules are switched over to be triggered by the TXIPP counter. This is done merely as a precaution; by using a single IPP counter there is no possibility of losing synchronization between the transmitter and receiver. Had both counters been used, as in drifted operation, some unforeseen glitch may have disturbed one counter with respect to the other, and the user would feel compelled to monitor the phase, an unnecessary inconvenience.

The timing modules are fully synchronous, both individually and collectively. Within this group of modules, the only asynchronous signals are GW RESTART ENABLE and SELECT FIXED CLK and these are static, i.e. mode control lines. Figure 6.2 is a simplified schematic diagram of the timing modules with pulses identified by name.

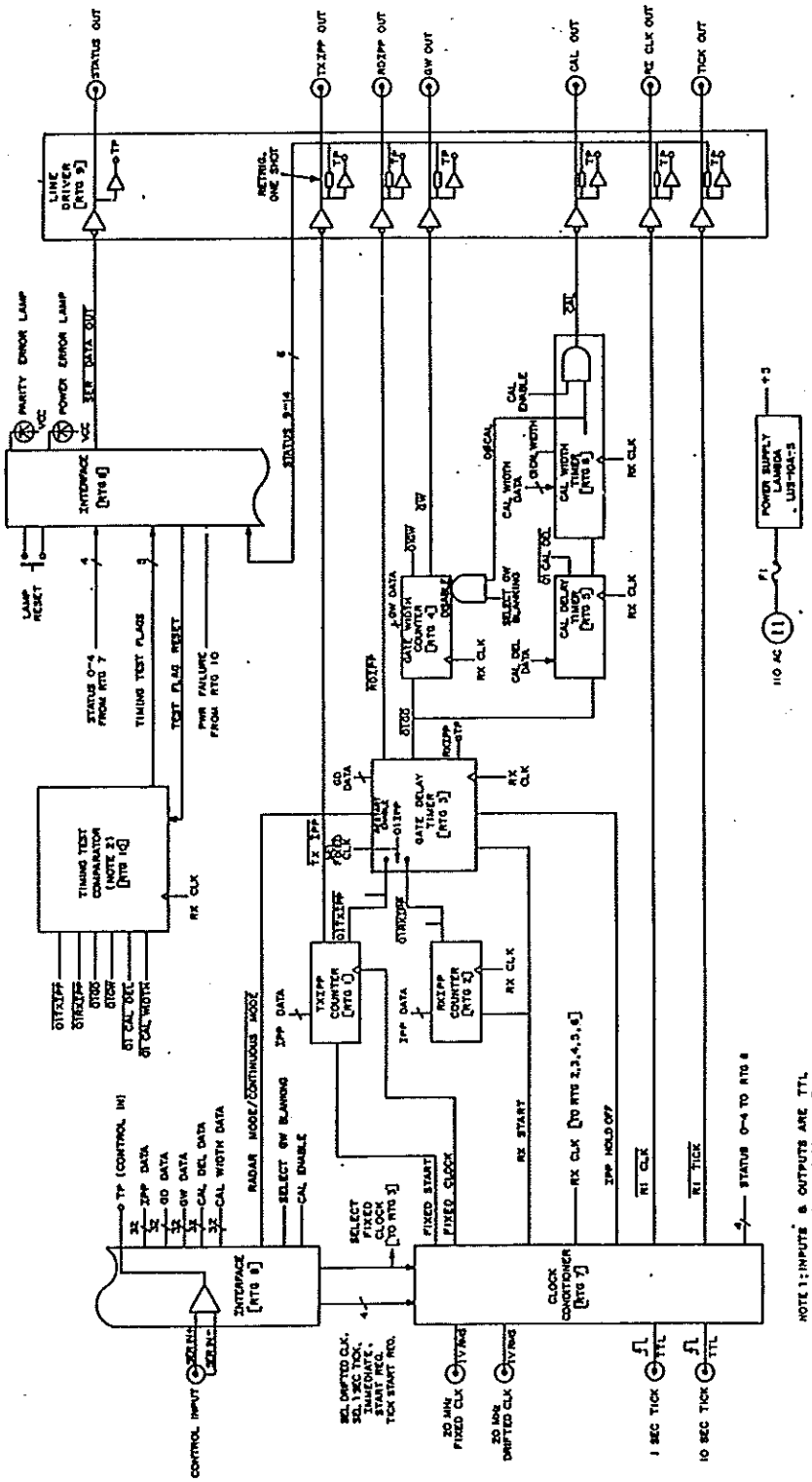

FIGURE 6.1 RADAR TIMING GENERATOR DETAILED BLOCK DIAGRAM

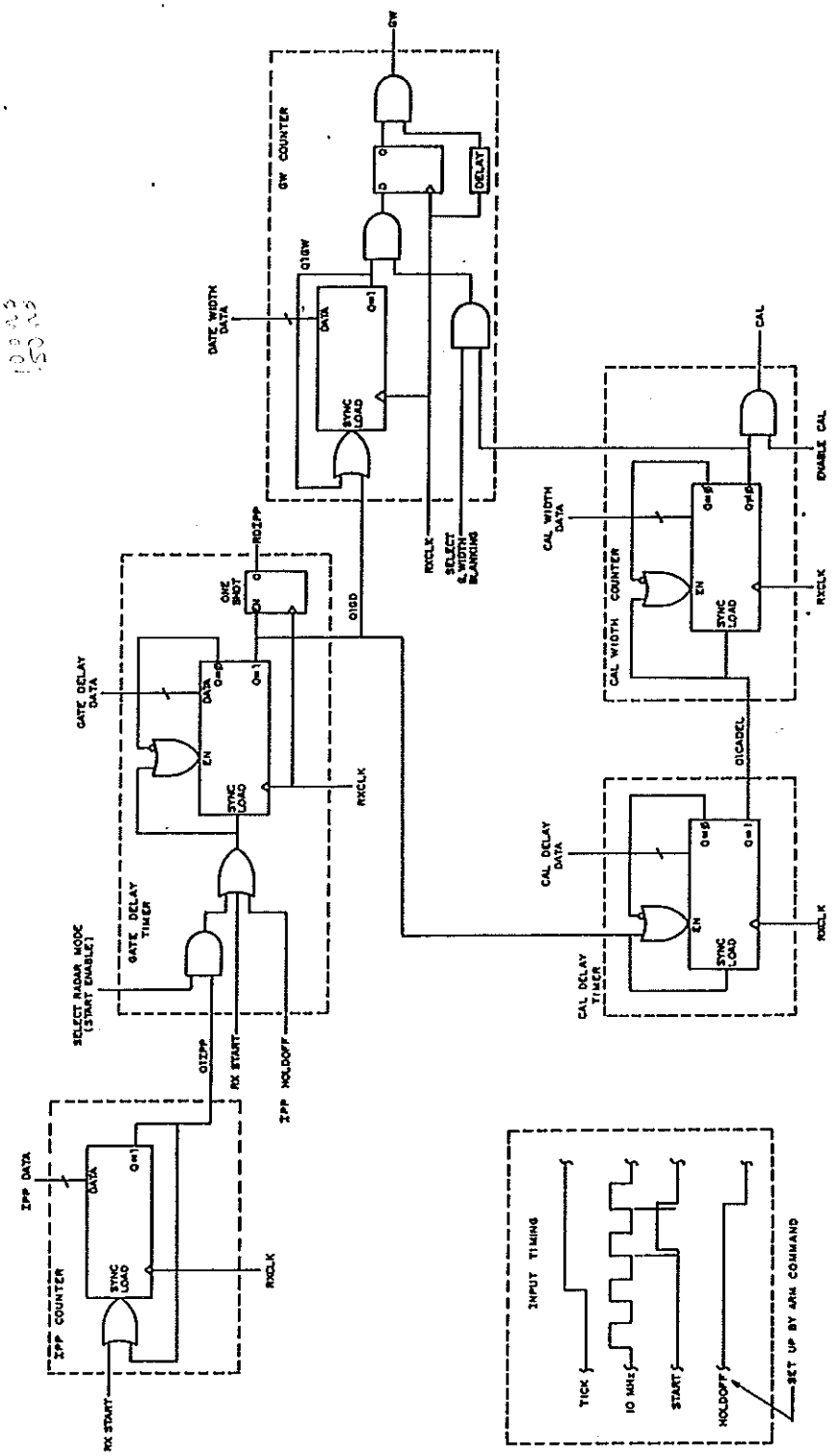

FIGURE 6.2 SIMPLIFIED SCHEMATIC DIAGRAM OF TIMING SECTION

6.1 TXIPP Counter

This synchronous logic circuit (see Fig 6.1) is clocked by the fixed 20 MHz clock. It has one external input, FIXED START (which is also synchronous). The counter will decrement at every clock pulse unless FIXED START is HI.OR.Q=1 (Q = present count). In these cases it loads its data input (IPP in tenths of microseconds). The output Q1TXIPP, is HI if and only if the count, Q, is one. The output TXIPP goes HI at Q = 200 and goes LO again at Q = 0 to produce a 20 microsecond pulse. This pulse gets the transmitter's klystron beam turned on. The trailing edge of the pulse triggers the transmitter's r.f. drive. Note that while this IPP counter nominally generates the TXIPP, it is also used for receiver timing when the Fixed Clock option is selected. (In this case the RXIPP counter is unused).

6.2 RXIPP Counter

This module is identical to the TXIPP counter except that it is clocked by RXCLK which is programmable to be either fixed or drifted. Its only output, Q1RXIPP, is HI when Q = 1. Like the TXIPP counter, this counter counts down except when RXSTART =1.OR. Q = 1. In these cases it loads the IPP Data (IPP length in tenths of microseconds). Note that the RXIPP counter is only used when the drifted clock is selected. When the fixed clock is selected, the receiver timing uses the TXIPP counter. Meanwhile, however, the unused RXIPP counter is being clocked with the fixed clock so that it can be checked against the TXIPP counter (see sec. 7, Testing and Troubleshooting).

6.3 Gate Delay Timer Module

This module (see figure 6.2) is also totally synchronous; the rising edge of the clock causes it to assume a state defined by its inputs and its present state, Q.

The circuit counts down except when RXSTART .OR. Q1IPP .OR. BLANK = 1. In these cases it loads the data (gate delay in tenths of microseconds). Once the counter has reached 0, it stays at 0, waiting for Q1IPP to go HI.

The output Q1GD is used to restart (resynchronize) the gate width counter and to fire the cal. If the GW RESTART ENABLE input is HI, Q1GD goes HI once every IPP. Otherwise, Q1GD (and RDIPP) fire only once after a START pulse.

The RDIPP output is derived from a 100-microsecond one-shot, fired when the clock encounters Q1GD = 1.

The purpose of the IPP holdoff input is to turn off the RDIPP in the interval between a Start Request from the computer and the subsequent first RDIPP. The first data read by the computer will then correspond to the time of the first RDIPP.

6.4 GW Counter

This module (see Fig 6.1) is another synchronous counter. It counts down except when Q1GD.OR.Q1GW = 1. In this case it loads the GW Data. The GW output is HI for the first half of every clock cycle that encounters Q1GW=1.

6.5 Cal Delay Timer

This module, another synchronous down-counter, is shown in Figure 6.2. It counts down except when Q1GD = 1. In that case it loads the data (cal delay in tens of microseconds). When it reaches 0 it stops. The line Q1CALDEL = 1 when the count is 1.

6.6 Cal Width Timer

This synchronous circuit (see Fig. 6.2) is almost identical to the Cal Delay Timer. It loads its data (cal width in tens of microseconds) when the clock encounters Q1CALDEL = 1. It then counts down to zero and stops. The Cal output is HI whenever this timer is not zero.

6.7 Clock Conditioner Module

This module (see figure 6.3) contains the input buffer for the two clock signals and the two time tick signals. Each input is provided with a retriggerable one-shot to provide clock status. A sync circuit is provided for each clock. These circuits divide the 20 MHz clock by two to provide the synchronized 10 MHz clocks. They also provide the start and blanking signals whose timing is shown in figure 6.4.

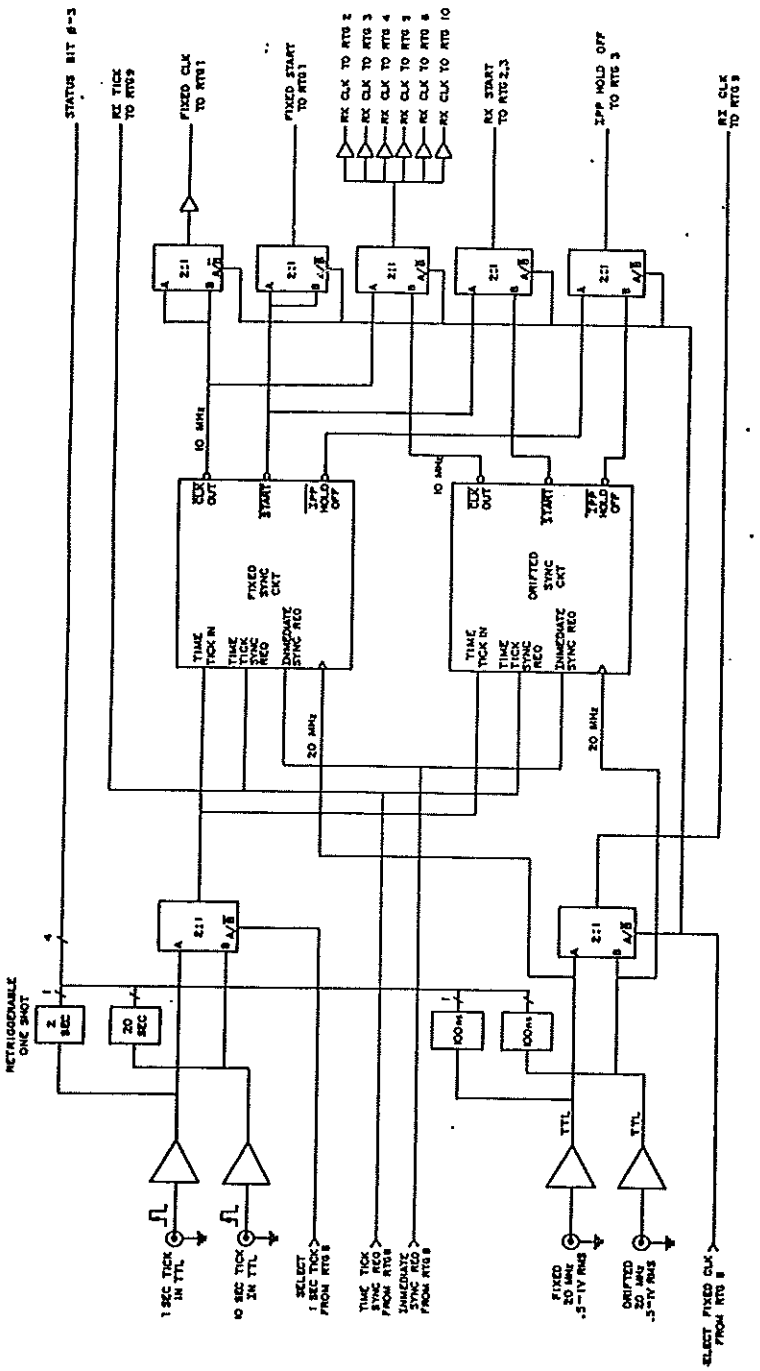

FIGURE 6.3 CLOCK CONDITIONER BLOCK DIAGRAM

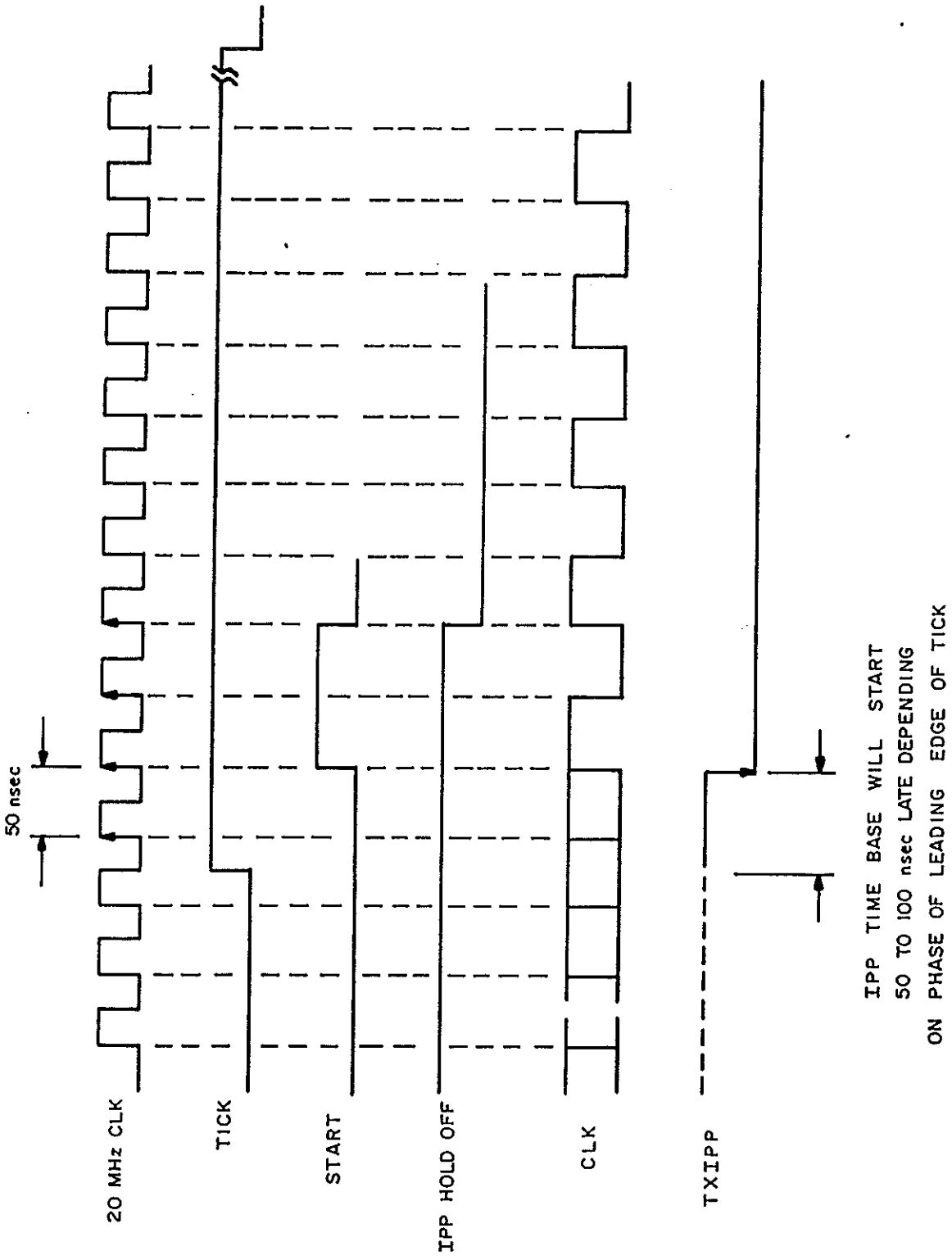

FIGURE 6.4 SYNC CIRCUIT TIMING DIAGRAM

6.8 Interface Module

Refer to figure 6.1 for the relationship of the interface module to the other modules. Figure 6.5 is a more detailed block diagram of the interface. At the input side is a serial decoder which separates data and clock pulses and also provides a strobe to indicate that an input word has arrived. If the input word has bit 23 HI, it is a command word and the command decoder/latch will be strobed. Every new input word causes the present contents (16 LSBs only) of the input latch to be shifted into the data register. This 160-bit register is filled with the 10-word data block. An update command transfers the 160 bits from the data register to the data latches which control the counter and timer cycle lengths.

A command word which requests status will produce a status strobe which loads the status shift register and then triggers the serial transmitter.

6.9 Line Driver Module

This module provides 74S140 drivers for the rear panel outputs, LSTTL drivers for the front panel test points, and retriggerable one-shots to provide output pulse status, i.e, that the outputs are not dead.

6.10 Timing Test Comparator Module

This module contains five exor gates and latches to compare the Q=1 output of the RXIPP counter to the Q=1 output of the other five timing modules (see section 7.4).

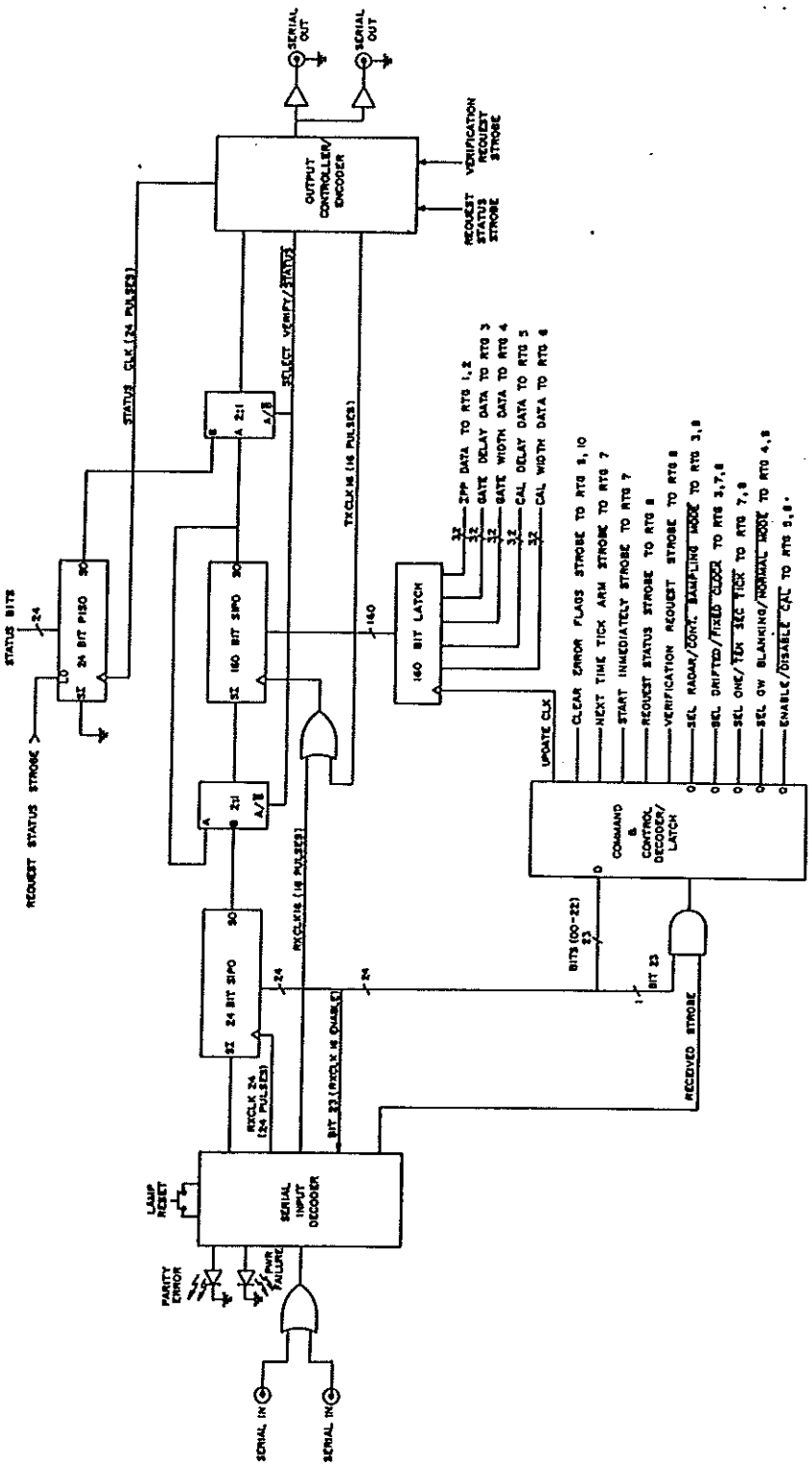

FIGURE 6.5 INTERFACE BLOCK DIAGRAM

7.0 TESTING

The RTG has enough built-in test capability to verify correct operation without external instruments. This makes maintenance checking a simple matter of running a test program. Likewise, data-taking programs can include an initial call to a test program to insure that the unit is energized, that it has the necessary clock signals, that it is producing output signals, and that the output signals are correct. The tests are outlined below in 7.1 through 7.4.

7.1 Communication Test

1. Send a Command Word to clear the parity error flag.
2. Send the 10 data words to the RTG (any data).
3. Send a Command Word requesting data verification. Read returned word from the Radar Interface and store. Repeat this step nine more times.
4. Check that the stored words correspond to the 10 data words (see Table 7.1).
5. Request Status and check that the parity error flag is LO.
6. Repeat steps 3 and 4 to verify that the data is still in place.
   Important: Ten (or a multiple of ten) verification requests must be sent or the data will be left misplaced in the RTG's internal registers.

7.2 Input Tests

1. Clear the error flags.
2. Request status and verify that the clocks and time ticks are present at the rear panel and that the power supply error flag is LO.

7.3 Output Tests

1. Load the generator and start.
2. Use status bits 9-14 to verify that the output signals are active.

7.4 Timing Test

1. Load the generator with identical values for each parameter, i.e. IPP = GATEDELAY = GATEWIDTH = CALDELAY = CALWIDTH.
2. Select fixed clock and start the generator.
3. Wait at least one IPP and then clear the error flags.
4. Verify that status bits 15 through 19 remain low.

This test forces the 6 counters in the RTG to run exactly in step. The associated error flags in the status word are set whenever the Q=1 output of the RXIPP counter disagrees with the Q=1 output of the other counters.

8. SCHEMATIC DRAWINGS

This section includes block diagrams, all detailed schematics, mechanical drawings and PAL chips specifications for the Radar Timing Generator.

A) General Block Diagram
B) Front and Rear Panels
C) Output Timing Diagram
D) Counters/Timers Block Diagram
E) Detailed Block Diagrams
    - RTG1 TXIPP Counter
    - RTG2 RXIPP Counter
    - RTG3 Gate Delay Timer
    - RTG4 Gate Width Timer
    - RTG5 Cal Delay Timer
    - RTG6 Cal Width Timer
    - RTG7 Clock Conditioner
    - RTG8 Interface
F) RTG Detailed Schematic (16 pages)
G) PAL Chips Specs, schematics, PALASM source code (28 pages)
H) Power Supply specs