515K

Manual No.9401

VME Radar Interface

Instruction Manual

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1.0 INTRODUCTION

This manual describes the VME Radar Interface (VME RI), a peripheral of the VME data taking computer. The VME RI replaces the original Radar Interface, a peripheral of the Harris computer. The VME RI was built in order to take advantage of the faster data transfer rates possible with a VME computer. The VME RI has four 12-bit, 10 MHz sampling, analog-to-digital converters for on-line data taking. It is also the controller for the VME Radar Multiplexer (VME RMUX), a separate unit that contains two 8-channel analog multiplexers.

2.0 RELATED DOCUMENTATION

2.1 Radar Interface Instruction Manual (Manual No. 8609), Arecibo Observatory, Electronics Department, 1991.

2.2 Radar Timing Generator Instruction Manual (Manual No. 8610), Arecibo Observatory, Electronics Department, 1986.

2.3 Radar Multiplexer Instruction Manual (Manual No. 8611) Arecibo Observatory, Electronics Department, 1991

2.4 PME VP-1 Manual, Rev. 1, Issue 2, Radstone Technology

2.5 VIC068A,VAC068A User's Guide, Cypress Semiconductor, 1992

2.6 The VMEbus Handbook, by Wade Peterson, VFEA International Trade Association

2.7 VME Radar Multiplexer Instruction Manual (Manual No.) Arecibo Observatory, Electronics Department, 1994

2.8 VME 5 MBaud Serial Ports Instruction Manual (Manual No.) Arecibo Observatory, Electronics Dept., 1994

2.9 VME SPS Instruction Manual (Manual No.) Arecibo Observatory, Electronics Department, 1994

3.0 GENERAL DESCRIPTION

3.1 Function

The VME RI is an analog data acquisition device containing four 12-bit, 10 MHz sampling, analog-to-digital converters, triggered in parallel. Each of these A-to-D converters is followed by a 16-bit Packer and a 16-bit FIFO (First-In-First-Out) buffer memory. The FIFOs permit taking data continuously at the maximum input rate of the computer. They also permit burst sampling at rates up to 10 MHz.

Each A-to-D converter normally produces a 12-bit word, sign-extended to 16 bits. Thus, each pair of digitizers, I & Q, produces a 32-bit word, the data word size on the VMEbus. Optionally, one can use only the eight MSBs of a digitizer to fill a 16-bit word every two conversions, or the four MSBs to fill a word every four conversions, etc. In total, there are 5 packing options, 16,8,4,2,1 bits/conversion. This allows faster conversion rates for continuous sampling and, for burst sampling, effectively lengthens the FIFOs.

The VME RI also provides eight bits to select the channel of an external multiplexer (256 possible channels). The channel number sequence is programmable upto a depth of 8K. Three of these bits are binary encoded and are used in the VME RMUX.

Figure 3.1 is a block diagram of the VME RI. The module designations, RI1-RI8, will be used in the following sections to denote the various functional blocks.

3.2 Physical Description

The VME RI consists of two physically separate parts. A chassis contains the A-to-D Converters (RI1), the 16-Bit Packers (RI2), the Sample Pulse Generator (RI4), and the Channel Sequence Memory(RI4), etc. The other part, as shown in the block diagram, is located in the Data-Taking VME Crate. It consists of the FIFOs and the controller that interfaces to the VMEbus (RI8).

Figure 3.2 shows the front and rear panel views of the chassis. The front panel has a door, which on opening, presents 16 BNC's that can be used as test points. All of the signals can drive 50Ω. Figure 3.2.2 shows the relationship between the VME RI, the VME RMUX, the Radar Timing Generator (RTG), and the VME 5MBaud Serial Ports (VME SBP). The VME SBP is located in the Data-Taking VME Crate.

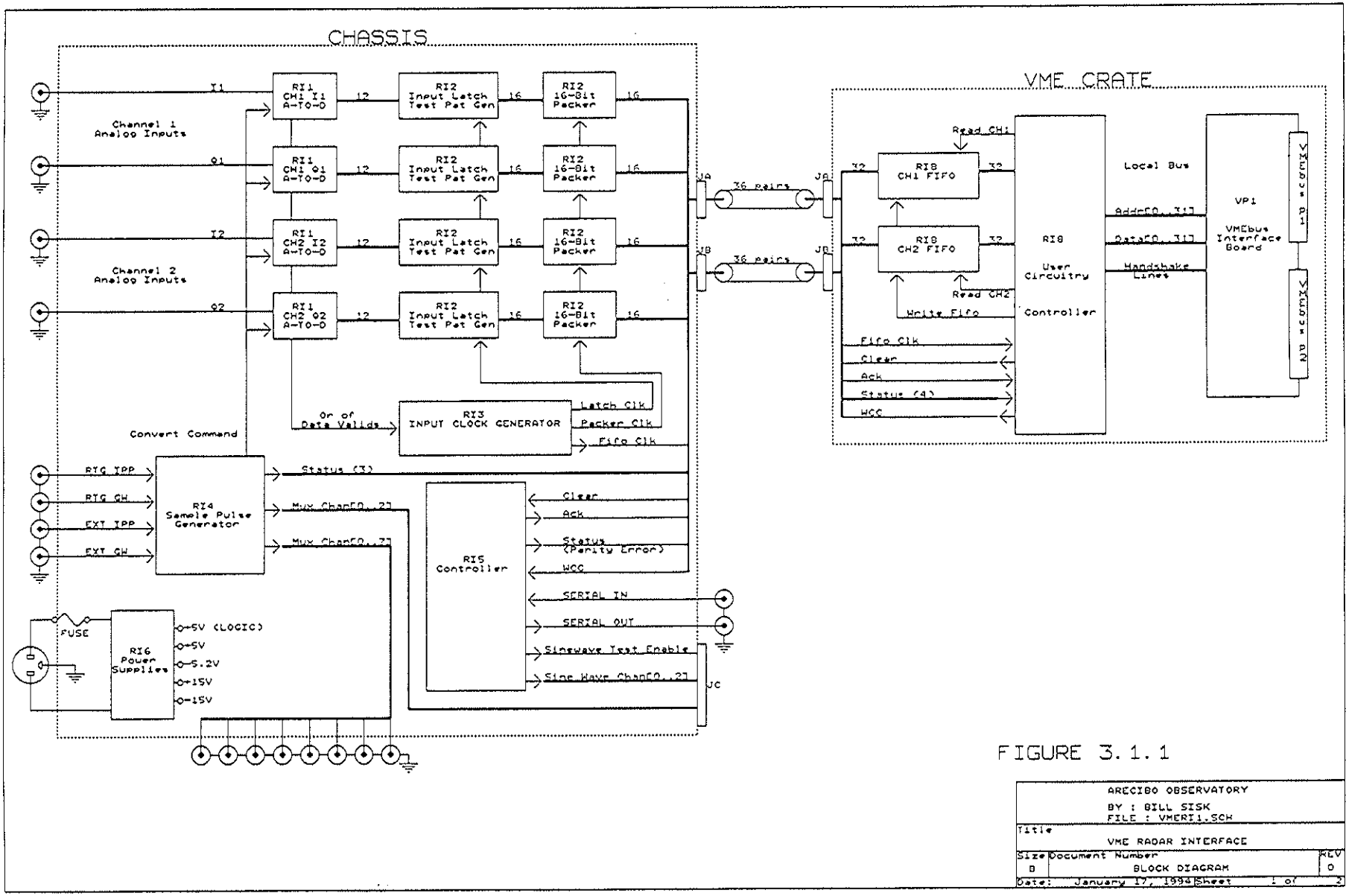


FIGURE 3.1.1

ARECIBO OBSERVATORY BY : BILL SISK FILE : VMERI1.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: BLOCK DIAGRAM	REV: 0
Date: January 17, 1994	Sheet 1 of 2	

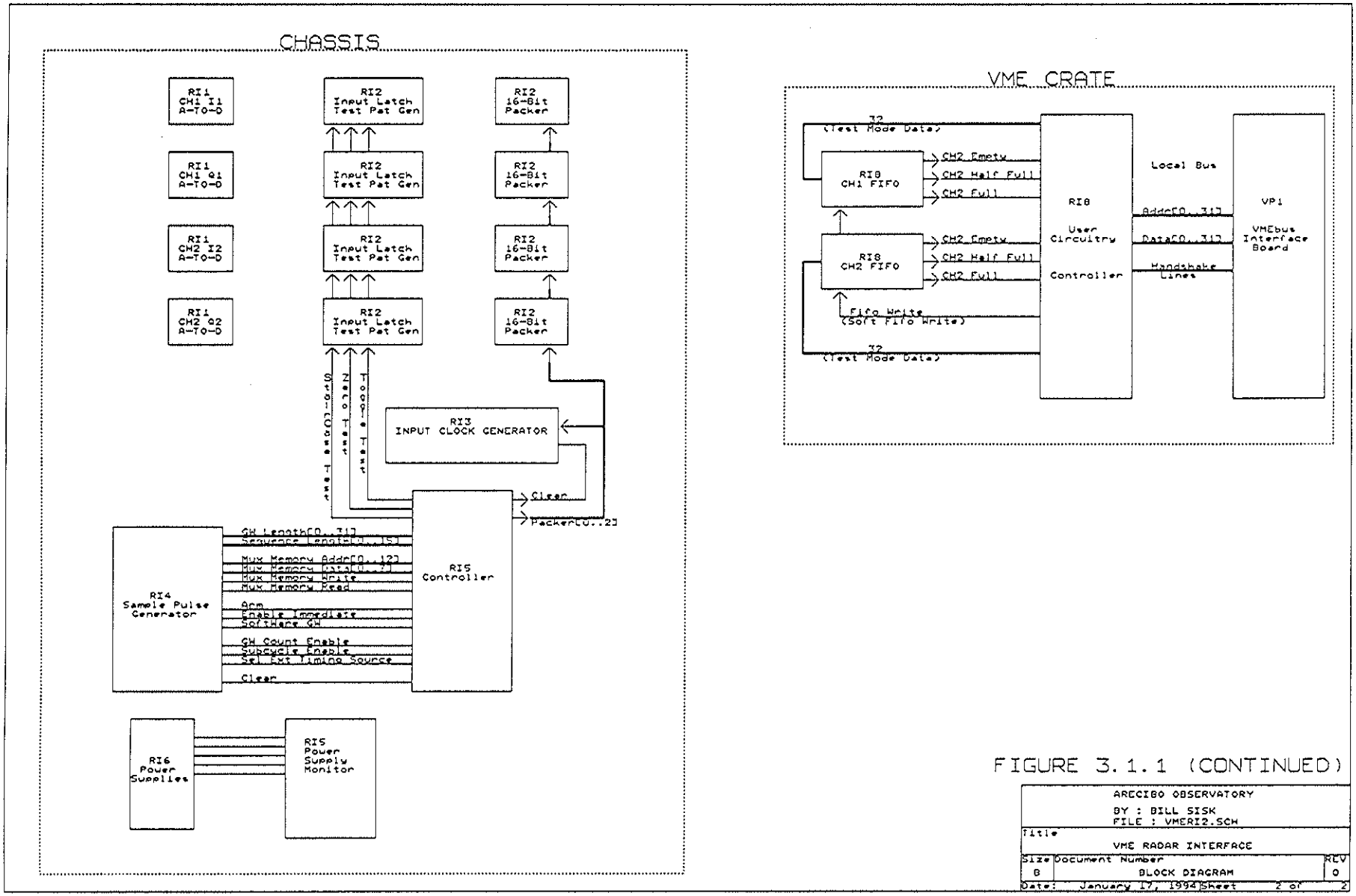
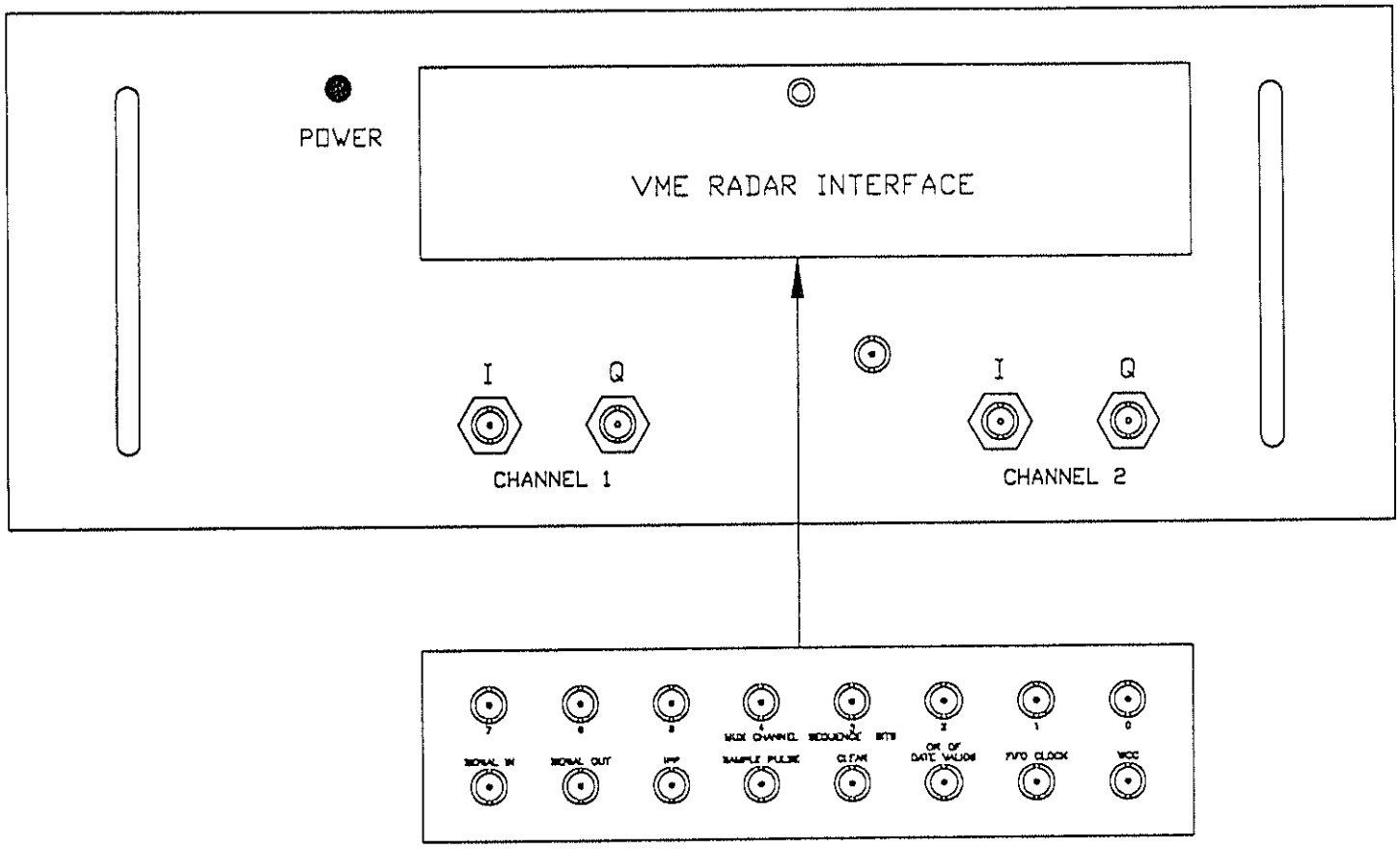


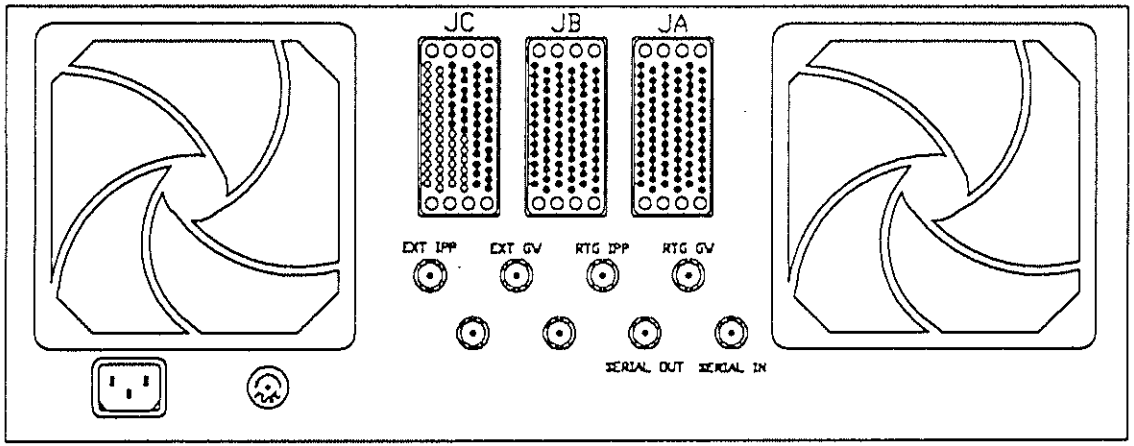
FIGURE 3.1.1 (CONTINUED)

ARECIBO OBSERVATORY BY : BILL SISK FILE : VMERI2.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: BLOCK DIAGRAM	REV: 0
Date: January 17, 1994	Sheet 2 of 2	



FILE: VME1

DATE 2-9-93	*ARECIBO OBSERVATORY* CORNELL UNIVERSITY	SCALE
APPR. BILL SISK	VME RADAR INTERFACE FRONT PANEL	SHEET NO.
BY G.A.SERRANO		



	2-12-93	*ARECIBO OBSERVATORY* CORNELL UNIVERSITY	
	BILL SISK	VME RADAR INTERFACE BACK PANEL	
	G.A.SERRANO		

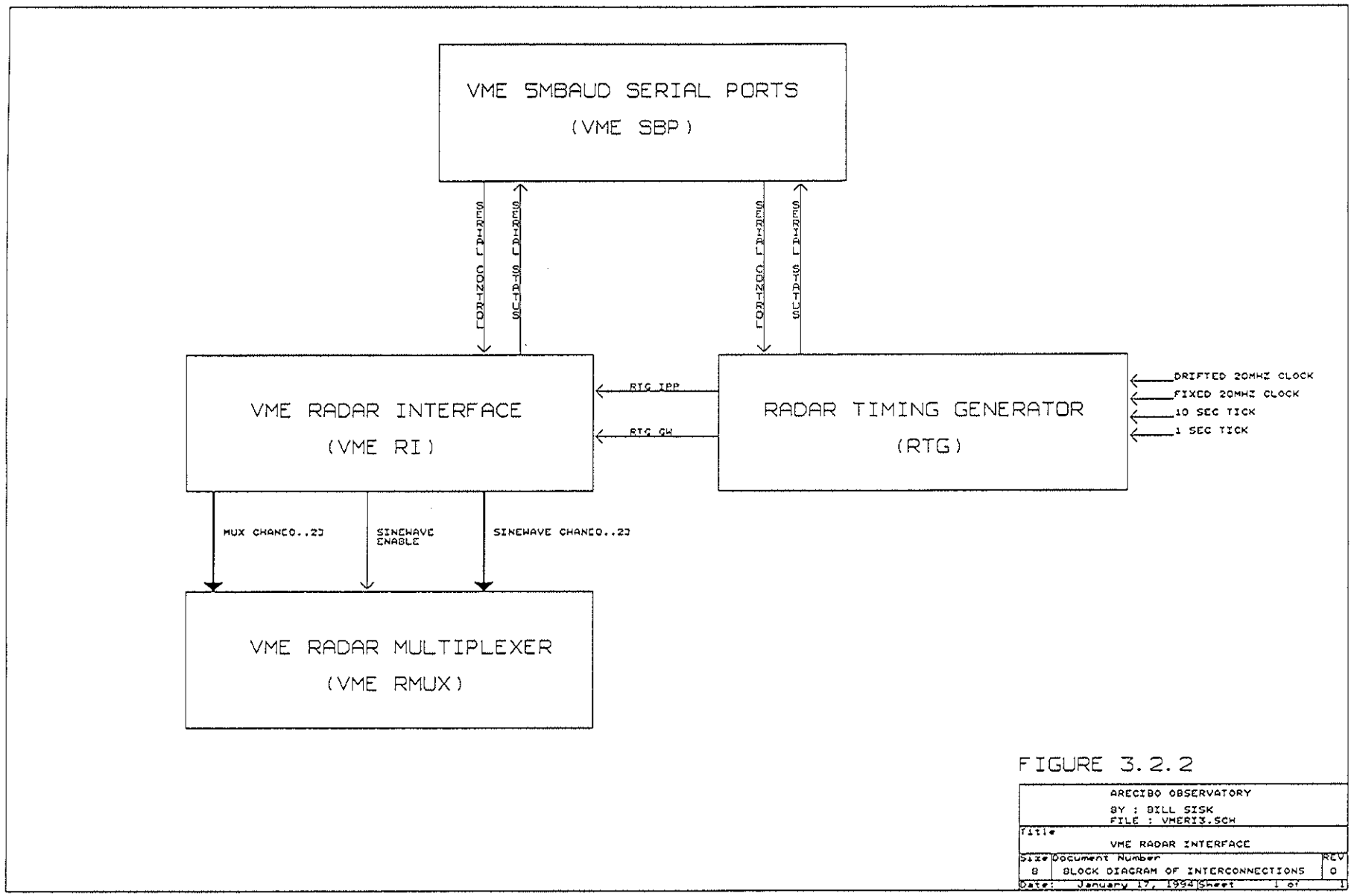


FIGURE 3.2.2

ARECIBO OBSERVATORY BY : BILL SISK FILE : VMERI3.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: BLOCK DIAGRAM OF INTERCONNECTIONS	REV: 0
Date: January 17, 1994	Sheet 1 of 1	

3.3 The Computer Connection

Communication between the VME RI and the VMEbus Single-Board Computer (System Controller) is done in two different ways. Setup information is sent to the Controller (RI5) in the chassis of the VME RI over a coaxial cable using a 5 MHz serial format. This information consists of "configuration words" to set sampler options, etc. RI5 can send back, when requested, status and verification information over a second coaxial cable. The System Controller uses the VME SBP, a VMEbus slave board that is dedicated to handling communications using the 5 MHz serial format, to talk to the VME RI and other peripherals.

The System Controller also directly communicates with the VME RI over the VMEbus. Module RI8 is both a master and slave on the VMEbus. As a slave, it receives setup information and responds to requests for status. As a master, it transfers the data from the FIFOs to a designated buffer on the VMEbus. Section 3.8 will explain data transfer to the VMEbus.

3.4 Digitizer Timing and Control

The digitizer control circuitry uses two externally supplied timing signals, the "GW" (Gate Width) and the "IPP" (InterPulse Period), which are nominally the sampler trigger and the trigger enable or start pulse. Two sets of GW and IPP inputs are provided. One set is connected from the RTG and an alternate set from the VME SPS or another timing source. The selected set controls all four digitizers simultaneously.

One can enable the VME RI to begin sampling (i.e. to accept GW pulses) immediately, or one can arm it to be automatically enabled by the next IPP pulse. Once sampling has begun, the 16-Bit Packer assembles the digitizer output into 16-bit words, which are then written into the FIFO buffer memories. Typical data-taking methods are discussed in sections 3.5 and 3.6.

3.5 Pulse Radar Data-Taking

Typically, a timing source, such as the RTG, provides more GW pulses in an IPP than are wanted for sample pulses. In the Harris RI, the FIFOs continue to fill up with unwanted samples, and thus it is necessary to clear the FIFOs before the start of each IPP. This can limit the data rate.

The VME RI is different. Before sampling is initiated, the VME RI is configured with the desired number of sampling pulses per IPP (GW Count Mode). After completing this count, sampling pulses will stop until the next IPP, and thus the FIFOs fill only with 'good data'. If the specified number of sampling pulses does not occur in a IPP, a status error flag (GW Count Error Flag) is set. GW Count Mode can be disabled for timing sources, such as the VME SPS, that produce the correct number of GW pulses in an IPP.

A typical sequence of events is as follows. At the start of data taking, the System Controller configures all the necessary registers in the VME RI. It then sends a command word to execute a CLEAR. This stops all previous sampling, clears the FIFOs, and readies all circuitry for a new timing cycle. Once CLEAR completes, the samplers are armed to be enabled at the next IPP. Sampling will stop at the preprogrammed number of sample pulses, and rearm the samplers to be enabled at the next IPP. No CLEAR command is necessary after the initial one.

3.6 Continuous Sampling

Continuous sampling is similar to Pulse Radar Data-Taking. The number of sample pulses in an IPP can be programmed to a maximum of 2e32 using GW Count Mode. Arming can be done on the start of an IPP. The RTG has a provision for continuous sampling in that it can be programmed to provide a continuous train of Gate Width pulses. Only one IPP occurs; subsequent IPP pulses which would resynchronize the GW train are absent.

Alternatively, if an IPP is not available, one can program the VME RI to begin accepting GW pulses immediately at the end of the CLEAR command. If GW Count Mode is used, a CLEAR is necessary to restart sampling when the GW Count completes. Caveat : The GW pulses in the timing source should be disabled until after the sampling mode has been enabled in the VME RI (after CLEAR). This is because CLEAR and the GW pulses are asynchronous; thus, sampling could be enabled while a GW pulse is occurring.

3.7 Parallel Communications to the VME Crate

All time-critical signals between the chassis of the VME RI and the VME Crate are sent in parallel using 72 twisted-pair, unidirectional, transmission lines. Sixty-four signals are the words from the four 16-Bit Packers (RI2). One pair (Fifo Clock) is used to clock the data into the FIFOs.

Two pairs are used are to initiate and synchronize the start of data taking between the VME crate and the chassis of the VME RI. The initiate signal, called CLEAR, originates from RI8. RI5 acknowledges the reception of CLEAR by returning a signal, called ACK, and which terminates CLEAR in RI8, and synchronizes the timing in the two locations.

The remainder of the pairs are used for the transmission of status information.

3.8 Data Transfer to the VMEbus

Once the FIFOs start filling, it is desirable to empty them as fast as possible. Depending on the experiment, the data may be sent to a memory buffer on a single-board computer, an array processor, or a memory board, and then eventually the raw or processed data is put on tape.

Before data transfer starts, registers on RI8 are loaded with a 32-bit first address and a 24-bit word count. The first data word from the selected FIFO will be sent to the VMEbus address given by the first address. Every succeeding data word will be sent to an address augmented by 4 from the previous address. (A 32-bit data word will be aligned on 4-byte address boundary.) The word count is the number of data words that will be sent to contiguous addresses (size of memory buffer).

When all the configuration registers have been loaded and data taking is ready to begin, a Command Word is sent the VME RI that enables CLEAR and either Single Word Transfer or Block Transfer. As soon as there is data in the FIFOs, RI8 requests the VMEbus. When granted the VMEbus, it becomes the VMEbus master and transfers one word (Single Word Transfer) or 64 words (Block Transfer) before releasing the VMEbus. When the total memory buffer has been written, RI8 generates a VMEbus interrupt to alert the System Controller that the transfer is complete. The System Controller can then read the Status Word to check for error conditions.

3.9 Using the Analog Multiplexer

The VME RMUX is a companion chassis to the VME RI. The VME RMUX contains two 8-to-1 analog multiplexers operating in tandem to select one of 8 port pairs. The VME RMUX analog output lines must be externally connected to the VME RI's analog inputs. A 8 X 8K byte memory in the VME RI is preloaded with the desired port-pair sequence. The three LSBs of the memory are sent to the VME RMUX and decoded to select the desired channel.

The starting channel of the VME RMUX is set up and settles before sampling begins. The sequence pointer advances when sampling is underway. For this purpose, the VME RI is preloaded with the Sequence Length (which is equal to one less than actual cycle length, N). If N = 1, the sequence pointer never advances and the multiplexer selects the port number indicated by the first memory location. If N > 1, the sequence pointer advances after every conversion, cycling through the port numbers contained in the first N locations in the 8K memory (starting at address N-1 and stopping at address 0). The memory is reset to the starting location when sampling begins and after every N sample pulses.

3.9.1 Subcycle Sampling

One sometimes wants to sample several analog port-pairs simultaneously at each GW pulse. The VME RI can approximate this by executing a fast (nominally 5.0 MHz) subcycle, triggered by each GW pulse. The length of the subcycle is set through the same multiplexer cycle length field (Sequence Length). At the end of the subcycle the memory is reset.

Note : the programmed time between GW pulses must be long enough to let the subcycle complete, that is Gate Width $\geq$(N * 0.2us)

3.9.2 Filterbank Multiplexers

The VME RI can be used with multiplexers other than the VME RMUX. In particular, external filter banks can have built-in multiplexers. These multiplexers use the eight Channel Sequence Bits coming out of the front panel of the RI Chassis.

4.0 SOFTWARE REQUIREMENTS

4.1 Serial Communications

Tables 4.1-6 show the bit assignments for 24-bit serial words sent to configure the chassis of the VME RI. Only the Channel Sequence Memory data can be read back, as part of the Auxiliary Status Word (Table 4.7).

Note : The highest numbered bit is always the most significant in the following bit assignments.

TABLE 4.1.1 : Bit Assignments for Sampler Configuration Word

Bits	Description
23,22,21	Set to 0 to identify Sampler Configuration Word
20	Unassigned
19	Timing Source 0 : RTG (Radar Timing Generator) 1 : External Timing Source
18,17	Sampling Mode 0 : Sampling Disabled; sampler is not enabled after CLEAR (*). 1 : ARM ; sampler is enabled on the next IPP after CLEAR (*). 2 : ENABLE IMMEDIATE; sampler is enabled immediately after CLEAR (*). 3 : SOFTWARE GW ; one GW pulse is generated immediately after CLEAR (*). If subcycle mode is enabled, N sampling pulses will be generated.
16,15	Packer and Fifo Test 0 : Staircase Test ; packers are fed with increasing digital numbers (numbers are in a bit reversed format; the most significant bit changes the fastest). 1 : Toggle Test ; packers are fed with all zeroes or all ones on every other sample. 2 : Normal Sampling ; packers receive data from the digitizers. 3 : Zero Test ; packers are fed with all zeros.
14,13,12	Packing Format 0 : 12 bit , sign extended to 16 bits 1 : 8 bit 2 : 4 bit 3 : 2 bit 7 : 1 bit
11	Subcycle Mode 0 : Disable Subcycle Mode 1 : Enable Subcycle Mode ; Every gate width pulse starts a sampling subcycle. Samples are spaced by 200ns. For a sequence of N samples, the Sequence Length must be set to N-1.
10	GW Counting 0 : Disable GW counting 1 : The GW Length sets the number of sample pulses per IPP. The GW Count Error Flag is set if the number of GW pulses occurring in an IPP is less than the GW Length.

9 - 7	Multiplexer Sinewave Test Channel (Binary Coded Channel, 0-7)
6	0 : Disable Mux Sinewave Test ; mux channel source is the normal front panel input. 1 : Enable Mux Sinewave Test ; mux channel source is a 460 KHz sinewave.
5 - 0	Unassigned

TABLE 4.1.2 : Bit Assignments for Channel Sequence Memory Word

The first mux channel in a sequence is at address N-1, where N is the number of channels in the sequence. The last mux channel in the sequence is at address 0. When sampling, the address is given by the Sequence Counter which counts from N-1 to 0.

Bits	Description
23,22,21	Set to 1 to identify Channel Sequence Memory Word
20 - 8	Memory Address
7 - 0	Memory Data

TABLE 4.1.3 : Bit Assignments for GW Length LSB's Word

The GW Length is a 32-bit word. It is loaded in two serial words. The GW Length is set to one less than the number of desired sample pulses.

Bits	Description
23,22,21	Set to 2 to identify GW Length LSB's Word
20-16	Unassigned
15 - 0	16 LSB's of GW Length

TABLE 4.1.4 : Bit Assignments for GW Length MSB's Word

Bits	Description
23,22,21	Set to 3 to identify GW Length MSB's Word
20 - 16	Unassigned
15 - 0	16 MSB's of GW Length

TABLE 4.1.5 : Bit Assignments for Sequence Length Word

The Sequence Length is set to one less than the actual cycle length.

Bits	Description
23,22,21	Set to 4 to identify Sequence Length Word
20 - 16	Unassigned
15 - 0	16 bits of Sequence Length

TABLE 4.1.6 : Bit Assignments for Request Auxiliary Status Word

Request Auxiliary Status Word : the Auxiliary Status Word, whose bit assignments are given in Table 4.1.7, is transmitted serially to the VME STR. Caveat : Do not request the Auxiliary Status Word while taking data using a multiplexer.

LoopBack Test : The entire Request Auxiliary Status Word can be read back to the System Controller to verify two-way serial connection between the VME RI and the VME SBP.

Bits	Description
23,22,21	Set to 5 to identify Request Auxiliary Status Word.
20	Unassigned
19	0 :Send the Auxiliary Status Word (Table 4.1.7) 1 : Loopback Test
12 - 0	Channel Sequence Memory Address The data byte at this address will be returned in the Auxiliary Status Word.

TABLE 4.1.7 : Bit Assignments for Auxiliary Status Word

Bits	Description
23 - 13	Unassigned
12	+15V Power Supply Out-of-Range
11	-15V Power Supply Out-of-Range
10	+5V Analog Power Supply Out-of-Range
9	-5V Power Supply Out-of-Range
8	+5V Logic Power Supply Out-of-Range
7 - 0	Channel Sequence Memory data byte at address given by bits 12-0 of Request Auxiliary Status Word.

4.2 VMEbus Communications

Tables 4.2.1 is the address decoder for slave accesses to the VME RI over the VMEbus. Table 4.2.2 is the bit assignments for the Command Word. Table 4.2.3 are the bit assignments for the Status Word.

TABLE 4.2.1 : VMEBus Address Decoder

32-bit Address	Read/ Write*	Description of Data Word D[31..0]
C3000000	0	32-bit First Address of the VMEbus Buffer for data transfer from the FIFOs. D[31..0]
C3000004	0	24-bit Word Count (size of buffer) for data transfer from the FIFOs. D[23..0]
C3000008	0	Command Word. See Table 4.2.2 for a description of the data word bit assignments. D[7..0]
C300000C	0	Soft FIFO Write when in Test Mode. The data word is loaded into CH1 FIFO. It's complement is loaded into CH2 FIFO. D[31..0]
C3000000	1	Read Status Word. See Table 4.2.3 for a description of the data word bit assignments. D[31..0]

TABLE 4.2.2 : Bit Assignments for Command Word

Bit	Description	
0	0 :	NOP
	1 :	CLEAR (*) & start sampling if a Sampling Mode is enabled in the Sampler Configuration Word.
1,2	0 :	NOP
	1 :	Enable Single Word Transfer ; when there is data in the selected FIFO, start transferring it to the VMEbus buffer starting at the First Address. Disable data transfer when the Word Count is complete.
	2 :	Enable Movem Block Transfer ; when there is data in the selected FIFO, start a block transfer to the VMEbus buffer starting at the First Address. Disable data transfer when the Word Count is complete.
	3 :	Disable Data Transfer
3,4	0 :	NOP
	1 :	Enable CH1 FIFO for data output.
	2 :	Enable CH2 FIFO for data output.
	3 :	Alternately Enable CH1 FIFO and CH2 FIFO for data output. A CLEAR must be done in this Command Word or later to insure that CH1 is the first channel read.
5,6	0,3:	NOP
	1 :	Disable Test Mode
	2 :	Enable Test Mode ; FIFOS are loaded from the VMEbus using Soft FIFO Write. The normal inputs are Tristated.
7	0 :	NOP
	1 :	Clear IPP Flag in Status Word.

TABLE 4.2.3 : Bit Assignments for Status Word

Bit	Description
31	Selected FIFO is empty.
30	Selected FIFO has overflowed. Flag is reset by CLEAR (*). (Overflow is defined as the FIFO Full Flag becoming active.)
29	Selected FIFO is more than half full.
28	GW Count Error Flag ; Reset by CLEAR (*). See explanation of flag in Sampler Configuration Word.
27	Sampling Enabled Flag ; Reset by CLEAR (*). The flag is set by the first IPP pulse after sampling has been enabled.
26	Parity Error Flag ; Reset by CLEAR (*). This flag indicates that a parity error has occurred in the Serial Receiver.
25	CLEAR Flag ; This flag indicates that CLEAR (*) is active. When CLEAR (*) is initiated, it should terminate in RI8 on reception of ACK. In Test Mode, the CLEAR is terminated after the Command Word is acknowledged in the handshake cycle on the local bus.
24	IPP Flag ; Reset by a bit in the Command Word. The flag is triggered by the IPP selected by the Timing Source in the Sampler Configuration Word.
23 - 0	Word Count ; The Word Count indicates the remaining number of data words to be transferred until the VMEbus buffer is full.

(*)

1) disables sampling.
(2) clears the FIFOs.
(3) clears the GW Counter.
(4) initializes the Sequence Counter and the first mux channel.
(5) clears the Staircase Generator Counter.
(6) initializes the Input Clock Generator Counter.
(7) initializes the first channel in Alternate Channel Mode
(8) clears the GW Count Error Flag.
(9) clears the Sampling Enabled Flag.
(10) clears FIFO Overflow Flag
(11) clears the serial receiver Parity Error Flag
(12) clears the power supply out-of-range flags
(13) if ARM, ENABLE IMMEDIATE, or SOFTWARE GW has been selected in the Sampler Configuration Word, sampling is enabled after CLEAR ends.

5.0 SPECIFICATIONS

5.1 Analog Inputs

No. of Inputs	4 (2 pairs)
Sampling Rate	10 Megasamples/sec max
Dynamic Range	12,8,4,2, or 1 bits
Converted Code	Two's Complement
Full Scale Range	±2.5 Volts @ Front Panel ±1.25 Volts @ ADC
Input Clamping Voltage	±2.0 Volts @ ADC
Input Impedance	50 Ω @ Front Panel
Data Format	CH1 Bits 32-16 : Q1 CH1 Bits 15-0 : I1 CH2 Bits 32-16 : Q2 CH2 Bits 15-0 : I2
Packing Format	12, 8, 4, 2, 1 bit packing into 16-bit word. Sign-extension on 12-bit packing.
Buffer Memories	Two 32 X 32K FIFOs The computer can read either : a. from a single FIFO, or b. alternate words from alternate FIFOs
Analog Test Source	2 volt (peak) sine wave source at 460.8 KHz can be selected in the VME RMUX with the normal inputs disabled. The mux channel is selected in the Sampler Configuration word.

5.2 Digital Input

Test Pattern Generator :
Four built-in up-counters can be selected in place of the digitizers to provide artificial data to test the Packers/FIFOs. CLEAR clears these counters. Note : In order to test all formats, these counters are bit reversed, i.e. the normal MSBs in the data words will toggle from one sample to the next.

TEST MODE :
The FIFOs can be loaded from the VMEbus to partially test module RI8 independent of the modules in the chassis of the VME RI.

5.3 Serial Control Port

No. of Port Pairs	1 Tx/Rx pair
Code	Biphase (see Fig 6.1)
Data Rate	5 MBaud (24-bits/4.8 microsecond)

5.4 Data Transfer Rate onto VMEbus

Single Word Transfer	9 Megabytes/second
Block Transfer	13.8 MBytes/sec (Motorola 167-25) 15.4 MBytes/sec (Motorola 167-33)

5.5 Power Requirements

RI Chassis :

+5 Volt Analog : 2.0 A
-5.2 Volt : 2.8 A
+15 Volt : 250 mA
-15 Volt : 250 mA
+5 Volt Logic : 3.6 A

5.6 RI8 VMEbus Identity

Slave Accesses :

A16 Address Range	7400 - 743F (64 Bytes)
A32 Address Range	C3000000 - C300FFFF (16K words)
Data Size	D32

Master Accesses :

Bus Request Level	BR3
Bus Release Mode	ROR - Release on Request

Interrupts :

Interrupt Number	4
ID Vector	B7

6.0 THEORY OF OPERATION

The block diagram, Figure 3.1, together with Sections 3, 4, and 5 of this manual provides an overall description of the functionality and architecture of the VME RI. This section expands on what has been covered previously and also discusses some circuitry. To obtain a detailed understanding, the schematic diagrams, PAL equations, and the PME VP-1 Manual (reference 2.4) should be studied.

6.1 RI1 Digitizers

Each of the four digitizer modules contains a Burr Brown ADC603 A-to-D converter (see Sec. 9.1 for data sheet). The ADC603's are mounted on printed circuit boards along with other circuitry. The analog input of the ADC603 is buffered by an external unity gain op-amp (Comlinear CLC502). The op-amp has an output clamping feature which limits the positive and negative output voltage levels. It protects the ADC603 from destructive transients or signals that would otherwise cause saturation. The CLC502's overload recovery time of 15ns is also much faster than the 140ns spec. of the ADC603.

There are two methods for reading output data from the ADC603. The Data Valid timing option is used in the VME RI. With this option, data for the conversion becomes valid after a fixed delay from the rising edge of the convert command. The delay is approximately 135ns, at which time the Data Valid strobe signal will rise. The pc board has a fast D-type register to latch the output data. It is necessary because as the sampling rate increases, the hold time for the output data decreases. (e.g. ~5ns at 10 MHz sampling rate).

6.2 RI2 Input Latch/Test Pattern Generator & 16-Bit Packer

These modules contain the counter/latches made of PAL22V10's, which load synchronously (for the latch function) and clear asynchronously (to initialize the test count). They also provide two other test modes. The Zero Test mode will always latch zeros into the output registers. The Toggle Test mode will alternately latch all zeros or all ones on every other sample pulse.

The module also contains the four 16-bit Packers, each made out of 4 PAL20V8's. Each Packer assembles a 16-bit word from its 12-bit digitizer. In sign-extended 12-bit mode, the upper 4-bit register latches the sign of the lower 12-bits. When 8 or fewer bits are used, the Packer is reconfigured as an n-wide shift register with parallel clocking. It is clocked with sequential samples until it is full.

Each digitizer produces a Data Valid pulse. The Data Valid pulses from all four digitizers are OR'ed and AND'ed in RI2. The OR of Data Valids is sent to RI3, the Input Clock Generator, and is used to generate the Latch Clock, the Packer Clock, and FIFO Clock. The AND of Data Valids can be used as a test point to quickly determine if a digitizer is failing.

6.3 RI8 FIFO's

The FIFO chips use internal dual-port RAMS so that input and output can be asynchronous and totally independent. The FIFOs include input and output address pointers so the depth of the FIFO does not affect the pinout.

Since the Packers and FIFOs are separated by a cable length of ~15 ft., differential line drivers and receivers are used to transfer the data between the two locations. The differential driver/receiver chips are specified to a maximum rate of 20 Megabits/second. The twisted-pair transmission lines are terminated in 120Ω.

In Test Mode, the differential line receivers are tri-stated, and the FIFOs are loaded from the VMEbus.

The FIFOs are labelled as the CH1 FIFO and CH2 FIFO, each consisting of four 8-bit FIFO chips in parallel. The lowermost 16 bits are from the I digitizer port and the uppermost bits are from the Q port.

The FIFOs have flags that indicate empty, half full, and full conditions. If the FIFOs become full, writes to the FIFO are inhibited until a CLEAR occurs, even if the FIFOs are read and the full condition is no longer true. The full flag is latched and can be read in the Status Word as a FIFO Overflow Error. This design consideration was implemented because data in the FIFOs is otherwise corrupted. The reason is as follows: The FIFO full condition changes from true to false asynchronously with respect to the FIFO write pulse. Thus, the active portion of the write pulse can be reduced so that it doesn't meet the minimum pulse width. A write pulse that is too short corrupts the good data in the FIFOs.

6.4 RI3 Input Clock Generator

This module delays the OR of Data Valids to allow an appropriate setup time before the digital data is clocked into the Input Latches. It is further delayed to produce the Packer Clock and the FIFO Clock. When shorter than 12-bit words are selected, the FIFOs are clocked only when a packed word has been fully assembled, i.e. every 16/n samples.

6.5 RI4 Sample Pulse Generator

The prime function of this module is to take the Gate Width pulse and pass it on as trigger to the four digitizers. This module also synchronizes the start of data taking with the IPP (ARM mode) or the termination of CLEAR (ENABLE IMMEDIATE mode). The module contains the Gate Width Counter, the Sequence Length Counter, the subcycle mode circuitry, and Channel Sequence Memory.

The GW Counter is used primarily when the timing source is the RTG, because the RTG usually generally generates an excess number GW pulses in an IPP. By using the GW Counter, only the desired number of GW pulses in an IPP will be used to generate sample pulses. The GW Counter is a 32-bit down-counter and thus, the allowable number of sample pulses in an IPP is 1 to 2e32. CLEAR clears the GW Counter. The first GW in an IPP loads the counter with the initial value, which is one less than the desired number of sample pulses. When the GW Counter counts down to zero, it will disable subsequent sample pulses, and thus stop its own clock. If GW Counter doesn't count to zero in an IPP, the GW Count Error Flag is set. This flag can be read in the Status Word. The GW Counter can be disabled, since it is not needed with timing sources such as the VME SPS.

The Sequence Length Counter has two purposes. When an analog multiplexer is used, it is the address pointer for the Channel Sequence Memory. When cycle mode is used, it determines the number of sample pulses generated by every GW pulse. When cycle mode and a multiplexer are used, and the Channel Sequence Memory will cycle through the complete channel sequence on every GW pulse at a 5MHz rate.

The Sequence Length Counter is a 16-bit counter. CLEAR will load the initial value of the counter, and thus the first address of the Channel Sequence Memory. Thus, the first channel of multiplexer will have time to settle before the first sample pulse. The initial value of the counter is one less than the desired cycle length. When the counter counts to zero, the next GW will reinitialize it. Thus, multiple complete sequences can occur in an IPP.

The Channel Sequence memory is an 8K X 8, 12ns SRAM. Since the memory data is indeterminate when the address lines are changing, it is necessary to latch the data at an appropriate delay after the address has changed. The three LSBs of the memory are sent to the VME RMUX using ECL differential drivers and decoded in the VME RMUX to enable one of eight channels. All eight memory bits are available on the front panel as TTL 50 ohm drivers for other analog multiplexers.

The timing between the sample pulse and the change of channels in the multiplexer is critical at high sampling rates. The proper timing is determined by measurement and by an understanding of the multiplexer and A-to-D converter dynamics. The timing is controlled by the delay lines, Q77 and L26, in RI4.

6.6 RI5 Controller

This module has the serial interface and latches for the configuration words. The module also receives the CLEAR signal from RI8, and returns an acknowledge pulse (ACK).

The 5 MHz serial format is shown in Figure 6.6.1. There are 24 data bits and a terminating parity bit in the format. A transition occurs at the start of every 200ns cell. If the data bit is a "1", there is also a transition at midcell. The number of "1's", including the parity bit will always be odd (odd parity).

The serial interface consists of a serial receiver and a serial transmitter, each connected to the VME SBP by coaxial cable. When a word is received, a Data Ready strobe is generated. The data is decoded and latched into registers. If there is a parity error on receiving a serial word, the Parity Error Flag will become active. It is sent on a status line to RI8 and can be read from the Status Word. It should be checked after every serial transmission. CLEAR will reset the Parity Error Flag.

6.7 RI8 Interface to the VMEbus

RI8 was designed to provide fast data transfer from the FIFOs to the VMEbus. It uses a VMEbus prototyping board, the VP-1 from Radstone Technology. A VP-1 user is spared the complexity of designing VMEbus circuitry; the VP-1's local bus is much simpler. The protocol of the local bus is equivalent to protocol of a 68020 processor.

The VP-1 is based around the VMEbus Interface Controller IC, the VIC068A from Cypress Semiconductor. Additional circuitry, henceforth called the user circuitry, must be added to make the board useful. The user circuitry communicates with the VIC068A over a local bus. The schematics for RI8 show only the user circuitry. For a thorough understanding, the PME VP-1 Manual should be read in addition to the following discussion.

The VP-1 is capable of handling VMEbus Master, Slave, and Interrupt Cycles. The VMEbus computer (System Controller) uses the Slave Write cycle to write the First Address, Word Count, and Command Word to RI8. The Slave Write cycle is also used to load the FIFOs with data in Test Mode (Soft Fifo Write). A Slave Read cycle is used to read the Status Word. A timing diagram for Slave Read and Write is shown in Figure 6.7.1.

To transfer data from the FIFOs to the VMEbus, the VP-1 becomes a VMEbus master. RI8 has the option to transfer data using two different local bus/VMEbus cycles, Master Write (Single Word Transfer) and Movem Write (normally called a Block Transfer (BLT) on the VMEbus). BLT's are faster, but are not supported by some VMEbus boards. Figure 6.7.2 is a flow chart for the data transfer process.

The Master Write cycle is relatively easy. When it is enabled by the Command Word, a VMEbus transfer will occur as soon as the selected FIFO is not empty and the VMEbus is granted to the VP-1.

The Movem Write cycle is more complex. The user circuitry initiates a Movem Write by writing to a register in the VIC068A. The BLT will start as soon as the selected FIFO is not empty and the VMEbus is granted to the VP-1. The VMEbus standard forbids BLT's from crossing 256 byte address boundaries. The user circuitry stops the BLT on 256 byte boundaries by writing to a register in the VIC068A (the same register used to start the BLT, but with a different data byte), and then restarts another BLT. The Movem Write will also stop if the selected FIFO becomes empty, and wait until it becomes non-empty before starting another BLT.

When the word count is complete, data transfer to the VMEbus is disabled, and remains disabled until another Command Word is written. To inform the System Controller that the word count is complete, the user circuitry writes to a register in the VIC068A that initiates a VMEbus interrupt.

Data transfer will also be disabled and a VMEbus interrupt will be generated if the FIFO Overflow Flag and FIFO Empty Flag are both active. This can occur before the Word Count is complete and indicates that the Word Count cannot be completed because writes to the FIFOs are inhibited. Thus, it is advisable to read the Status Word after the interrupt cycle to determine the cause of the interrupt.

RIPAL31 is a state machine which makes all the decisions on what to do based on the inputs (FIFO Empty, Boundary Crossing, Word Count Complete) during a Master data transfer.

The registers in the VIC068A are configured on boot up from an EPROM on the VP-1. The configuration is stored at an offset of $1000 from the start of the EPROM. The original EPROM was modified and the new listing is shown in Table 6.7.1.

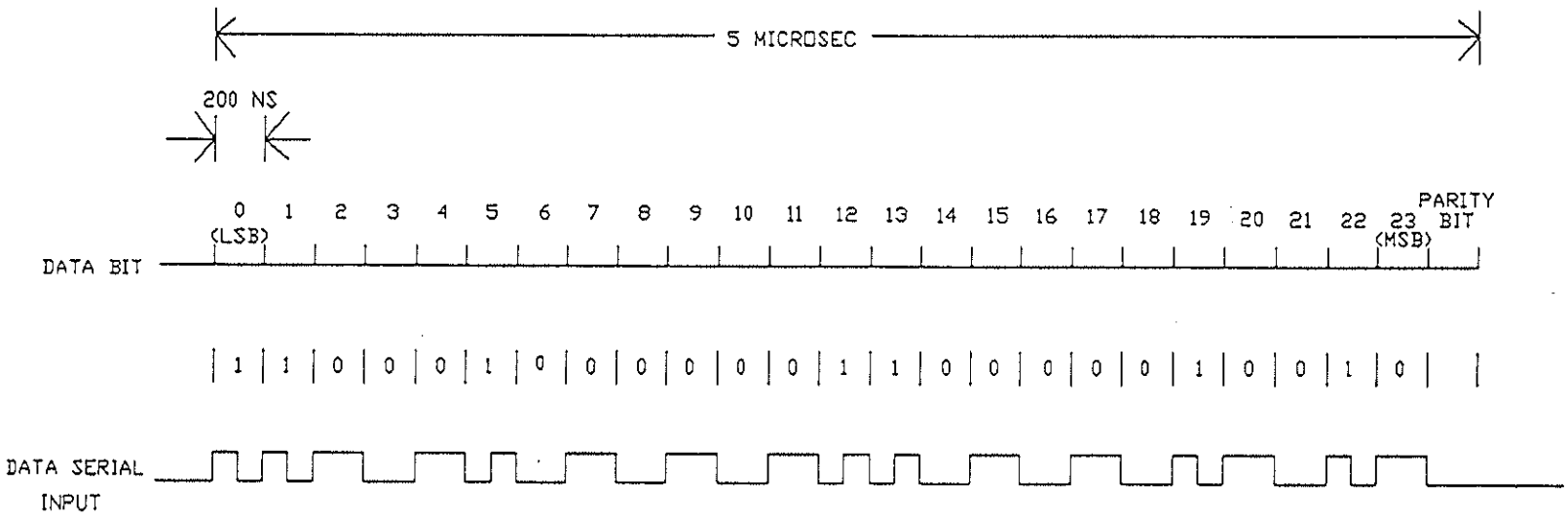
The hardware configurable features on the VP-1 are listed in Table 6.7.2.

TABLE 6.7.1 VP-1 REGISTER CONFIGURATION

Address (hex)	Name	Description	Data (hex)
47	ICMSICR	ICMS Interrupt Control Register	E9
C3	SS0CR0	Slave Select 0 Control Reg. 0 (A24, D32)	15
CB	SS1CR0	Slave Select 1 Control Reg. 0 (A32, D32)	11
A7	LBTR	Local Bus Timing Register (Min DS*,PAS* deasserted time)	30
B3	ARCR	Arbiter/Requester Config. Reg. (No DRAM refresh; BR3)	60
93	VIVBR	VMEbus Interrupt Base Register (Interrupt 4, ID Vector B7)	B7
C7	SS0CR1	Slave Select 0 Control Reg. 1 (min SAT)	00
CF	SS1CR1	Slave Select 1 Control Reg. 1 (min SAT)	00
78	ICR6	Interprocessor Communication Reg. 6 (Local Resources are running and operational.)	00

TABLE 6.7.2 VP-1 HARDWARE CONFIGURATION

SW1 : 0 LK23 : jumpered LK22 : no jumper	The A16 VME address range for the inter-processor communication registers in the VIC068A is 7400-743f hex (64 bytes).
LK15 : Link 2 & 3 LK17 : " " LK19 : " " LK21 : " " LK14 : " " LK16 : " " LK18 : " " LK20 : " "	The A24 VME address range for Slave 0 in the VIC068A is 000000 - 00FFFF hex (64K). A24 addressing is not used, but the address range (64K) applies to A32.
LK9 : no link LK8 : no link LK7 : link LK6 : link LK5 : link LK4 : link LK3 : no link LK2 : no link	The A32 VME address range for Slave 1 in the VIC068A is C3000000 - C300FFFF hex. (16K words)
LK10 : no link LK11 : link LK12 : link LK13 : no link	The interrupt level from the VIC068A which maps onto the non-maskable interrupt on the 63A03X processor is level 1.
LK1 : no link	The VP-1 is not the system controller.

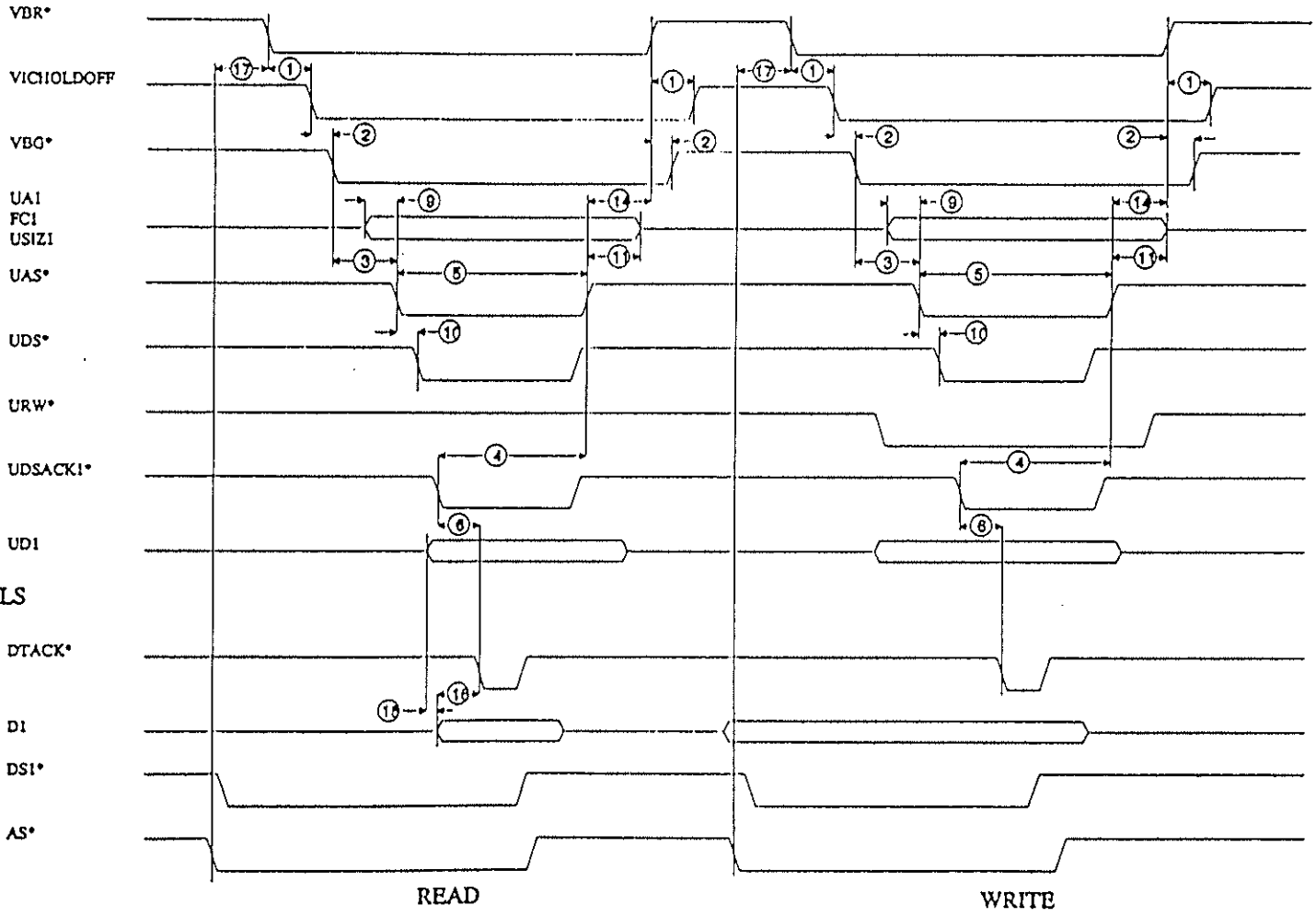


NOTE: INPUT HAS A TRANSITION AT THE BEGINNING OF EACH 200 NSEC CELL
IF THE DATA IS A '1' THERE IS ALSO A TRANSITION AT MIDCELL
THE NUMBER OF '1 s' INCLUDING THE PARITY BIT WILL ALWAYS BE ODD (ODD PARITY)

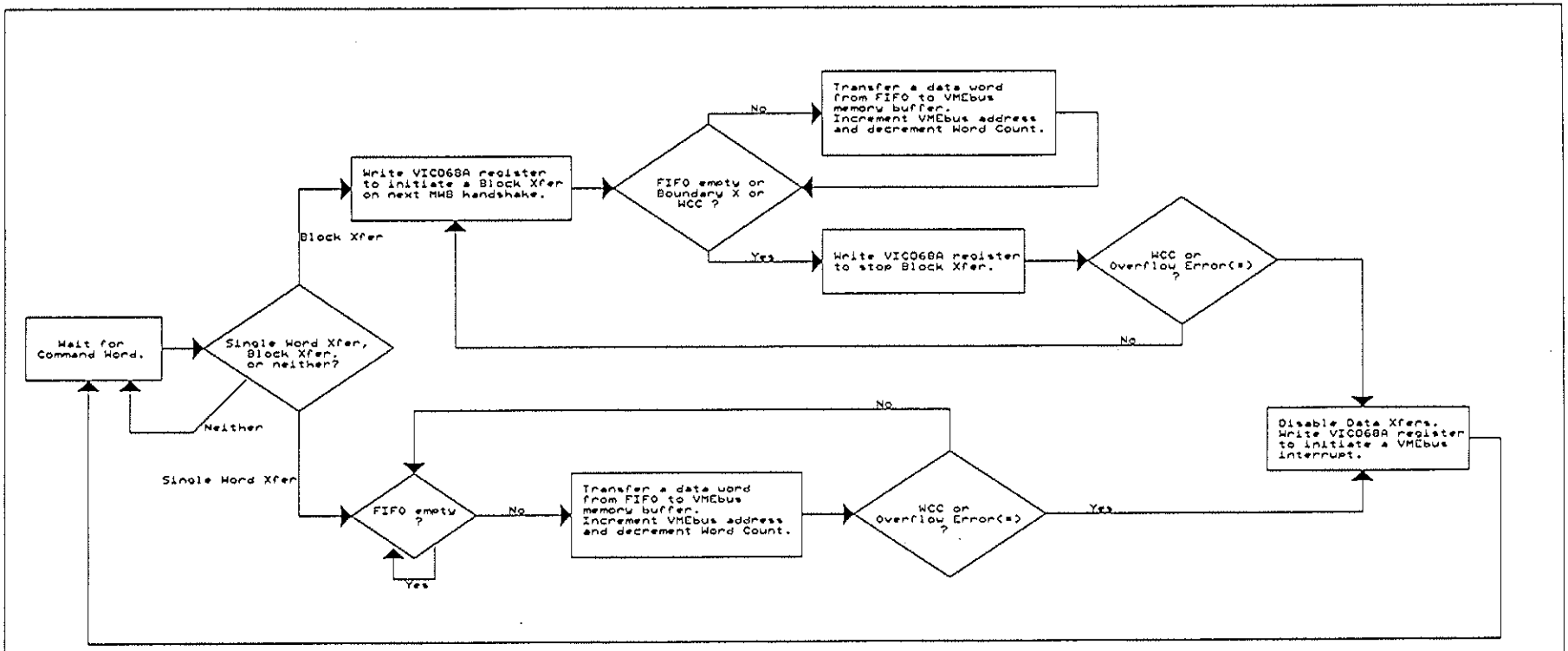
	DATE 2-22-93	*ARECIBO OBSERVATORY* CORNELL UNIVERSITY	SCALE
	APVD. B. SISK		
	BY G.A.SERRANO	SERIAL BIPHASE CONTROL WORD FORMAT	DRAWING

PROTOTYPING
AREA SIGNALS

SLAVE READ AND WRITE



VMEbus SIGNALS



* Overflow Error = FIFO is empty and Latched FIFO Full Flag is active.

FIGURE 6.7.2

ARECIBO OBSERVATORY BY : BILL SISK FILE : VMERI4.SCH		
Title: VME RADAR INTERFACE		
Size: D	Document Number: Flow Chart for VMEbus Master Xfer'S	REV: 0
Date: January 17, 1994	Sheet 1 of 1	

7.0 OPERATIONAL TESTS

The VME RI has several built-in test provisions by which the computer can check its operation. It is suggested that testing be done in the following order.

7.1 Basic Serial Communications Test

The Read Auxiliary Status Word command can be transmitted back to the VME STR (Loopback Test - bit 19) to verify that the serial communications is working correctly.

The multiplexer memory can be written to and read back in the Auxiliary Status Word as a further operational verification.

7.2 Power Supply Test

This test checks the power supplies in the chassis of the VME RI. Clear the error flags by sending a CLEAR (VMEbus data transfers and Test Mode should be disabled). Read the Status Word to ascertain that CLEAR has become inactive. Then read the Auxiliary Status Word over the serial link. Check that bits 8-12 of the Auxiliary Status Word are zeroes. A one indicates an out-of-range voltage and the power supply should be checked for 60Hz ripple.

7.3 Test Mode

The FIFOs can be loaded from the VMEbus with test data to verify the operation of data transfer to the VMEbus, creating a test independent of the other modules of the VME RI. This mode is enabled by the Test Mode option in the Command Word (Table 4.2.2). The FIFOs are loaded with the Soft FIFO Write Command.

In this test, the FIFOs are loaded, and then data transfer to the VMEbus Buffer is enabled. This is not as good a test of the FIFOs as loading the FIFOs from the Packers using the artificial data (section 7.4) since writes and reads to the FIFOs are not occurring 'simultaneously'.

7.4 Packer/Cable/FIFO Test

The Test Pattern Generators provide deterministic artificial data to verify the packing and FIFO operation. When this test is selected (via the Sampler Configuration Word), each digitizer is replaced by a 12-bit binary counter. The counters are zeroed automatically at the start of sampling and are incremented on each sample. Note : the counters are bit reversed, i.e. the LSB or the most rapidly changing counter bit appears as the MSB or sign bit in the data. This avoids rounding off the changing bits when testing the modes with fewer than 12 bits. This test can be performed without an external timing source (RTG or SPS) by using the Software GW sampling mode together with the subcycle mode.

7.5 Digitizer/VME RMUX Test

A sinewave generator is built into the VME RMUX and can be selected instead of the front panel input. When this mode is selected (Enable Sinewave Test in Sampler Configuration Word), all front panel inputs to the VME RMUX are disabled. The sinewave is applied to only one mux channel at a time. The channel is selected in the Sampler Configuration Word. The peak amplitude was chosen so that all the digitizer's bits are exercised.

The test will check the transmission and isolation of all mux channels at 460 KHz, as well as the functionality of the digitizers.

8.0 PAL SOURCE CODE

The PAL Source Code is written for PALASM 4, Version 1.5, available from AMD.