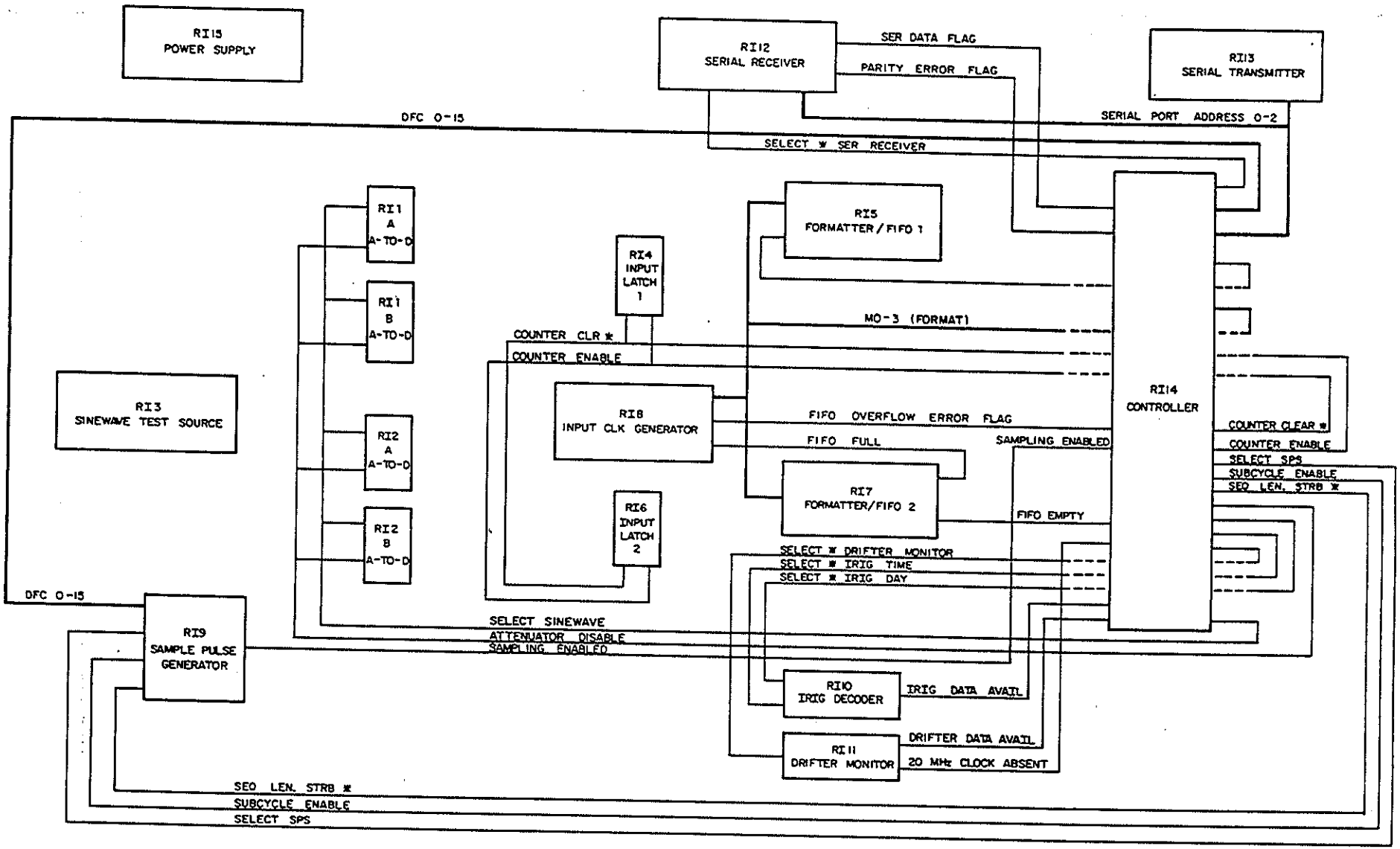
10.0 SCHEMATICS

NOTE:
1. RI1A, RI1B, RI2A, RI2B, RI3 ARE ON INDEPENDENT SUBASSEMBLIES.
2. RI4, RI5, RI6, RI7, RI8, RI10 ARE ON BOTTOM CARD.
3. RI9, RI11, RI12, RI13, RI14 ARE ON UPPER CARD.

REVISIONS	DATE	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	3 - 30 - 90		PAGE 1 of 2
	APPD. JBH / ETR	NAME RADAR INTERFACE BLOCK DIAGRAM	DWN. NO. D721B0180
	BY G.A. SERRANO		

(44)

DWG. NO. D72180280

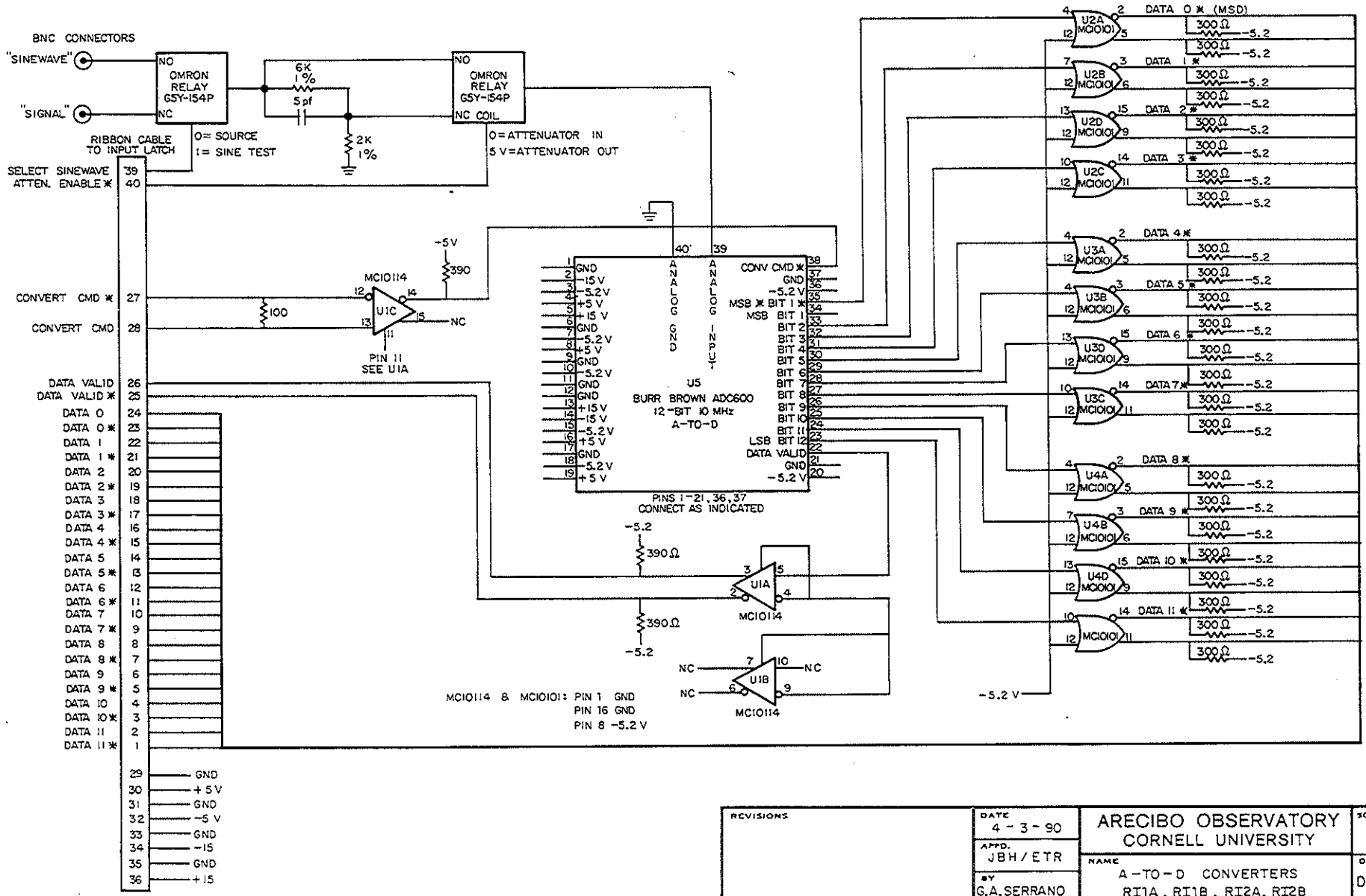


REVISIONS	DATE 4-2-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 2 of 2
	APPD. JBH./ETR	NAME RADAR INTERFACE BLOCK DIAGRAM	DWN. NO. D72180280
	BY G.A. SERRANO		

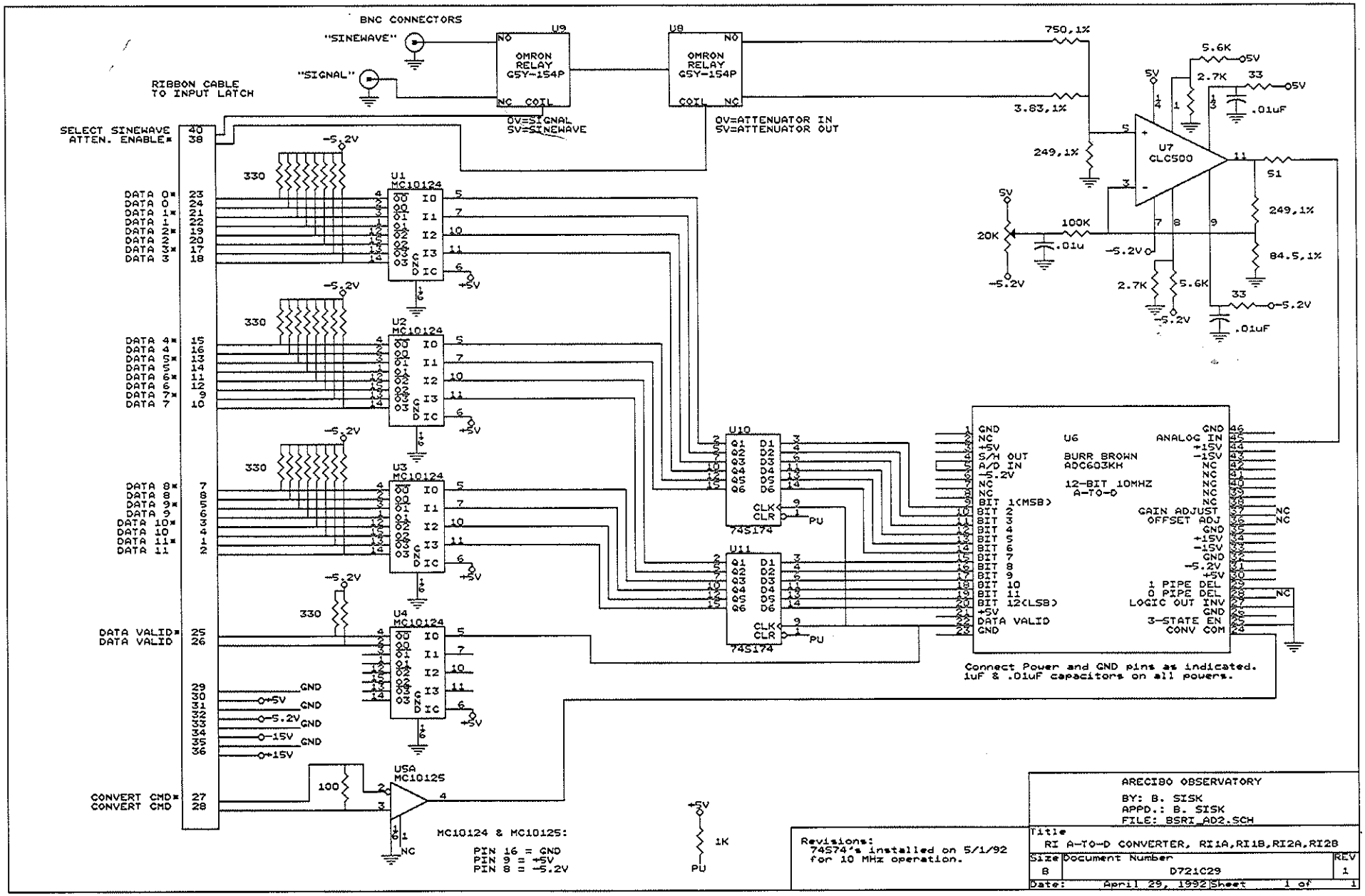
(59)

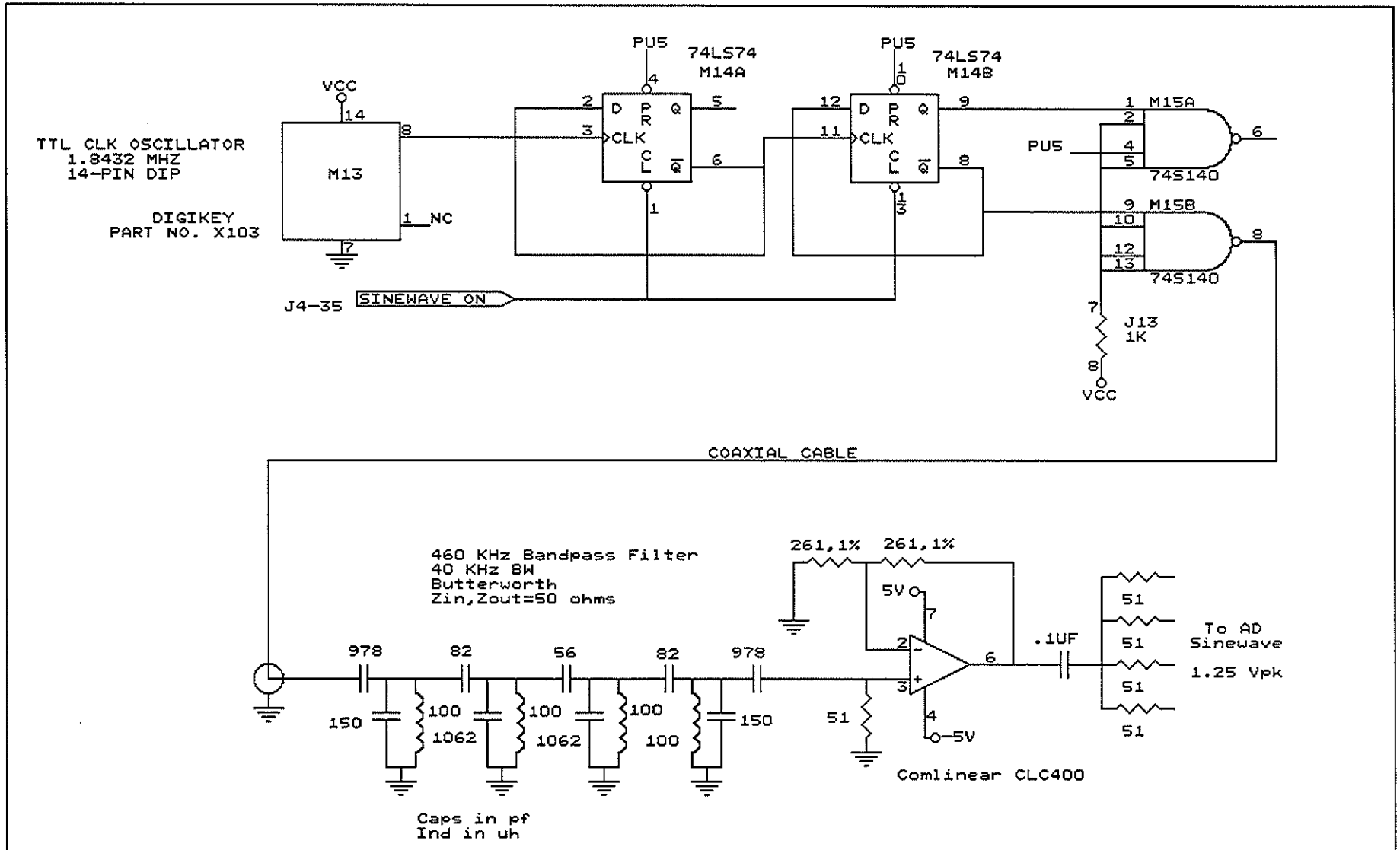
K&E 10 5185 9-77 W3858

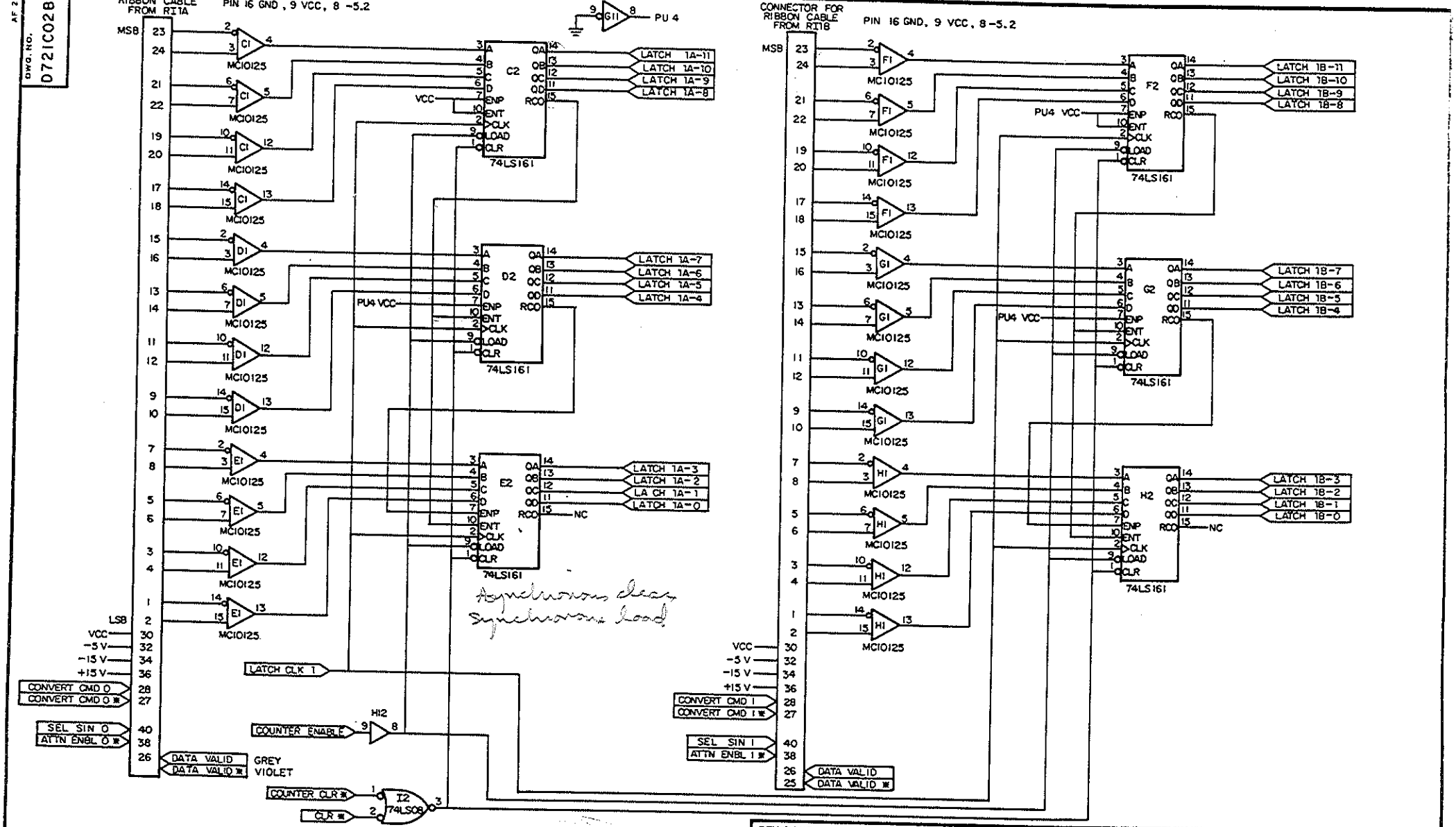
DWG. NO. D721C01B1



REVISIONS	DATE 4-3-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 1 of 2
	APPD. JBH/ETR	NAME A-TO-D CONVERTERS RI1A, RI1B, RI2A, RI2B	DWN. NO. D721C01B1
	BY G.A.SERRANO		


BNC CONNECTORS
"SINEWAVE"
"SIGNAL"
RIBBON CABLE TO INPUT LATCH
OMRON RELAY G5Y-154P
0V=SIGNAL 5V=SINEWAVE
0V=ATTENUATOR IN 5V=ATTENUATOR OUT
SELECT SINEWAVE
ATTEN. ENABLE
DATA 0
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
DATA 8
DATA 9
DATA 10
DATA 11
DATA VALID
CONVERT CMD
MC10124
MC10125
74S174
BURR BROWN ADC603KH
12-BIT 10MHZ A-TO-D
CLC500
750,1%
3.83,1%
249,1%
100K
20K
84.5,1%
5.6K
2.7K
33
.01uF
.01u
100
1K
GND
+5V
-5.2V
-15V
+15V
Connect Power and GND pins as indicated.
1uF & .01uF capacitors on all powers.
MC10124 & MC10125:
PIN 16 = GND
PIN 9 = +5V
PIN 8 = -5.2V
Revisions:
74S74's installed on 5/1/92
for 10 MHz operation.
ARECIBO OBSERVATORY
BY: B. SISK
APPD.: B. SISK
FILE: BSRI_AD2.SCH
Title
RI A-TO-D CONVERTER, RI1A,RI1B,RI2A,RI2B
Size B
Document Number D721C29
REV 1
Date: April 29, 1992
Sheet 1 of 1


TTL CLK OSCILLATOR
1.8432 MHZ
14-PIN DIP
DIGIKEY
PART NO. X103
VCC
M13
NC
PU5
74LS74
M14A
M14B
J4-35
SINEWAVE ON
M15A
M15B
74S140
PU5
J13
1K
COAXIAL CABLE
460 KHz Bandpass Filter
40 KHz BW
Butterworth
Zin,Zout=50 ohms
978
82
56
82
978
150
100
1062
51
261,1%
5V
-5V
.1UF
To AD
Sinewave
1.25 Vpk
Comlinear CLC400
Caps in pf
Ind in uh
On opamp power pins
.01uF
6.8uf
Revisions:
Installed on 11/26/91.
NAIC - ARECIBO OBSERVATORY
BY: B. SISK
APPD.: B. SISK
Title
SINEWAVE TEST SOURCE - RI3
Size
A
Document Number
D721C10
REV
1
Date: November 27, 1991
Sheet 1 of 1

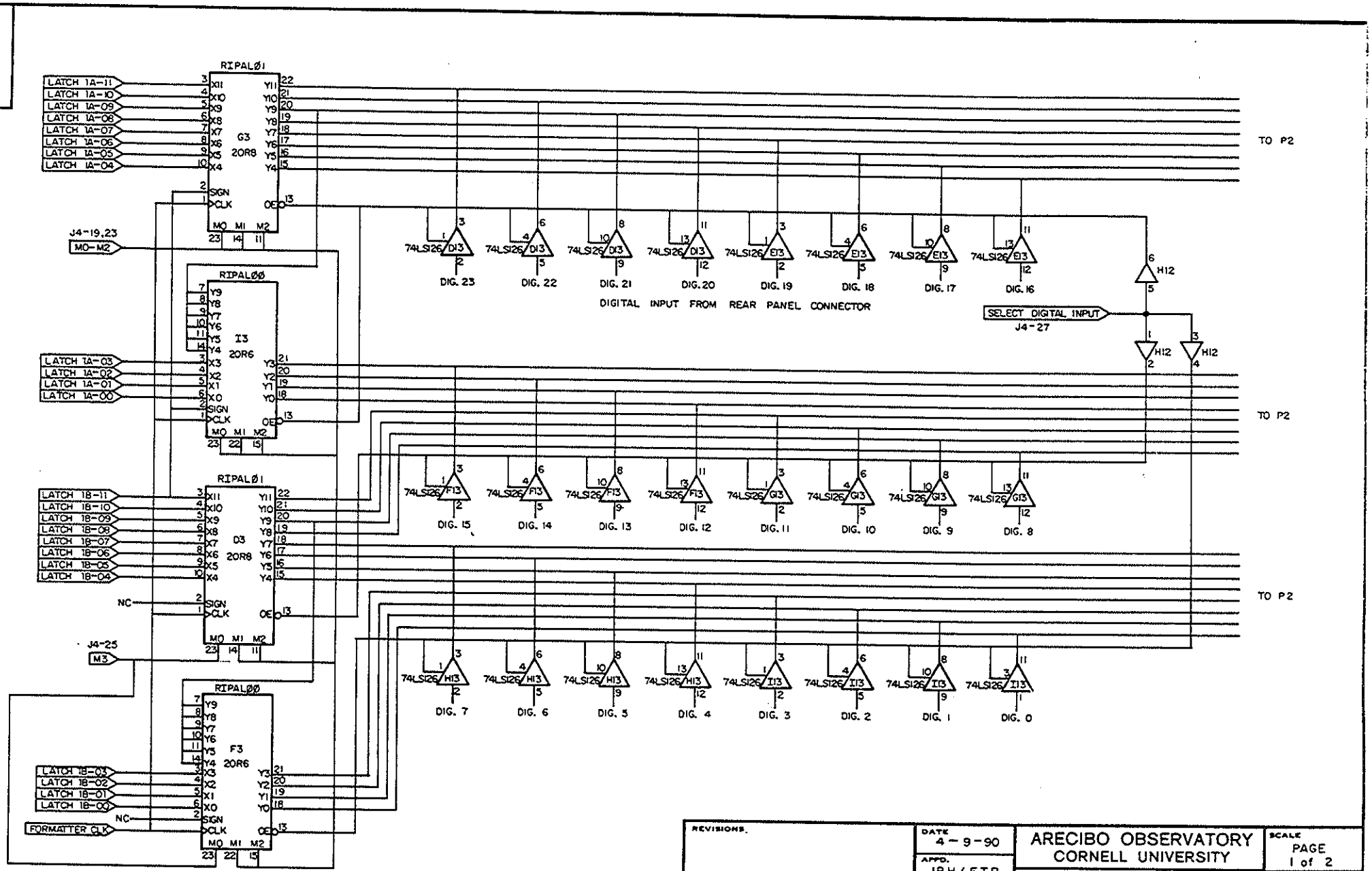


REVISIONS	DATE 4-4-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 1 of 1
	APPD. JBH/ETR	NAME CHANNEL 1 INPUT LATCH / TEST PATTERN GEN. RI4	DWG. NO. D721C02B0
	BY G.A.SERRANO		

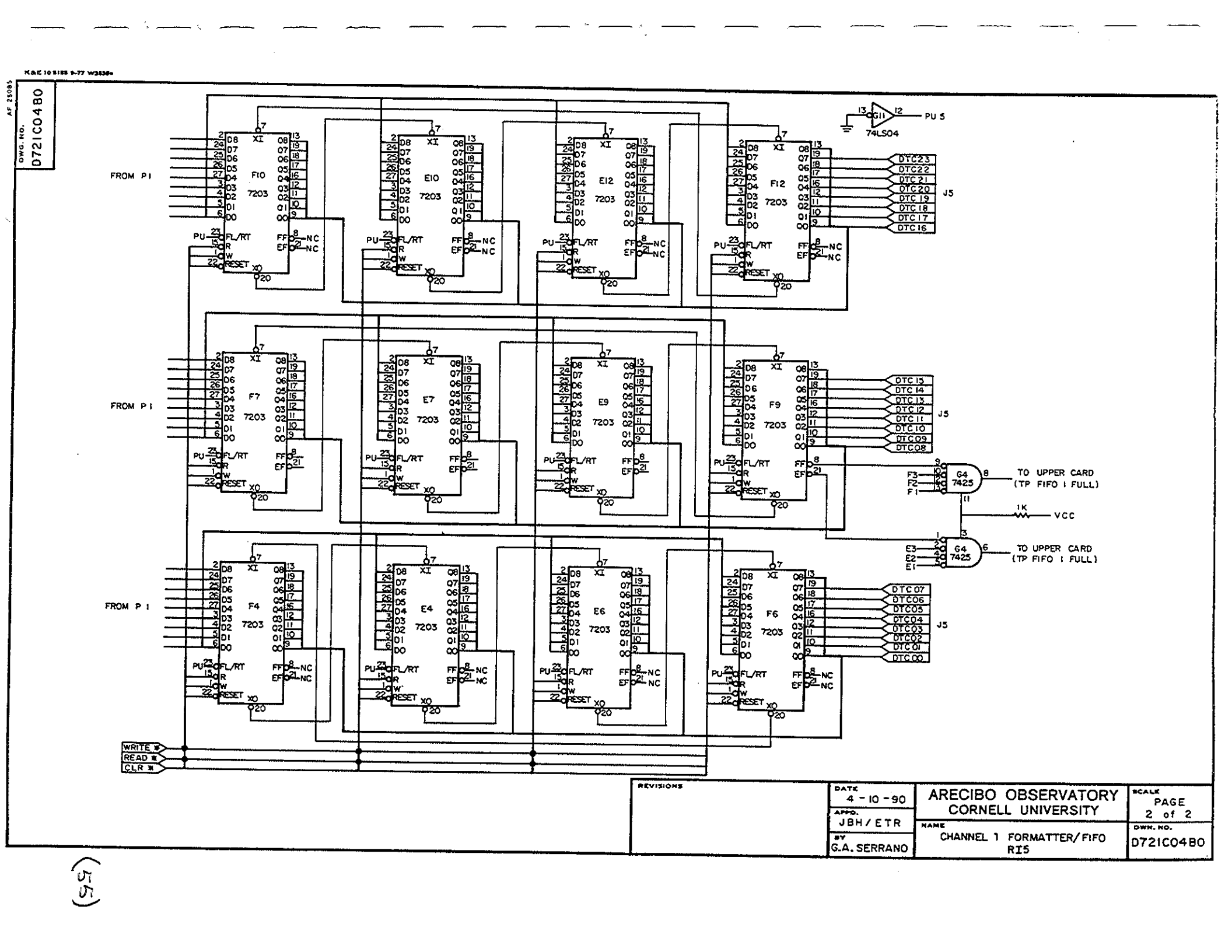
DWG. NO. D721C02B0

AF 25065

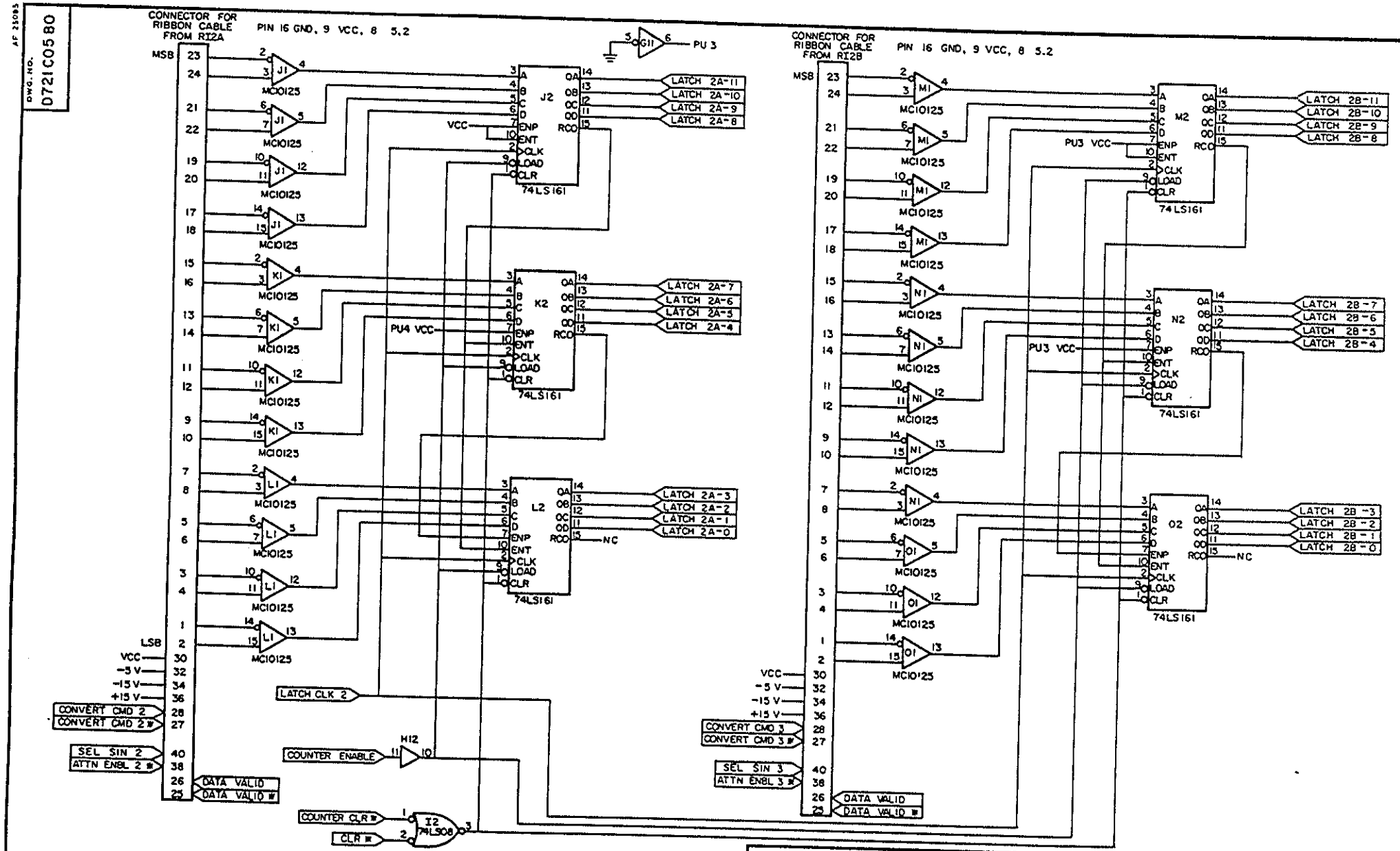
(55)


DWG. NO. D721C0380
RIPALØ1
RIPALØØ
RIPALØ1
RIPALØØ
G3 20R8
I3 20R6
D3 20R8
F3 20R6
LATCH 1A-11
LATCH 1A-10
LATCH 1A-09
LATCH 1A-08
LATCH 1A-07
LATCH 1A-06
LATCH 1A-05
LATCH 1A-04
LATCH 1A-03
LATCH 1A-02
LATCH 1A-01
LATCH 1A-00
LATCH 1B-11
LATCH 1B-10
LATCH 1B-09
LATCH 1B-08
LATCH 1B-07
LATCH 1B-06
LATCH 1B-05
LATCH 1B-04
LATCH 1B-03
LATCH 1B-02
LATCH 1B-01
LATCH 1B-00
J4-19,23
M0-M2
J4-25
M3
NC
FORMATTER CLK
SIGN
CLK
OE
M0 M1 M2
74LS126 D13
74LS126 E13
74LS126 F13
74LS126 G13
74LS126 H13
74LS126 I13
DIG. 23
DIG. 22
DIG. 21
DIG. 20
DIG. 19
DIG. 18
DIG. 17
DIG. 16
DIG. 15
DIG. 14
DIG. 13
DIG. 12
DIG. 11
DIG. 10
DIG. 9
DIG. 8
DIG. 7
DIG. 6
DIG. 5
DIG. 4
DIG. 3
DIG. 2
DIG. 1
DIG. 0
DIGITAL INPUT FROM REAR PANEL CONNECTOR
SELECT DIGITAL INPUT
J4-27
H12
TO P2
TO P2
TO P2
REVISIONS.
DATE 4-9-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME CHANNEL 1 FORMATTER/FIFO RI5
SCALE PAGE 1 of 2
DWN. NO. D721C03B0

(54)

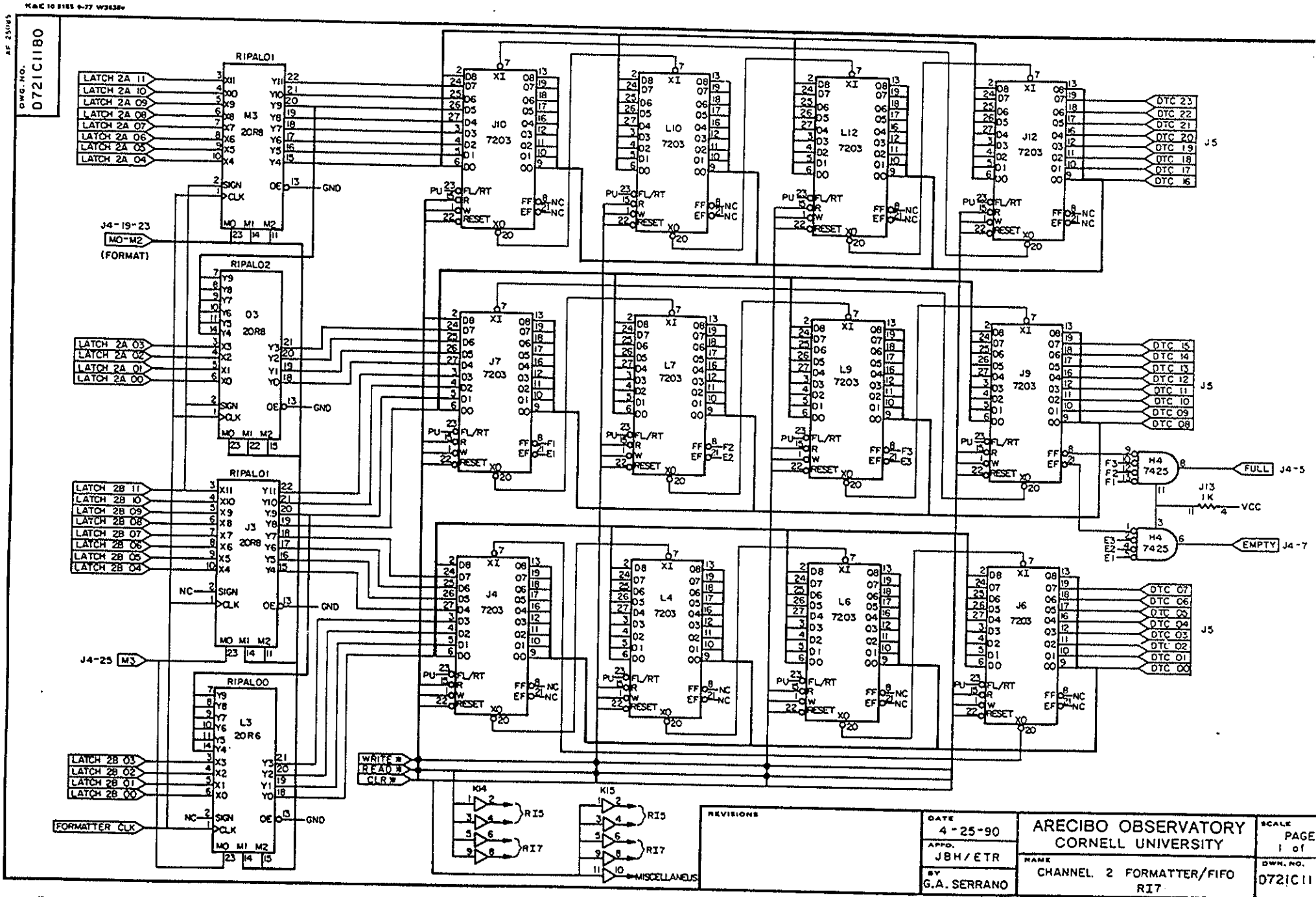

DWG. NO. D721C04B0
FROM P1
F10
E10
E12
F12
J5
DTC23
DTC22
DTC21
DTC20
DTC19
DTC18
DTC17
DTC16
74LS04
PU 5
FROM P1
F7
E7
E9
F9
J5
DTC15
DTC14
DTC13
DTC12
DTC11
DTC10
DTC09
DTC08
G4 7425
TO UPPER CARD (TP FIFO 1 FULL)
1K
VCC
G4 7425
TO UPPER CARD (TP FIFO 1 FULL)
FROM P1
F4
E4
E6
F6
J5
DTC07
DTC06
DTC05
DTC04
DTC03
DTC02
DTC01
DTC00
WRITE
READ
CLR
REVISIONS
DATE 4 - 10 - 90
APPD. JBH / ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME CHANNEL 1 FORMATTER/FIFO RI5
SCALE PAGE 2 of 2
DWN. NO. D721C04B0

(55)

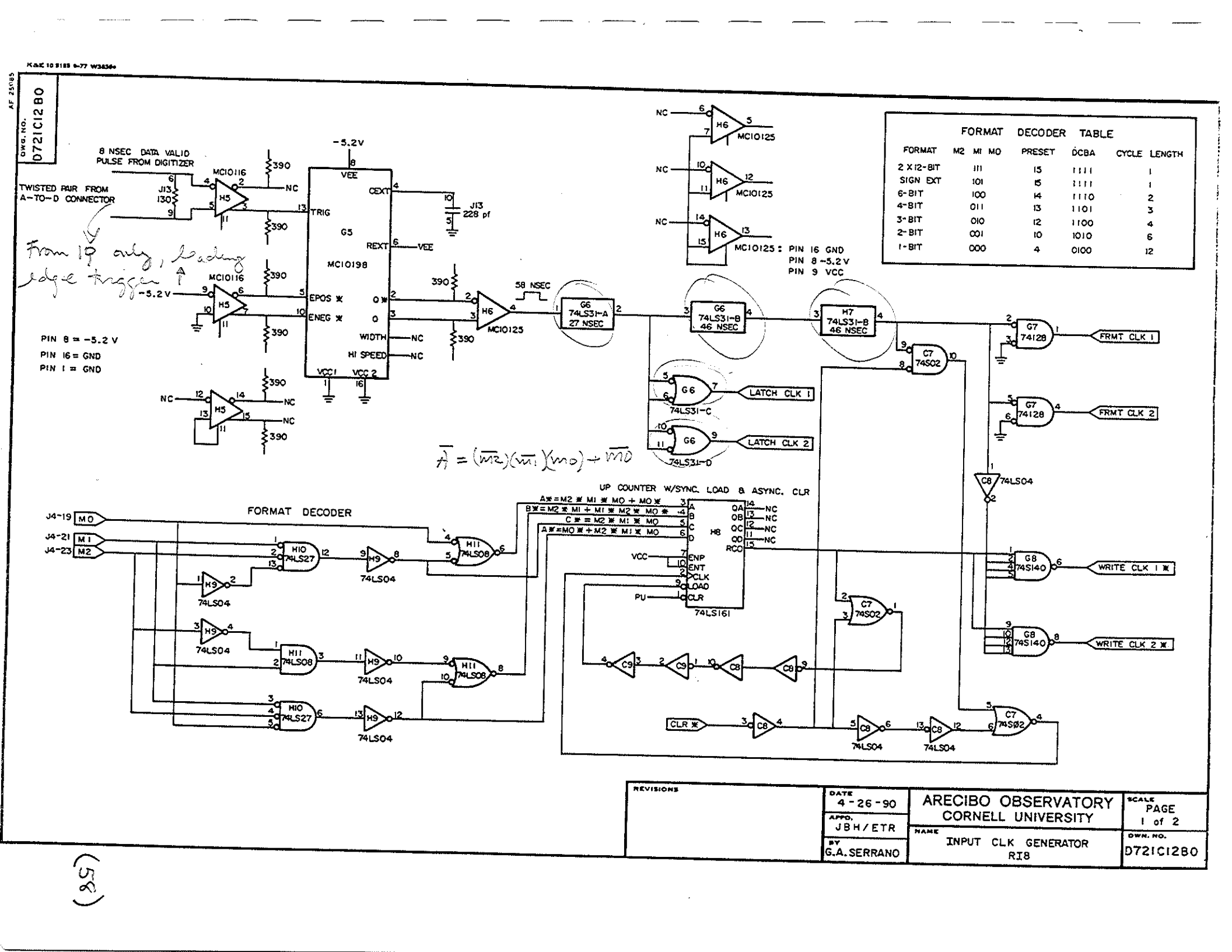


REVISIONS	DATE 4 - 12 - 90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 1 of
	APPD. JBH / ETR	NAME CHANNEL 2 INPUT LATCH/ TEST PATTERN GEN. RI6	DWN. NO. D721C05
	BY G.A. SERRANO		

(56)


DWG. NO. 0721C1180
RIPALO1
RIPALO2
RIPALO1
RIPALOO
M3 20R8
03 20R8
J3 20R8
L3 20R6
LATCH 2A 11
LATCH 2A 10
LATCH 2A 09
LATCH 2A 08
LATCH 2A 07
LATCH 2A 06
LATCH 2A 05
LATCH 2A 04
LATCH 2A 03
LATCH 2A 02
LATCH 2A 01
LATCH 2A 00
LATCH 2B 11
LATCH 2B 10
LATCH 2B 09
LATCH 2B 08
LATCH 2B 07
LATCH 2B 06
LATCH 2B 05
LATCH 2B 04
LATCH 2B 03
LATCH 2B 02
LATCH 2B 01
LATCH 2B 00
J4-19-23
M0-M2
(FORMAT)
J4-25 M3
FORMATTER CLK
WRITE*
READ*
CLR*
J10 7203
L10 7203
L12 7203
J12 7203
J7 7203
L7 7203
L9 7203
J9 7203
J4 7203
L4 7203
L6 7203
J6 7203
DTC 23
DTC 22
DTC 21
DTC 20
DTC 19
DTC 18
DTC 17
DTC 16
DTC 15
DTC 14
DTC 13
DTC 12
DTC 11
DTC 10
DTC 09
DTC 08
DTC 07
DTC 06
DTC 05
DTC 04
DTC 03
DTC 02
DTC 01
DTC 00
H4 7425
FULL J4-5
EMPTY J4-7
J13 1K
VCC
KI4
KI5
RI5
RI7
MISCELLANEUS
GND
REVISIONS
DATE 4-25-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME CHANNEL 2 FORMATTER/FIFO RI7
SCALE
PAGE 1 of
DWN. NO. 0721C11

(57)



FORMAT DECODER TABLE

FORMAT	M2 MI MO	PRESET	DCBA	CYCLE LENGTH
2 X 12-BIT	111	15	1111	1
SIGN EXT	101	15	1111	1
6-BIT	100	14	1110	2
4-BIT	011	13	1101	3
3-BIT	010	12	1100	4
2-BIT	001	10	1010	6
1-BIT	000	4	0100	12

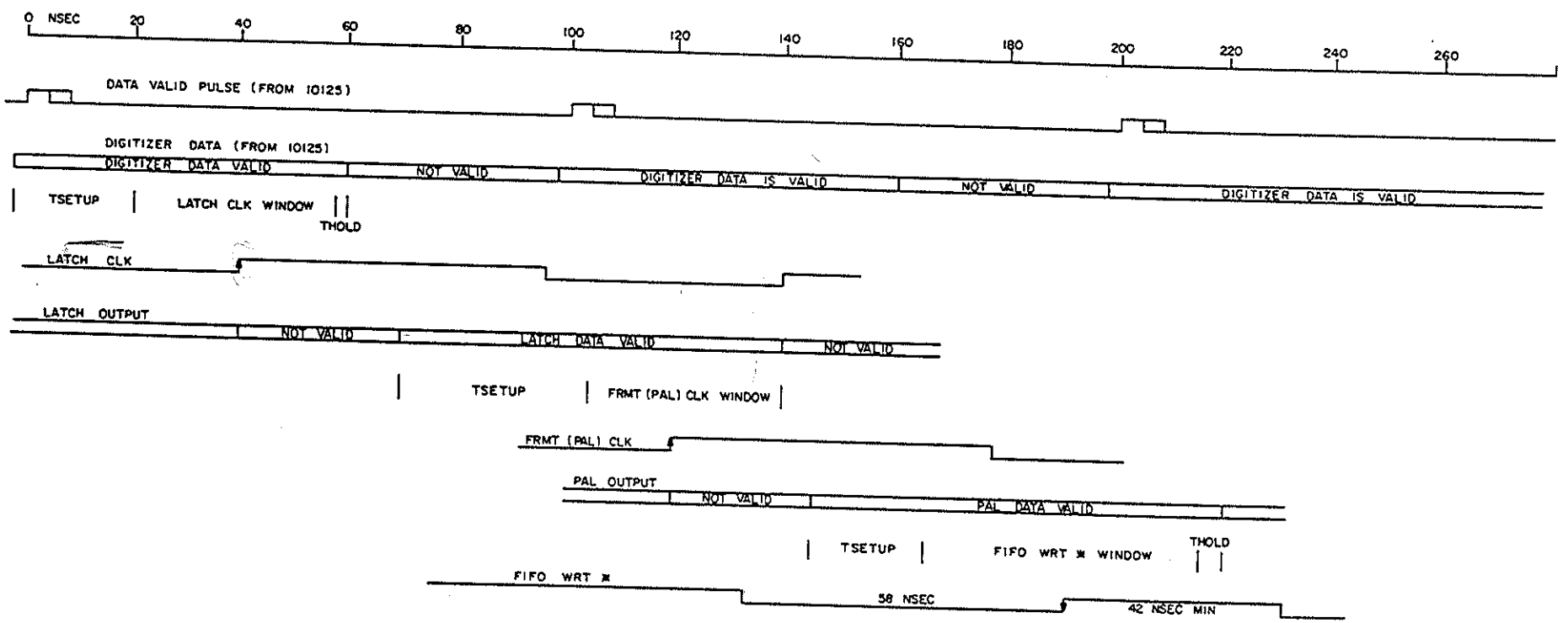
From 19 only, leading edge trigger

$\overline{A} = (\overline{M2})(\overline{M1})(M0) + \overline{M0}$

REVISIONS	DATE 4-26-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 1 of 2
	APPD. JBH/ETR	NAME INPUT CLK GENERATOR RI8	DWG. NO. D721C1280
	BY G.A. SERRANO		

(85)

DWG. NO. D721T0180



(10 MHz SAMPLING RATE)

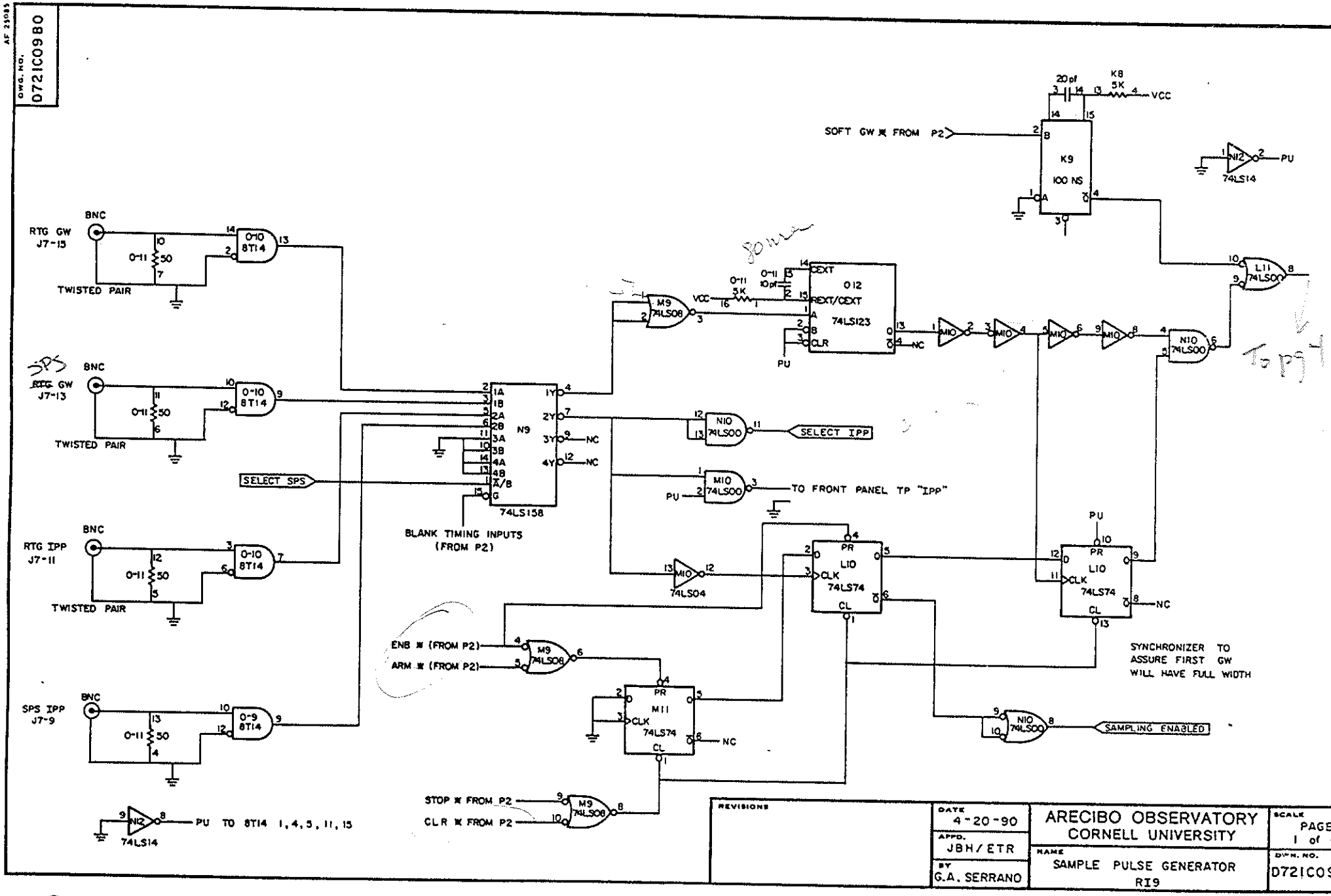
	MIN SETUP	THIS DESIGN	MIN HOLD	THIS DESIGN	DEVICE PROP. TIME	MIN CLK WITH HIGH	THIS DESIGN	MIN CLK WIDTH LOW	THIS DESIGN
LATCH LS161A	20 NSEC	45	2	20	27	25	58	16	42
FORMATTER PAL20R8A-2 PAL20R6A-2	55	52	0	18	25	25	58	37	42
FIFO DALLAS SEMICONDUCTOR DS2012-65	20	33	5	42		15 (TWR)	42	50 (TWPW)	58

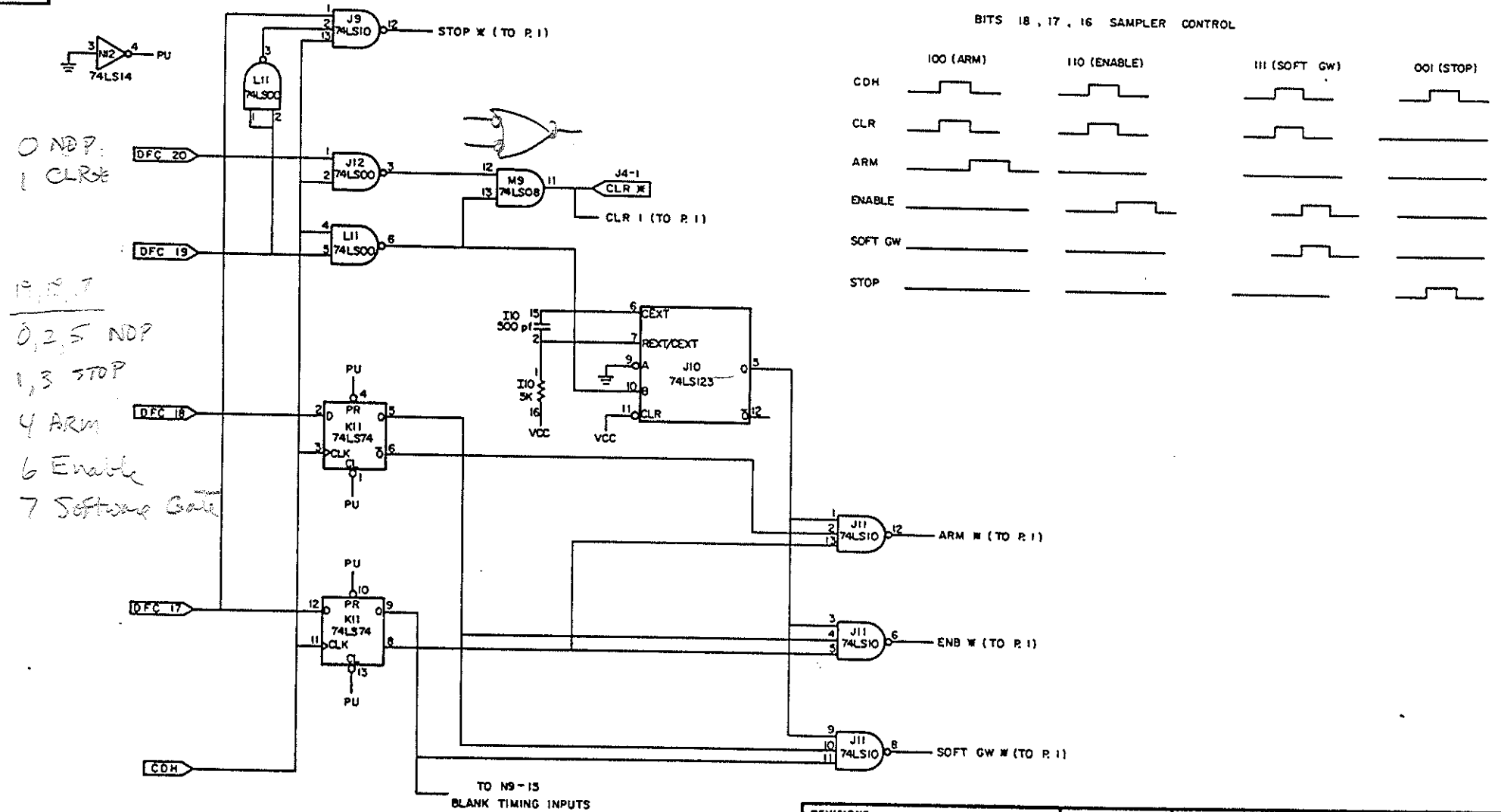
NOTE: TIMING SHOWN FOR MAXIMUM SAMPLING RATE (10 MHz)

NOTE: FIFO WRITE INITIATED BY FALLING EDGE OF ITS CLOCK BUT SET UP AND HOLD TIMES ARE W.R.T RISING EDGE.

REVISIONS	DATE	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	4-12-90		2 of
	APPD. JBH/ETR	NAME INPUT CLK GENERATOR RI8	DWN. NO. D721T0
	BY G.A. SERRANO		

(59)


DWG. NO. D721C0980
SOFT GW ※ FROM P2
K8 5K
20pf
VCC
K9 100 NS
74LS14
RTG GW J7-15
BNC
TWISTED PAIR
SPS RTG GW J7-13
RTG IPP J7-11
SPS IPP J7-9
0-10 8T14
0-9 8T14
0-11 50
SELECT SPS
BLANK TIMING INPUTS (FROM P2)
74LS158
M9 74LS08
0-11 5K
0-11 10pf
012 74LS123
CEXT
REXT/CEXT
CLR
PU
L11 74LS00
M10 74LS00
N10 74LS00
SELECT IPP
TO FRONT PANEL TP "IPP"
74LS04
M11 74LS74
PR
CLK
CL
NC
ENB ※ (FROM P2)
ARM ※ (FROM P2)
SAMPLING ENABLED
SYNCHRONIZER TO ASSURE FIRST GW WILL HAVE FULL WIDTH
STOP ※ FROM P2
CLR ※ FROM P2
PU TO 8T14 1,4,5,11,15
REVISIONS
DATE 4-20-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME SAMPLE PULSE GENERATOR RI9
SCALE
PAGE 1 of
DWG. NO. D721C0



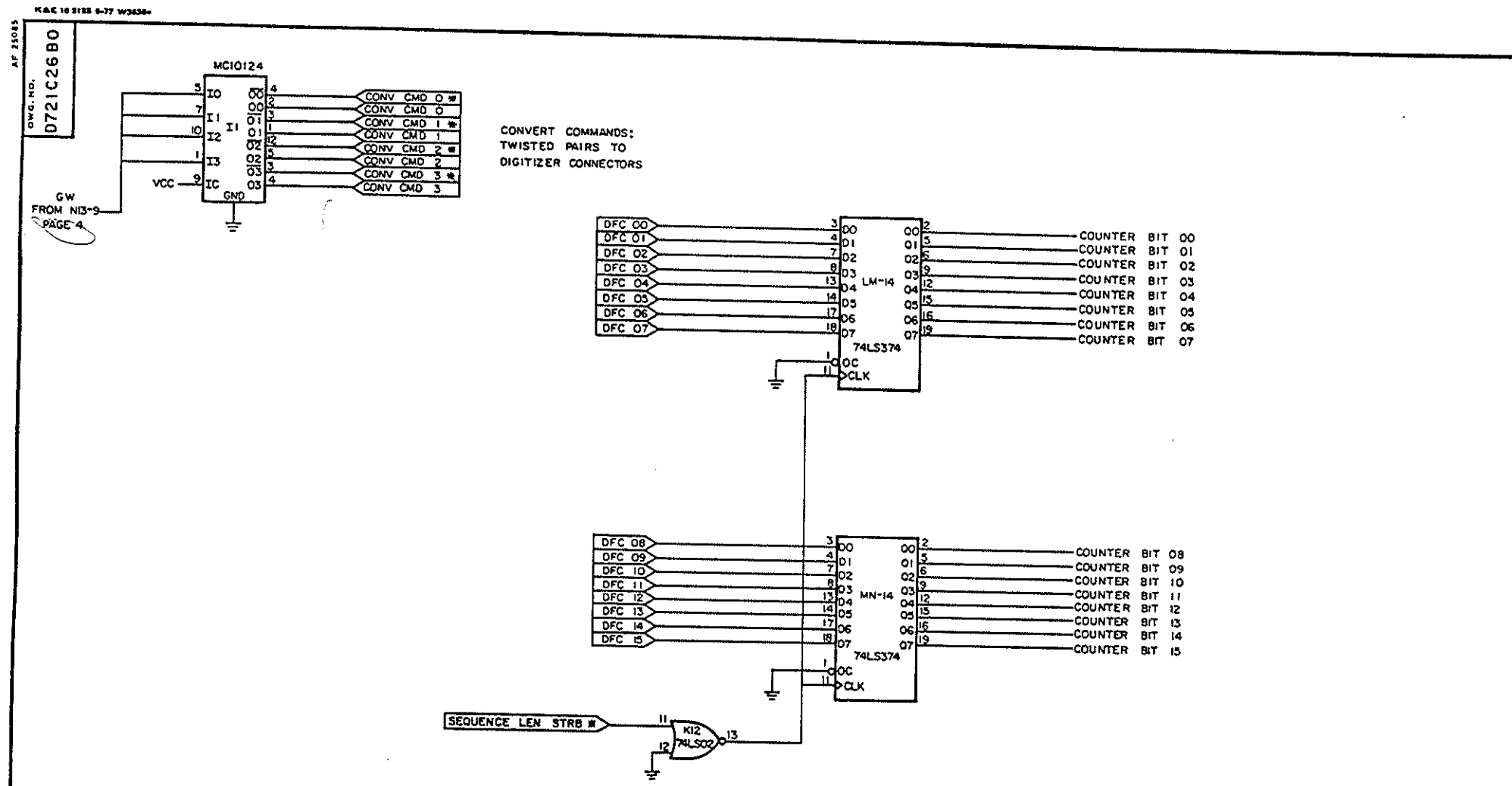
0 NDP
1 CLR✻

19, 18, 17

0, 2, 5 NDP
1, 3 STOP
4 ARM
6 Enable
7 Software Gate

(19)

REVISIONS	DATE 4-12-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAG 2 of
	APPD. JBH/ETR	NAME SAMPLE PULSE GENERATOR RI9	DWN. NO. D721C
	BY G.A. SERRANO		

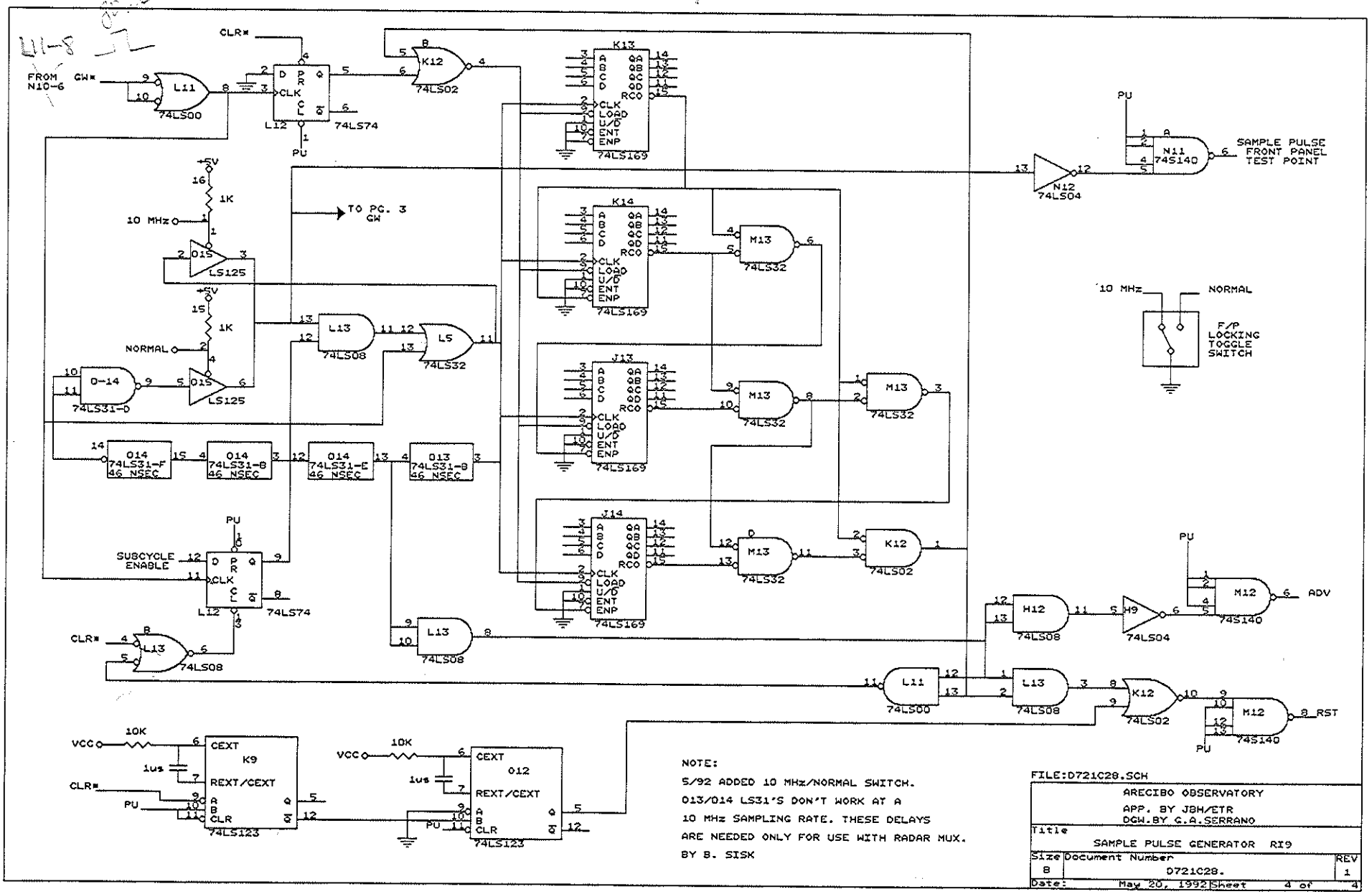


REVISIONS	DATE 5-18-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 3 of
	APPD. JBH/ETR	NAME SAMPLE PULSE GENERATOR RI9	DWG. NO. D721C26
	BY G.A. SERRANO		

(62)

Multiplexer limited to 5 MHz Sampling Rate - because of this opt.

LS169 Synch Load



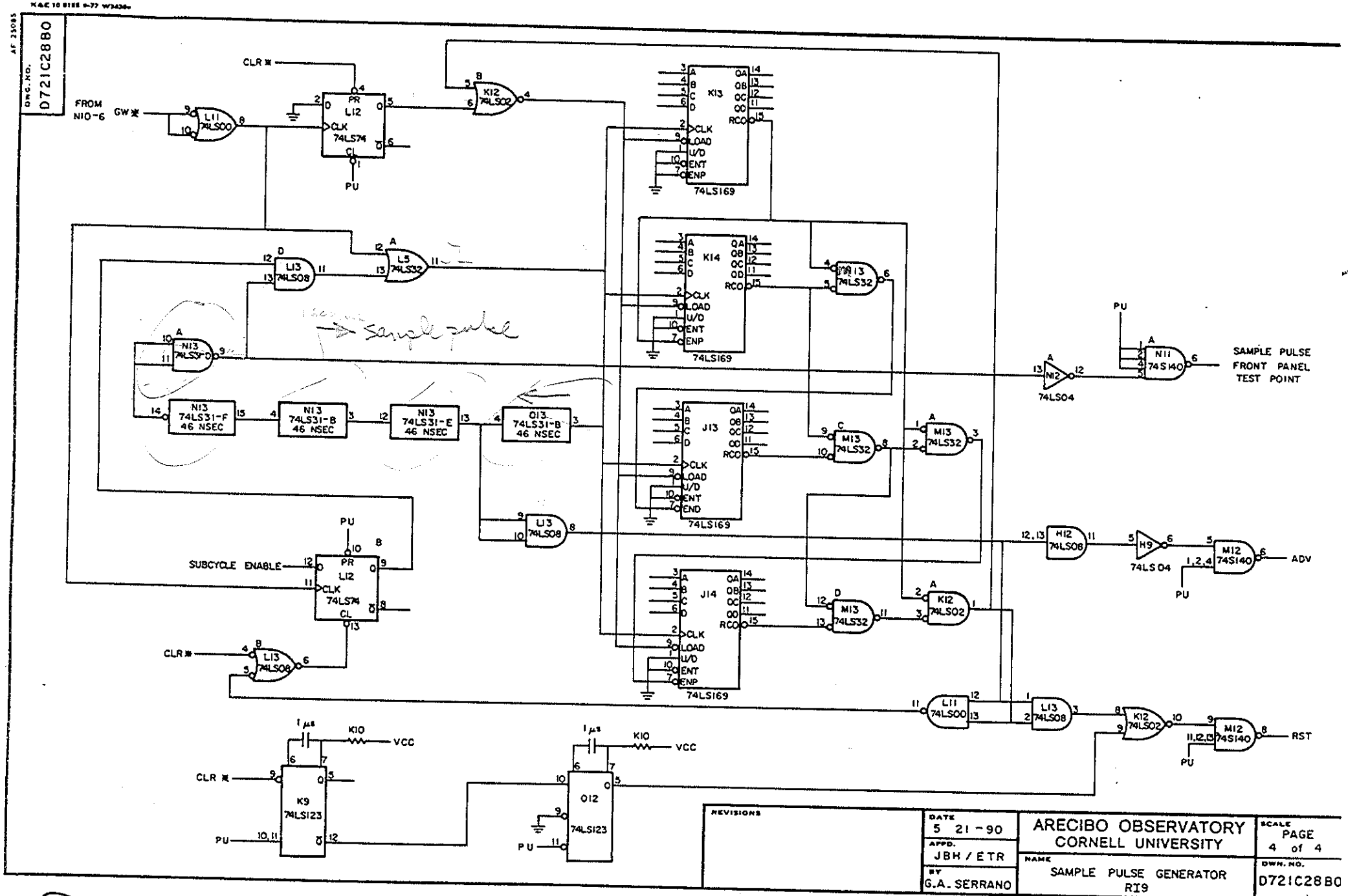
NOTE:
5/92 ADDED 10 MHz/NORMAL SWITCH.
013/014 LS31'S DON'T WORK AT A
10 MHz SAMPLING RATE. THESE DELAYS
ARE NEEDED ONLY FOR USE WITH RADAR MUX.
BY B. SISK

FILE:D721C28.SCH

ARECIBO OBSERVATORY
APP. BY JBH/ETR
DGW.BY G.A.SERRANO

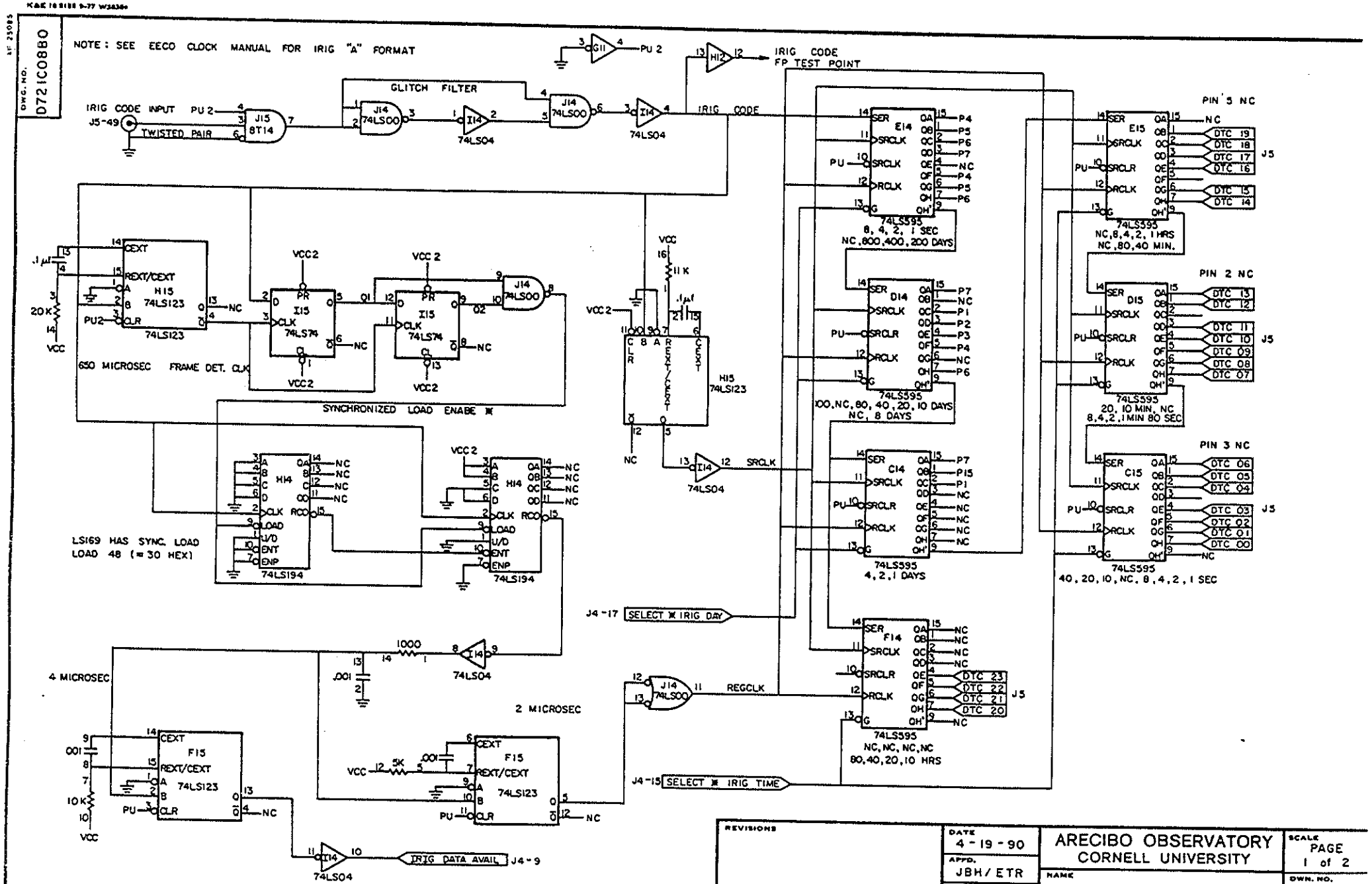
Title: SAMPLE PULSE GENERATOR RI9

Size	Document Number	REV
B	D721C28.	1
Date: May 20, 1992	Sheet 4 of 4	



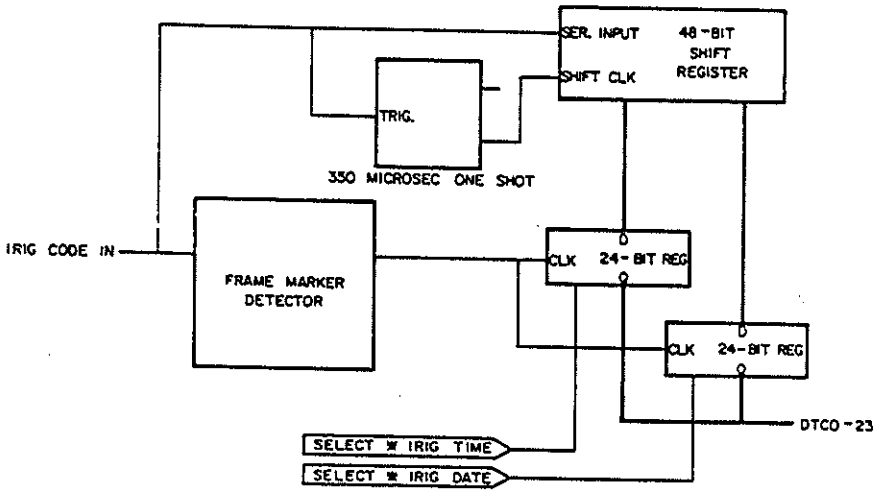
(63)

OLD DRAWING

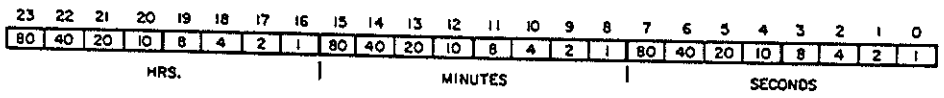

D721C0880
NOTE : SEE EECO CLOCK MANUAL FOR IRIG "A" FORMAT
IRIG CODE INPUT J5-49
TWISTED PAIR
PU 2
GLITCH FILTER
74LS04
74LS00
IRIG CODE
IRIG CODE FP TEST POINT
74LS123
74LS74
650 MICROSEC FRAME DET. CLK
SYNCHRONIZED LOAD ENABLE
74LS194
LS169 HAS SYNC. LOAD
LOAD 48 (= 30 HEX)
4 MICROSEC
2 MICROSEC
SRCLK
REGCLK
74LS595
8, 4, 2, 1 SEC
NC, 800, 400, 200 DAYS
100, NC, 80, 40, 20, 10 DAYS
NC, 8 DAYS
4, 2, 1 DAYS
NC, NC, NC, NC
80, 40, 20, 10 HRS
PIN 5 NC
NC, 8, 4, 2, 1 HRS
NC, 80, 40 MIN.
PIN 2 NC
20, 10 MIN, NC
8, 4, 2, 1 MIN 80 SEC
PIN 3 NC
40, 20, 10, NC, 8, 4, 2, 1 SEC
J4-17 SELECT IRIG DAY
J4-15 SELECT IRIG TIME
IRIG DATA AVAIL J4-9
REVISIONS
DATE 4-19-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME IRIG DECODER RIIO
SCALE PAGE 1 of 2
DWN. NO. D721C088

(64)

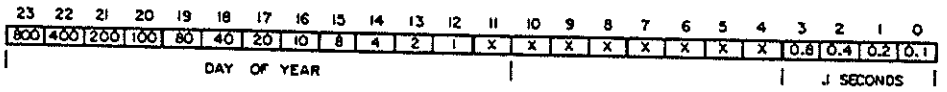
DWG. NO. D721T0280



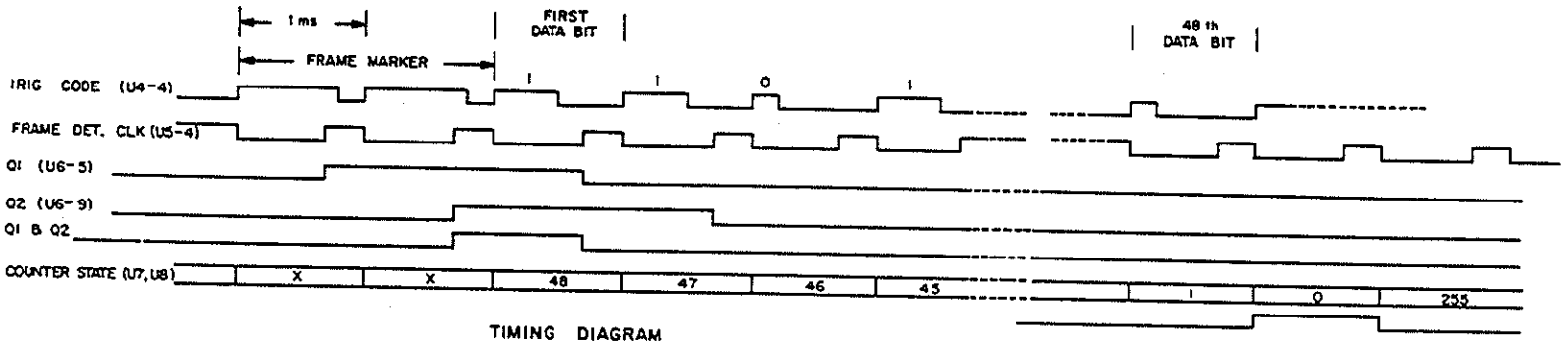
BLOCK DIAGRAM



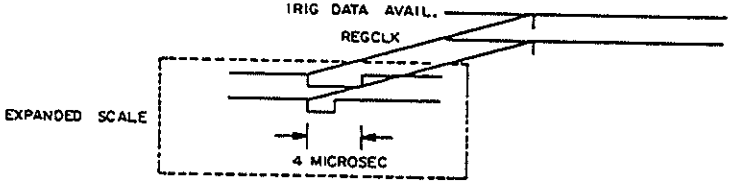
IRIG TIME WORD FORMAT



IRIG DAY WORD FORMAT

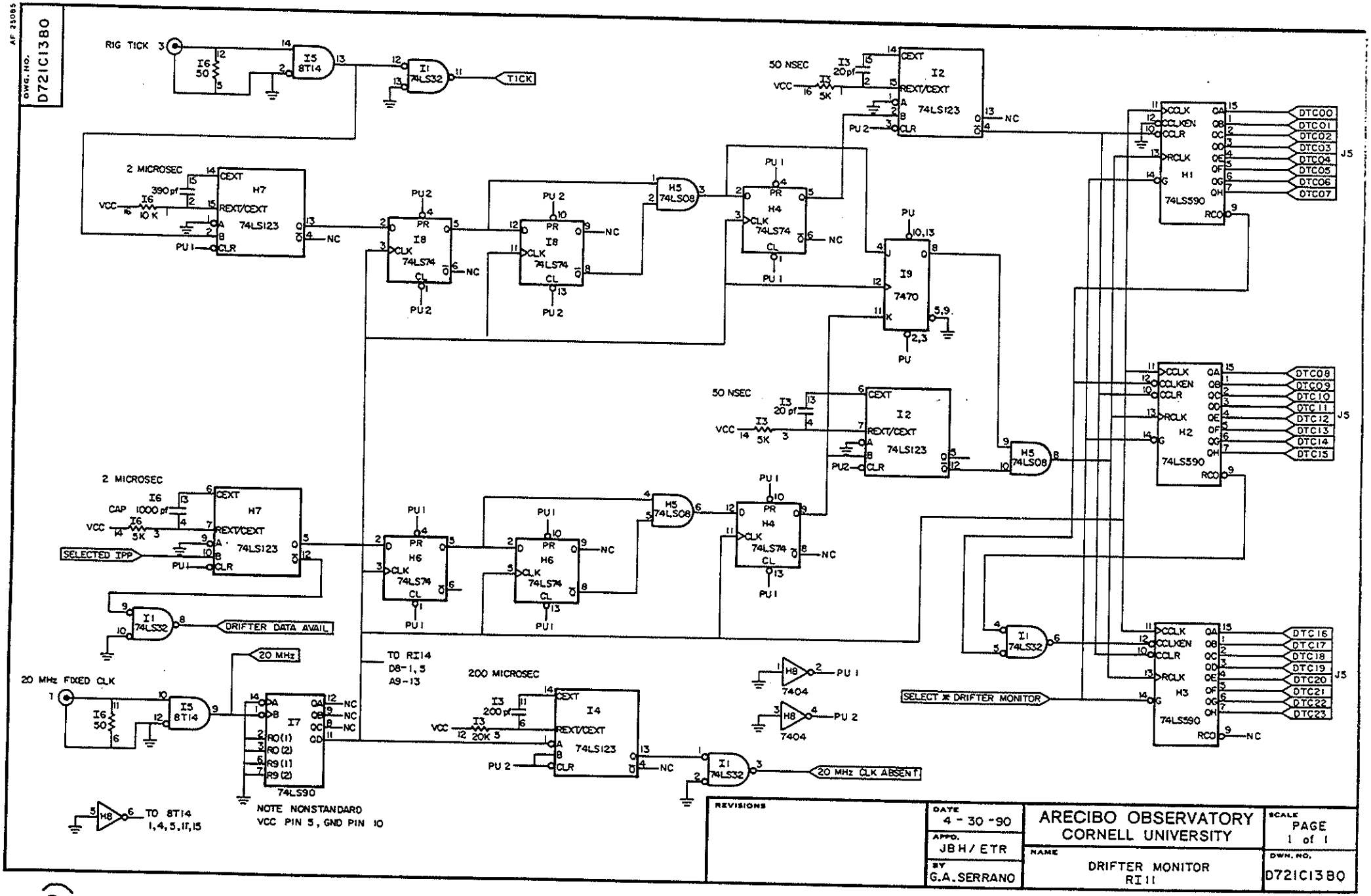


TIMING DIAGRAM

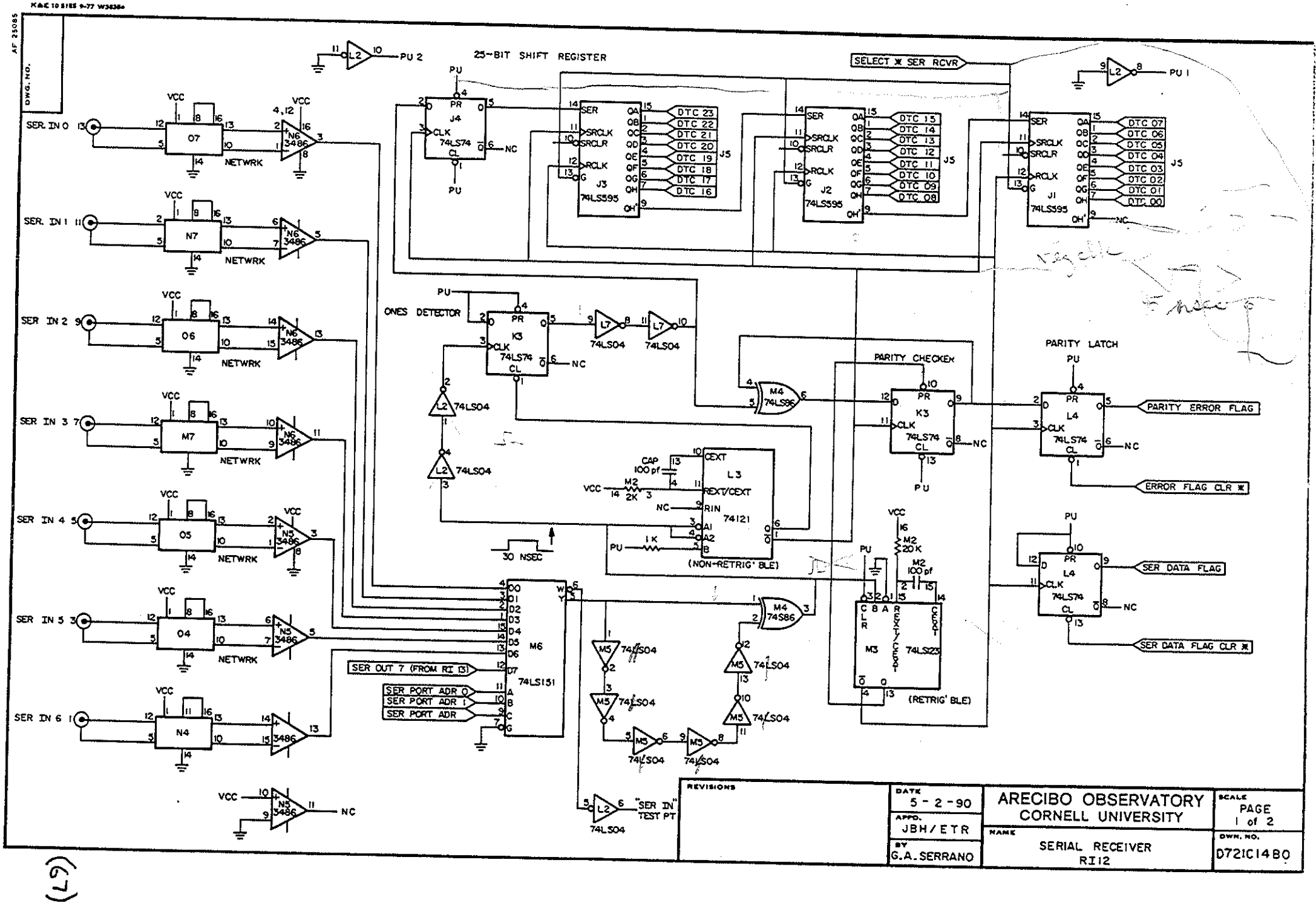


REVISIONS	DATE 4-27-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 2 of 2
	APPD. JBH / ETR	NAME IRIG DECODER RIIO	DWG. NO. D721T0280
	BY G.A.SERRANO		

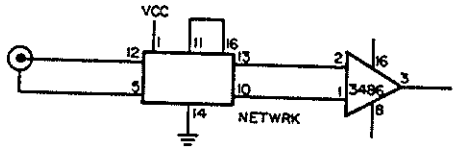
(65)


DWG. NO. D721C1380
RIG TICK
TICK
50 NSEC
2 MICROSEC
390 pf
10 K
74LS123
74LS74
74LS08
74LS32
74LS590
7470
7404
DTC00
DTC01
DTC02
DTC03
DTC04
DTC05
DTC06
DTC07
DTC08
DTC09
DTC10
DTC11
DTC12
DTC13
DTC14
DTC15
DTC16
DTC17
DTC18
DTC19
DTC20
DTC21
DTC22
DTC23
SELECTED TPP
DRIFTER DATA AVAIL
20 MHz
20 MHz FIXED CLK
TO RI14
D8-1,5
A9-13
200 MICROSEC
20 MHz CLK ABSENT
SELECT * DRIFTER MONITOR
NOTE NONSTANDARD
VCC PIN 5, GND PIN 10
TO 8T14
1,4,5,11,15
REVISIONS
DATE 4-30-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME DRIFTER MONITOR RI11
SCALE PAGE 1 of 1
DWN. NO. D721C1380

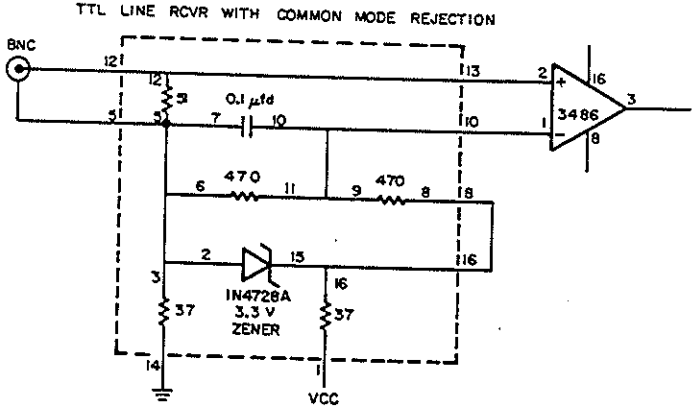
(99)


AF 25085
DWG. NO.
25-BIT SHIFT REGISTER
SELECT * SER RCVR
PU 2
PU 1
SER. IN 0
SER. IN 1
SER. IN 2
SER. IN 3
SER. IN 4
SER. IN 5
SER. IN 6
NETWRK
74LS595
74LS574
ONES DETECTOR
PARITY CHECKER
PARITY LATCH
PARITY ERROR FLAG
ERROR FLAG CLR *
SER DATA FLAG
SER DATA FLAG CLR *
(NON-RETRIG' BLE)
(RETRIG' BLE)
74121
74LS123
74LS151
74LS04
74LS86
30 NSEC
SER OUT 7 (FROM RI 13)
SER PORT ADR 0
SER PORT ADR 1
SER PORT ADR
"SER IN" TEST PT
REVISIONS
DATE 5 - 2 - 90
APPD. JBH / ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME SERIAL RECEIVER RI12
SCALE PAGE 1 of 2
DWN. NO. D721C1480

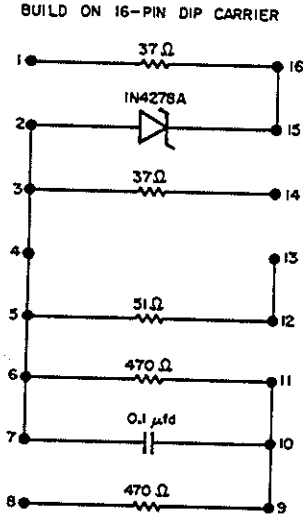
DWG. NO. D721C1580



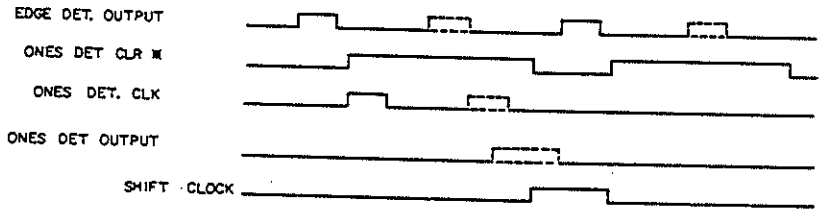
A. SCHEMATIC USAGE



B. DETAILED SCHEMATIC

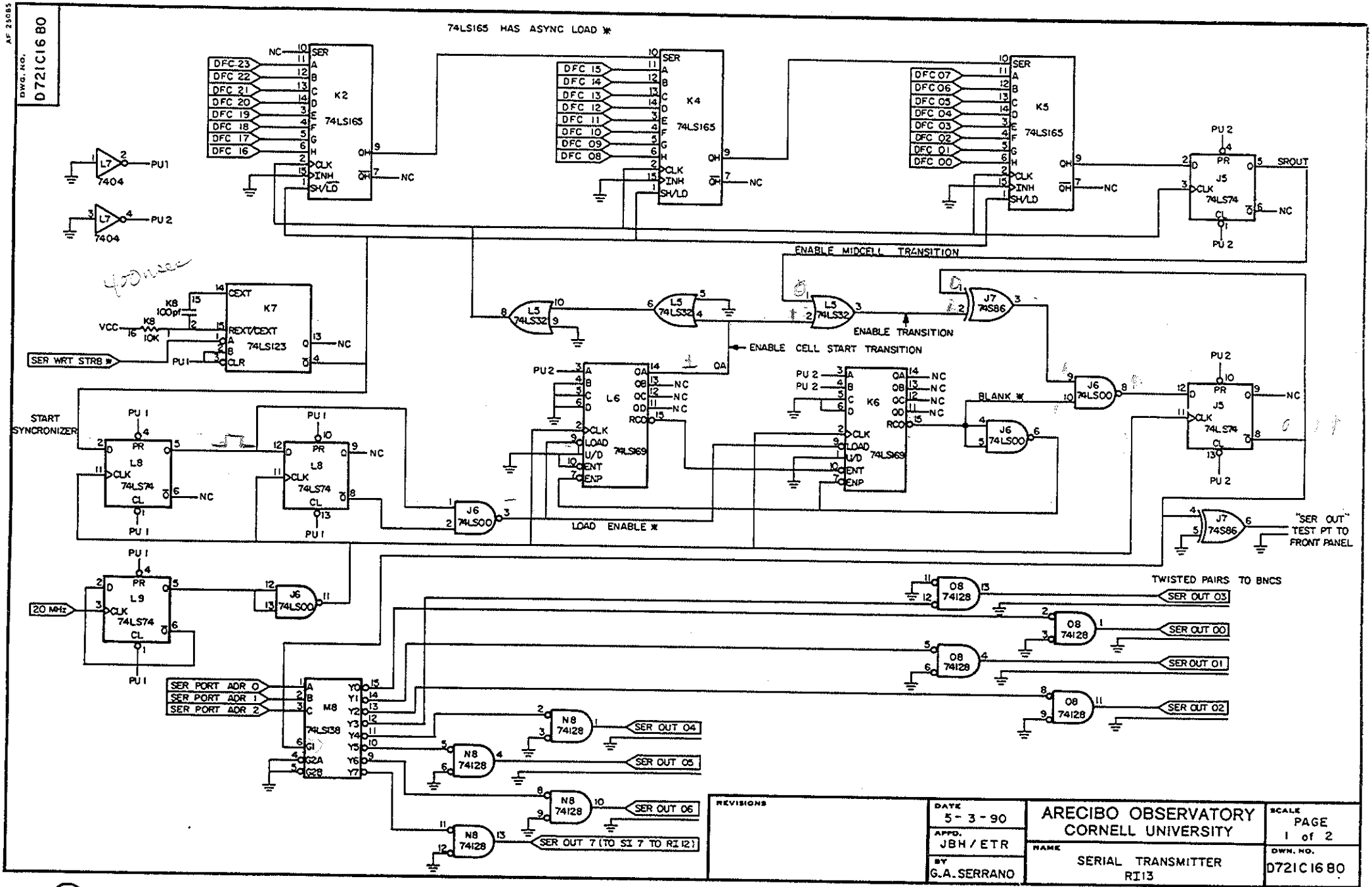


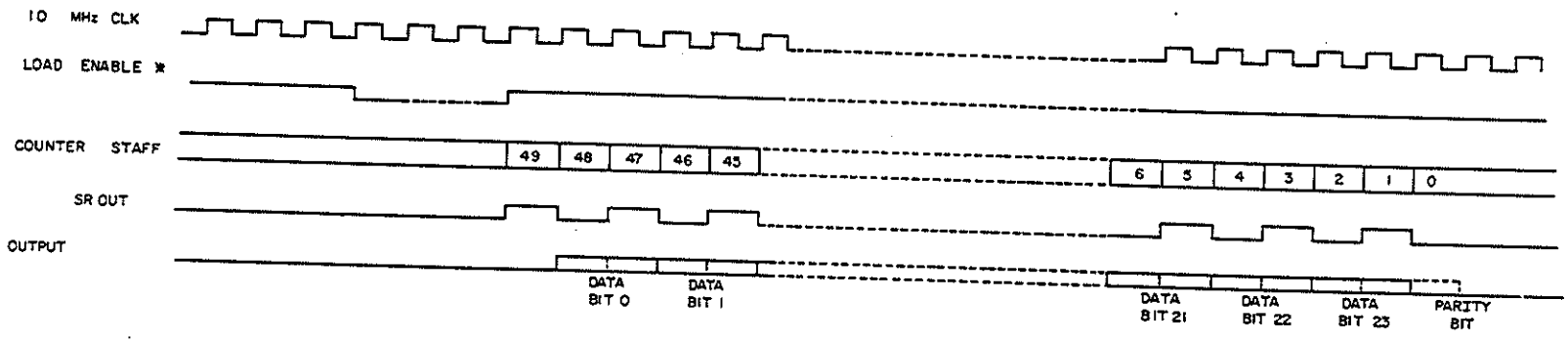
C. DIP CARRIER DETAIL



REVISIONS	DATE	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 2 of 2
	5 - 2 - 90		
	APPD. JBH / ETR	NAME SERIAL RECEIVER RI12	DWN. NO. D721C1580
	BY G. A. SERRANO		

(89)


74LS165 HAS ASYNC LOAD *
DWG. NO. D721C1680
K2
K4
K5
74LS165
DFC 23
DFC 22
DFC 21
DFC 20
DFC 19
DFC 18
DFC 17
DFC 16
DFC 15
DFC 14
DFC 13
DFC 12
DFC 11
DFC 10
DFC 09
DFC 08
DFC 07
DFC 06
DFC 05
DFC 04
DFC 03
DFC 02
DFC 01
DFC 00
SER
CLK
INH
SH/LD
QH
NC
L7
7404
PU1
PU2
J5
74LS74
PR
CL
SROUT
ENABLE MIDCELL TRANSITION
ENABLE TRANSITION
ENABLE CELL START TRANSITION
K7
74LS123
REXT/CEXT
CEXT
K8
100pf
10K
VCC
SER WRT STRB *
CLR
L5
74LS32
J7
74S86
L6
74LS169
K6
U/D
ENT
ENP
RCO
QA
QB
QC
QD
J6
74LS00
BLANK *
START SYNCRONIZER
L8
L9
20 MHz
LOAD ENABLE *
"SER OUT" TEST PT TO FRONT PANEL
TWISTED PAIRS TO BNCS
SER OUT 03
SER OUT 00
SER OUT 01
SER OUT 02
SER OUT 04
SER OUT 05
SER OUT 06
SER OUT 7 (TO SI 7 TO RI 12)
SER PORT ADR 0
SER PORT ADR 1
SER PORT ADR 2
M8
74LS138
N8
74128
O8
74128
REVISIONS
DATE 5-3-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME SERIAL TRANSMITTER RI13
SCALE
PAGE 1 of 2
DWN. NO. D721C1680

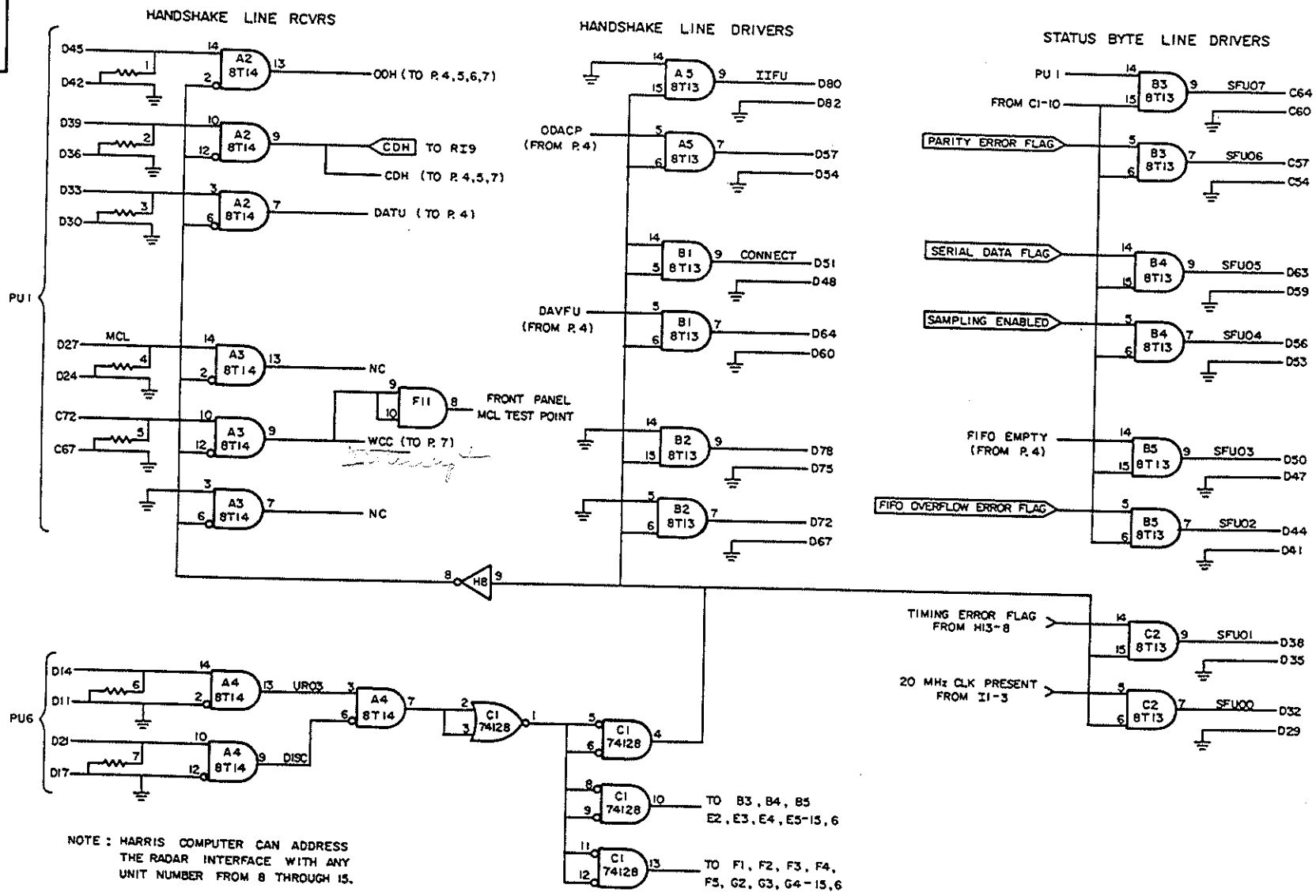


NOTE: OUTPUT HAS A TRANSITION AT THE BEGINNING OF EACH 200 NSC CELL. IF THE DATA BIT IS A 1 THERE IS ALSO A TRANSITION AT MIDCELL. THE NUMBER OF "1s" INCLUDING THE PARITY BIT WILL ALWAYS BE ODD (ODD PARITY)

REVISIONS	DATE 5-4-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 2 of 2
	APPD. JBH/ETR	NAME SERIAL TRANSMITTER RI13	DWN. NO. D721T0380
	BY G.A. SERRANO		

(10)

DWG. NO. D721C1780



NOTE : HARRIS COMPUTER CAN ADDRESS THE RADAR INTERFACE WITH ANY UNIT NUMBER FROM 8 THROUGH 15.

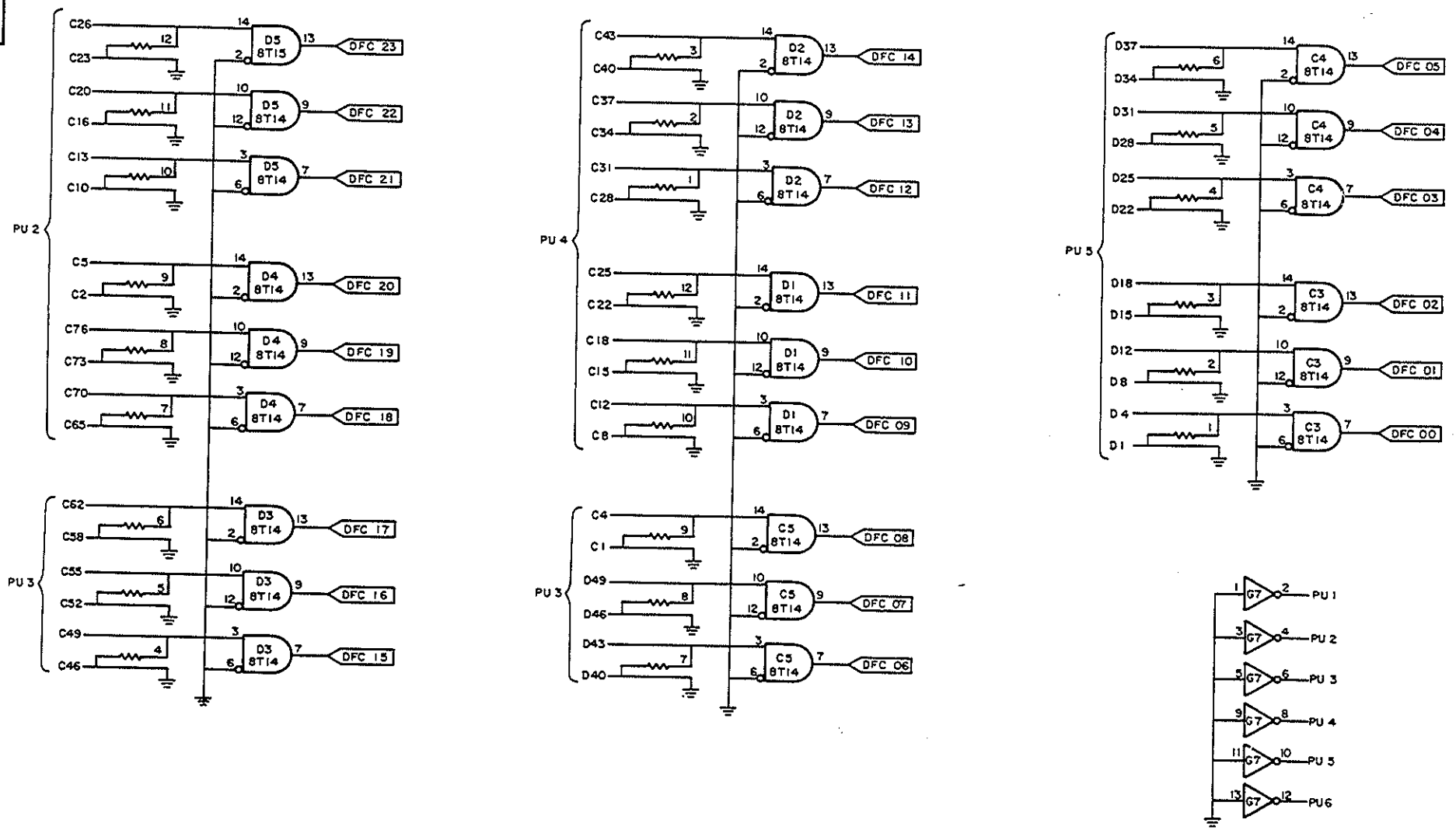
NOTE : 8T13 EQUIV. TO SN75121
8T14 EQUIV. TO SN75122

REVISIONS	DATE	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	5 - 4 - 90		PAGE 1 of 9
	APPD. JBH / ETR	NAME CONTROLLER RI14	DWN. NO. D721C1780
	BY G.A. SERRANO		

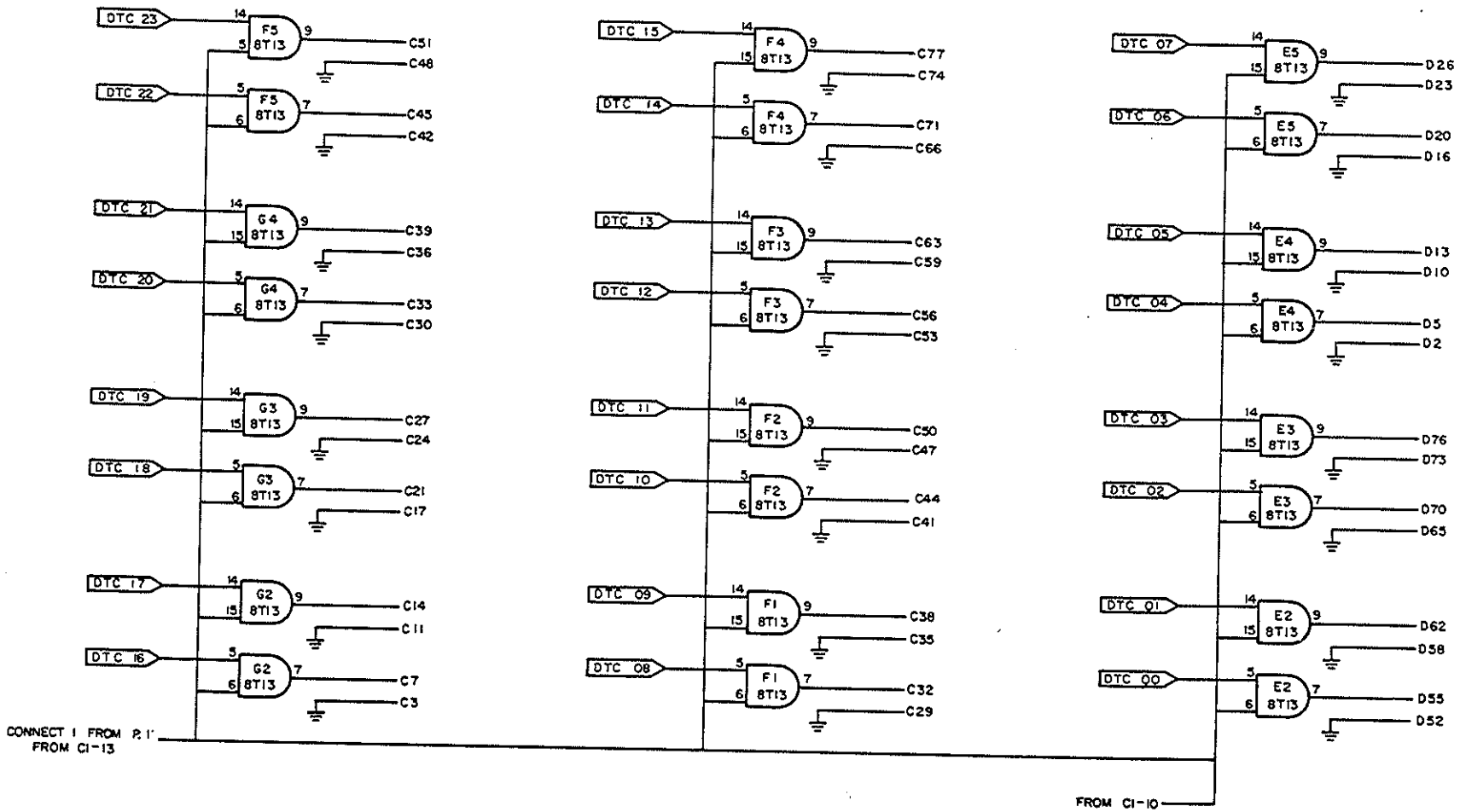
(1L)

DWG. NO. D721C1880

TWISTED PAIRS TO
C & D CONNECTORS

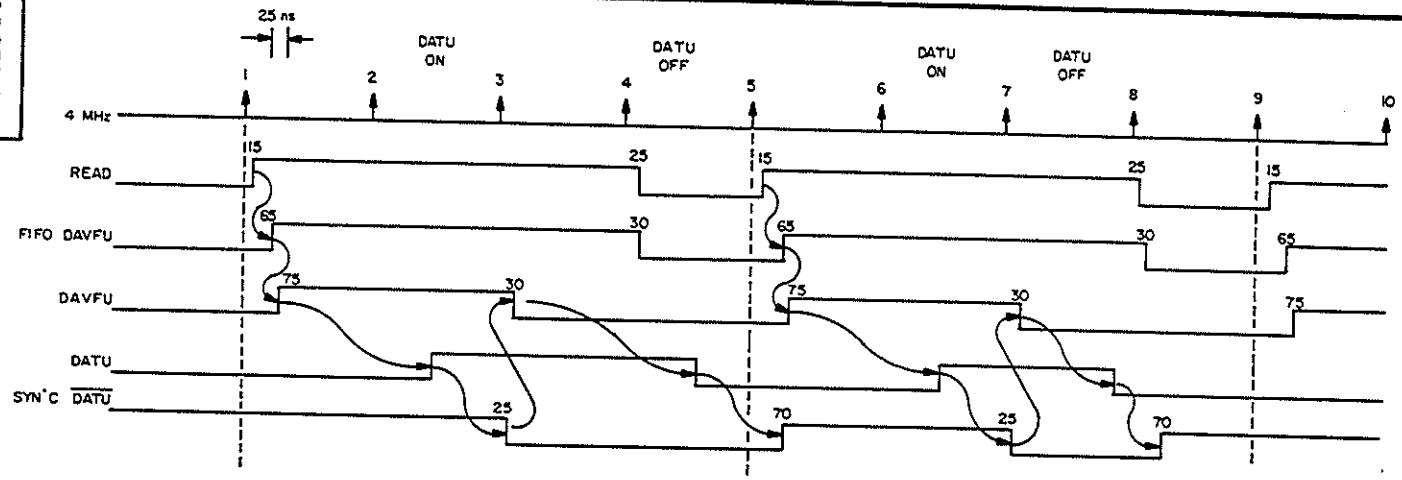


REVISIONS	DATE 5 - 7 - 90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 2 of 9
	APPD. JBH / ETR	NAME CONTROLLER RI14	DWN. NO. D721C1880
	BY G.A. SERRANO		

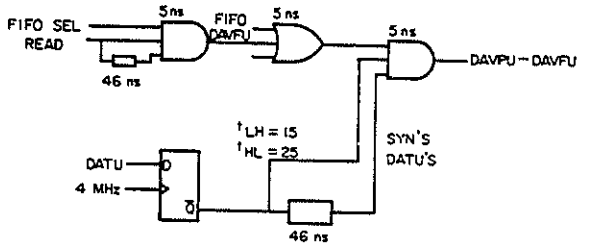


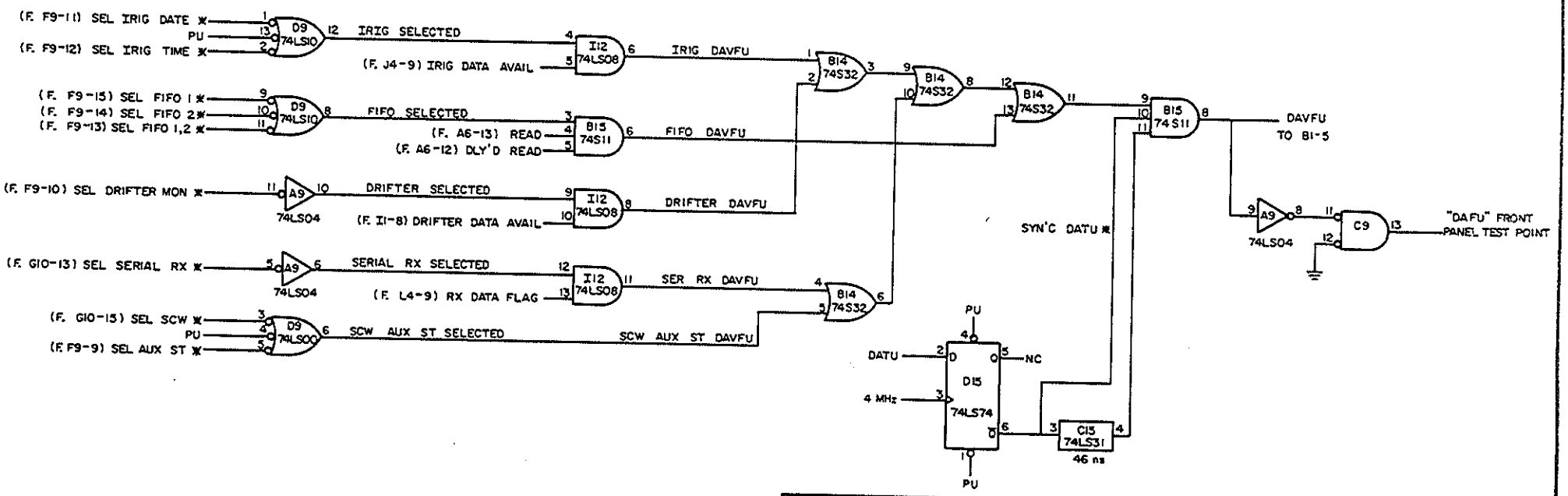
REVISIONS	DATE 5-7-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 3 of 9
	APPD. JBH/ETR	NAME CONTROLLER RI14	DWN. NO. D721C19 B0
	BY G.A. SERRANO		

(3)

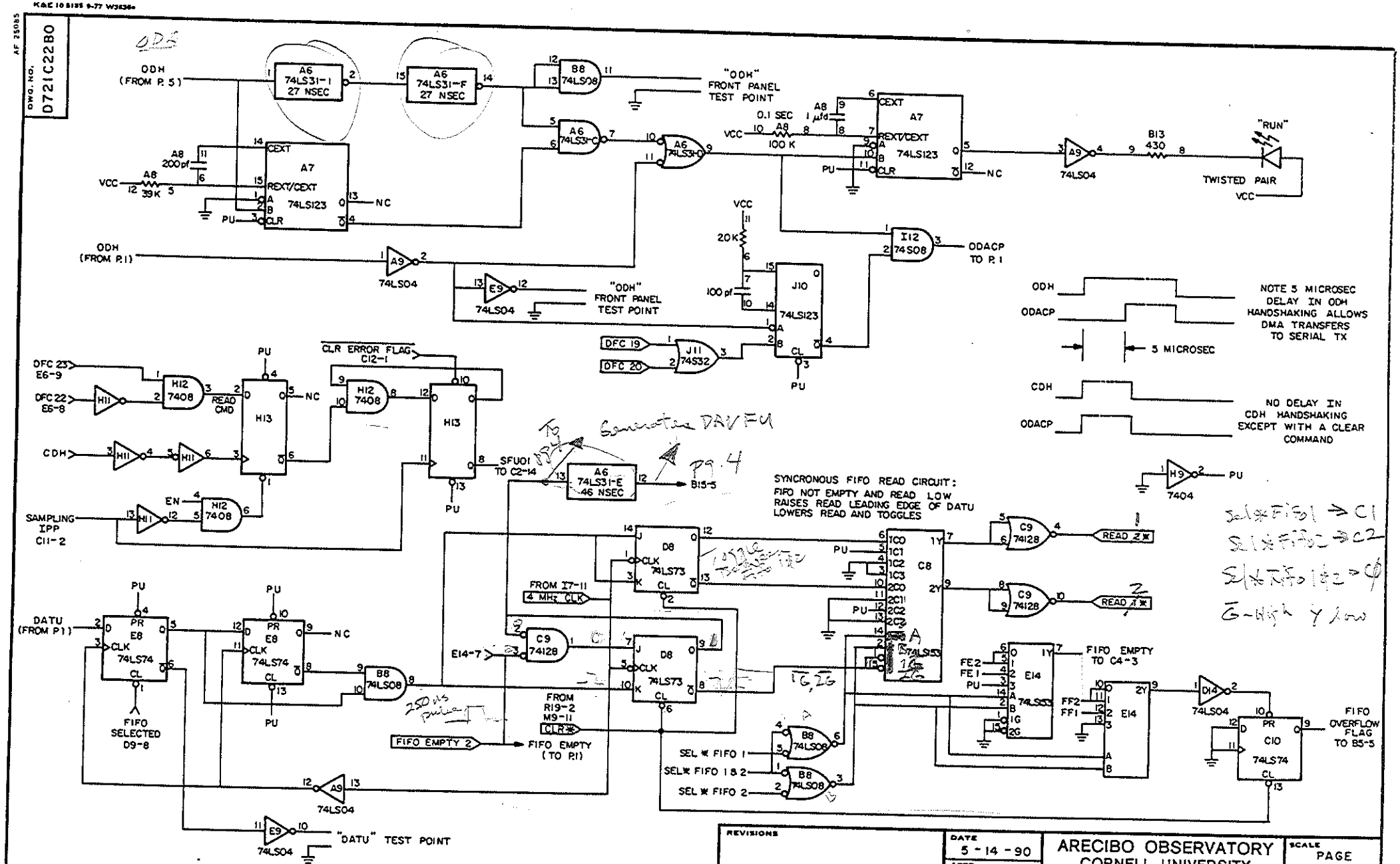


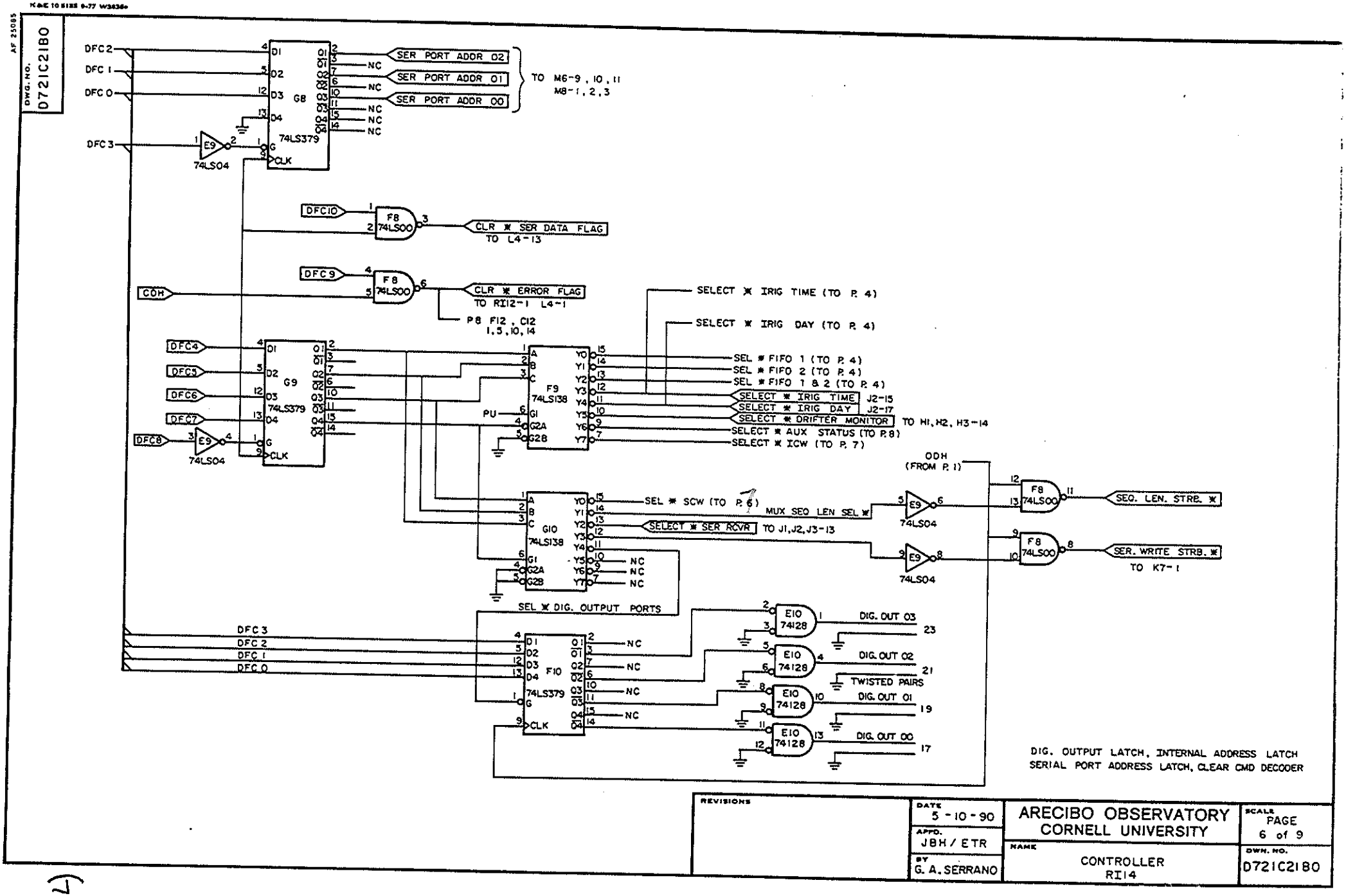
FIFO READ EQUIVALENT CIRCUIT





REVISIONS	DATE 5 - 9 - 90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 4 of 9
	APPD. JBH / ETR	NAME CONTROLLER RI14	DWN. NO. D721C2080
	BY G.A. SERRANO		


DWG. NO. D721C22B0
ODH (FROM P. 5)
A6 74LS31-1 27 NSEC
A6 74LS31-F 27 NSEC
B8 74LS08
"ODH" FRONT PANEL TEST POINT
A6 74LS31-C
A6 74LS31-D
A8 0.1 SEC 1 µfd
VCC
A8 100 K
A7 74LS123
REXT/CEXT
CEXT
CLR
PU
NC
A9 74LS04
B13 430
"RUN"
TWISTED PAIR
A8 200 pf
A8 39K
ODH (FROM P.1)
E9 74LS04
"ODH" FRONT PANEL TEST POINT
20K
100 pf
J10 74LS123
I12 74S08
ODACP TO P.1
DFC 19
DFC 20
J11 74S32
NOTE 5 MICROSEC DELAY IN ODH HANDSHAKING ALLOWS DMA TRANSFERS TO SERIAL TX
5 MICROSEC
NO DELAY IN CDH HANDSHAKING EXCEPT WITH A CLEAR COMMAND
CLR ERROR FLAG C12-1
DFC 23 E6-9
DFC 22 E6-8
H12 7408
H11
READ CMD
H13
CDH
SAMPLING IPP C11-2
EN
SFU01 TO C2-14
A6 74LS31-E 46 NSEC
B15-5
SYNCRONOUS FIFO READ CIRCUIT:
FIFO NOT EMPTY AND READ LOW RAISES READ LEADING EDGE OF DATU LOWERS READ AND TOGGLES
H9 7404
PU
DATU (FROM P1)
E8 74LS74
FIFO SELECTED D9-8
FROM I7-11 4 MHz CLK
D8 74LS73
C9 74128
C8 74LS153
READ 2*
READ 1*
E14-7
FROM R19-2 M9-11 CLR*
FIFO EMPTY 2
FIFO EMPTY (TO P1)
SEL * FIFO 1
SEL* FIFO 1 & 2
SEL * FIFO 2
E14
FE2
FE1
FF2
FF1
FIFO EMPTY TO C4-3
D14 74LS04
C10 74LS74
FIFO OVERFLOW FLAG TO B5-5
A9 74LS04
E9 74LS04
"DATU" TEST POINT
NOTE: 74LS73 CAN'T BE REPLACED BY 7473 (CLOCK POLARITIES ARE DIFFERENT)
REVISIONS
DATE 5-14-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY CORNELL UNIVERSITY
NAME CONTROLLER RI14
SCALE PAGE 5 of 9
DWN. NO. D721C22B0



REVISIONS	DATE 5-10-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 6 of 9
	APPD. JBH / ETR	NAME CONTROLLER RI14	DWN. NO. D721C2180
	BY G. A. SERRANO		

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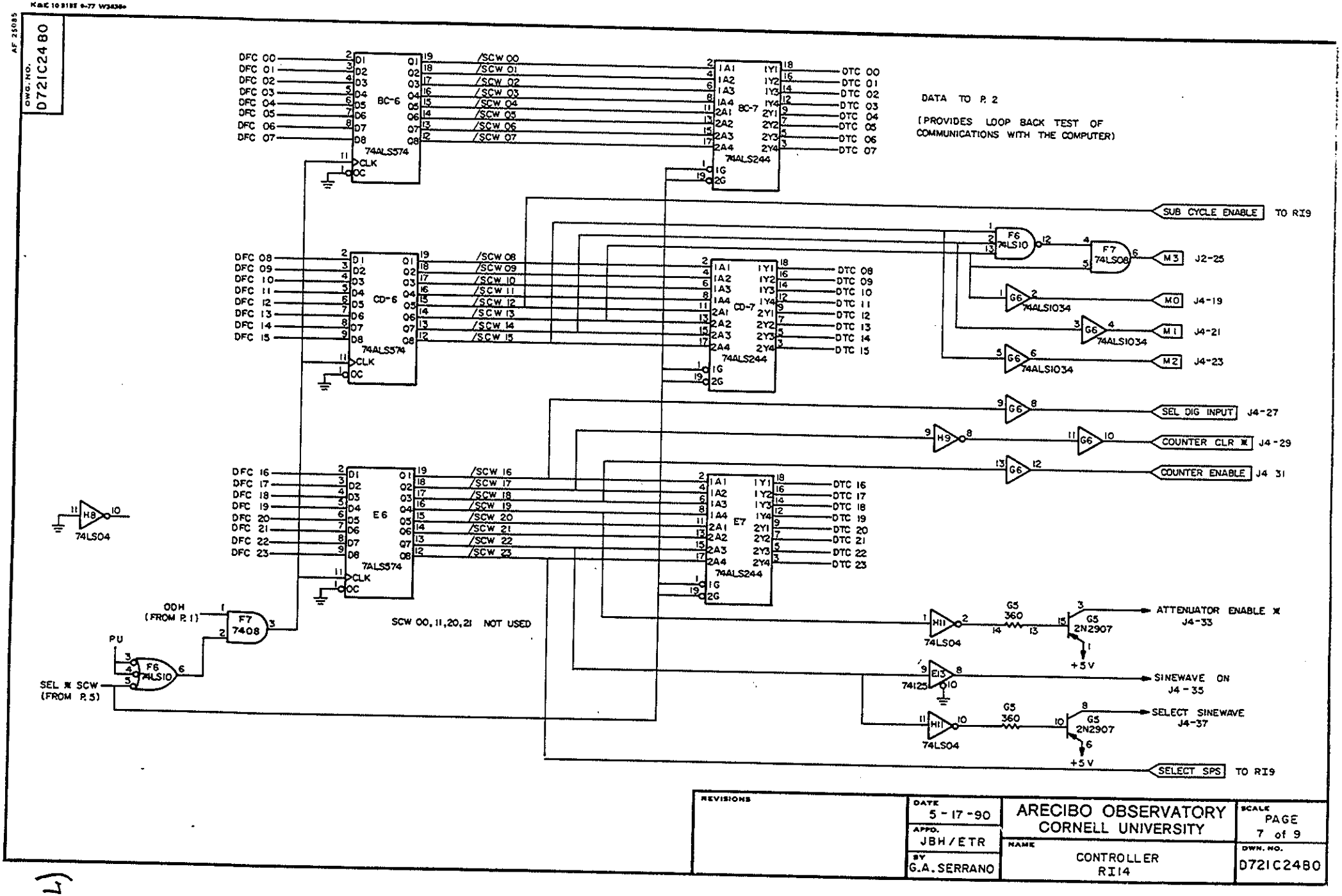
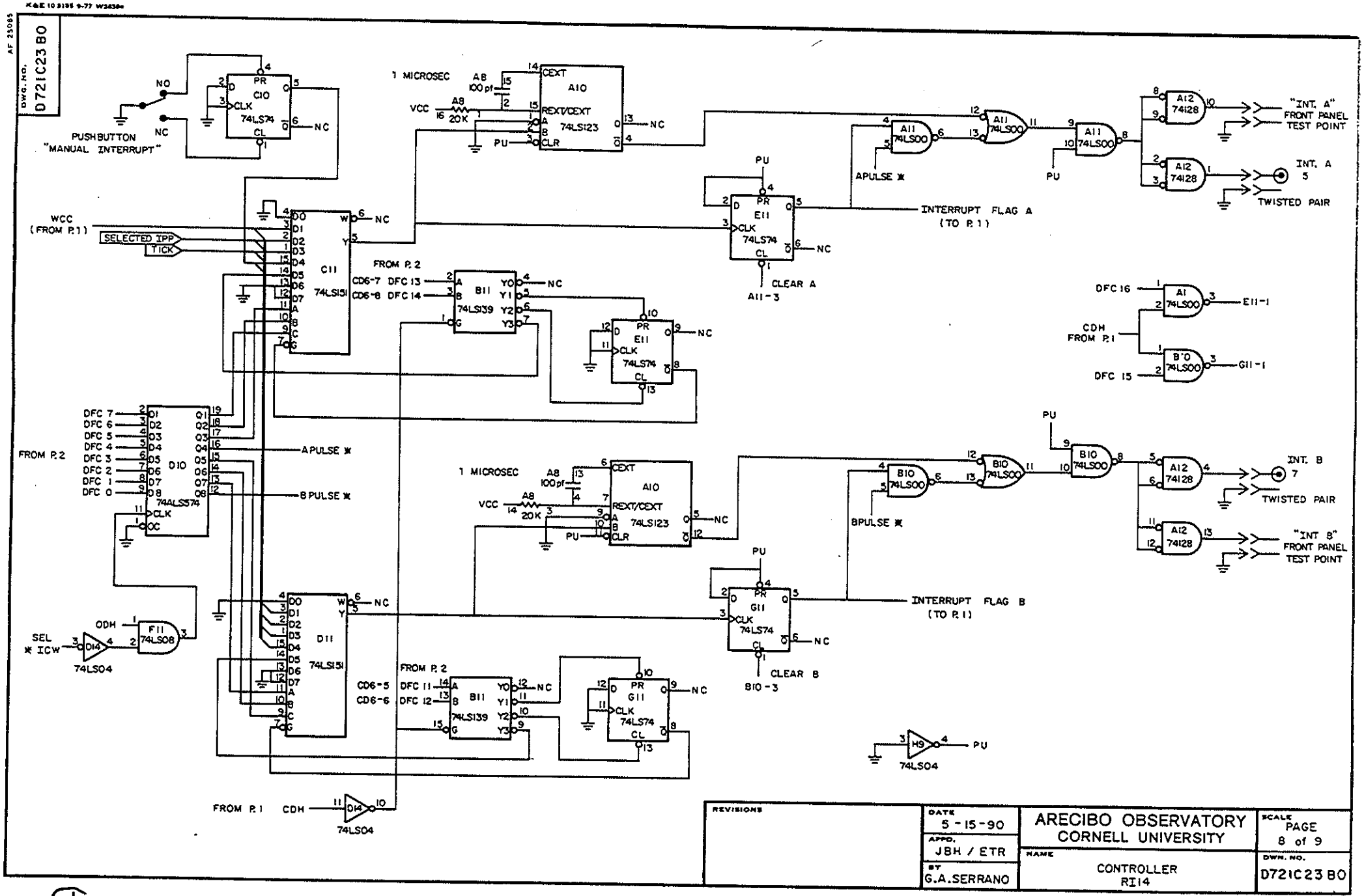
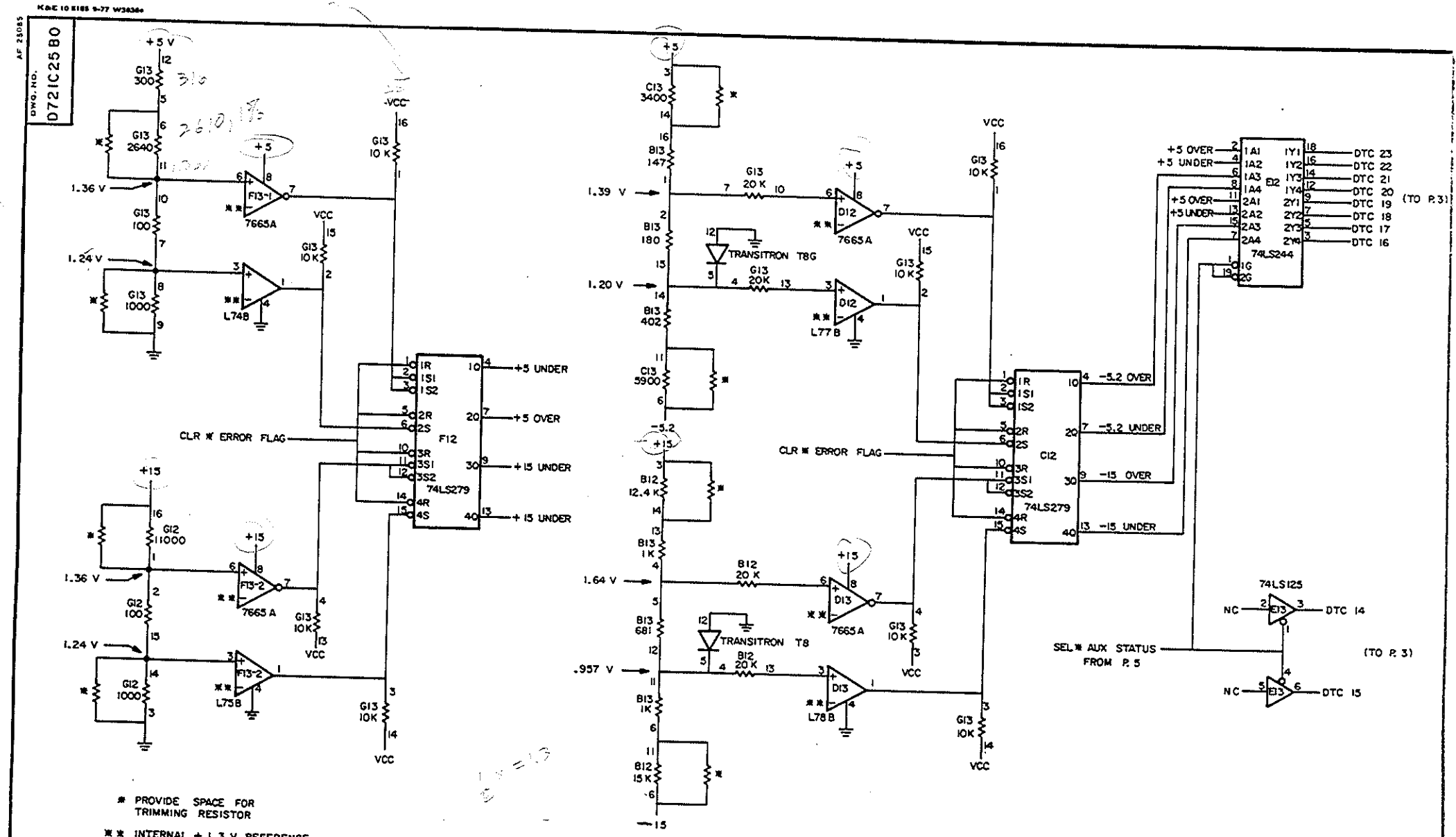

DWG. NO. D721C2480
DFC 00
DFC 01
DFC 02
DFC 03
DFC 04
DFC 05
DFC 06
DFC 07
BC-6
74ALS574
/SCW 00
/SCW 01
/SCW 02
/SCW 03
/SCW 04
/SCW 05
/SCW 06
/SCW 07
BC-7
74ALS244
DTC 00
DTC 01
DTC 02
DTC 03
DTC 04
DTC 05
DTC 06
DTC 07
DATA TO P. 2
(PROVIDES LOOP BACK TEST OF COMMUNICATIONS WITH THE COMPUTER)
SUB CYCLE ENABLE
TO RI9
DFC 08
DFC 09
DFC 10
DFC 11
DFC 12
DFC 13
DFC 14
DFC 15
CD-6
74ALS574
/SCW 08
/SCW 09
/SCW 10
/SCW 11
/SCW 12
/SCW 13
/SCW 14
/SCW 15
CD-7
74ALS244
DTC 08
DTC 09
DTC 10
DTC 11
DTC 12
DTC 13
DTC 14
DTC 15
F6 74LS10
F7 74LS08
M3
J2-25
G6 74ALS1034
MO
J4-19
M1
J4-21
M2
J4-23
SEL DIG INPUT
J4-27
H9
COUNTER CLR *
J4-29
COUNTER ENABLE
J4 31
DFC 16
DFC 17
DFC 18
DFC 19
DFC 20
DFC 21
DFC 22
DFC 23
E6
74ALS574
/SCW 16
/SCW 17
/SCW 18
/SCW 19
/SCW 20
/SCW 21
/SCW 22
/SCW 23
E7
74ALS244
DTC 16
DTC 17
DTC 18
DTC 19
DTC 20
DTC 21
DTC 22
DTC 23
H8
74LS04
ODH (FROM P. 1)
F7 7408
PU
F6 74LS10
SEL * SCW (FROM P. 5)
SCW 00, 11, 20, 21 NOT USED
H11
74LS04
G5 360
G5 2N2907
+5V
ATTENUATOR ENABLE *
J4-33
E13
74125
SINEWAVE ON
J4-35
SELECT SINEWAVE
J4-37
SELECT SPS
TO RI9
REVISIONS
DATE 5-17-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME CONTROLLER RI14
SCALE PAGE 7 of 9
DWN. NO. D721C2480

(LL)


DWG. NO. D721C23 BO
PUSHBUTTON "MANUAL INTERRUPT"
NO
NC
C10
74LS74
1 MICROSEC
A8 100 pf
VCC
A8 16 20K
A10
74LS123
REXT/CEXT
CEXT
PU
NC
A11 74LS00
A12 74128
"INT. A" FRONT PANEL TEST POINT
INT. A 5
TWISTED PAIR
APULSE *
INTERRUPT FLAG A (TO P.1)
E11
CLEAR A
A11-3
WCC (FROM P.1)
SELECTED IPP
TICK
C11
74LS151
FROM P.2
CD6-7 DFC 13
CD6-8 DFC 14
B11
74LS139
DFC 16
CDH FROM P.1
DFC 15
A1
B'0
E11-1
G11-1
D10
74ALS574
DFC 7
DFC 6
DFC 5
DFC 4
DFC 3
DFC 2
DFC 1
DFC 0
BPULSE *
B10 74LS00
INT. B 7
"INT B" FRONT PANEL TEST POINT
G11
INTERRUPT FLAG B (TO P.1)
CLEAR B
B10-3
D11
SEL * ICW
ODH
F11 74LS08
D14 74LS04
CD6-5
CD6-6
H9
FROM P.1
CDH
REVISIONS
DATE 5-15-90
APPD. JBH / ETR
BY G.A.SERRANO
ARECIBO OBSERVATORY CORNELL UNIVERSITY
NAME CONTROLLER RI14
SCALE PAGE 8 of 9
DWG. NO. D721C23 BO

(8L)


DWG. NO. D721C25B0
+5 V
G13 300
G13 2640
1.36 V
G13 100
1.24 V
G13 1000
F13-1
7665A
L74B
VCC
G13 10 K
CLR * ERROR FLAG
F12
74LS279
1R
1S1
1S2
2R
2S
3R
3S1
3S2
4R
4S
+5 UNDER
+5 OVER
+15 UNDER
+15
G12 11000
G12 100
G12 1000
F13-2
7665 A
L75B
G13 3400
B13 147
B13 180
B13 402
G13 5900
-5.2
1.39 V
G13 20 K
D12
7665A
TRANSITRON T8G
1.20 V
L77B
B12 12.4 K
B13 1K
1.64 V
B12 20 K
D13
7665A
TRANSITRON T8
.957 V
B13 681
B12 15 K
L78B
C12
74LS279
-5.2 OVER
-5.2 UNDER
-15 OVER
-15 UNDER
E12
74LS244
1A1
1A2
1A3
1A4
2A1
2A2
2A3
2A4
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
2Y3
2Y4
1G
2G
DTC 23
DTC 22
DTC 21
DTC 20
DTC 19
DTC 18
DTC 17
DTC 16
(TO P. 3)
74LS125
E13
NC
DTC 14
DTC 15
SEL * AUX STATUS
FROM P. 5
(TO P. 3)
* PROVIDE SPACE FOR TRIMMING RESISTOR
** INTERNAL + 1.3 V REFERENCE
5.25 V.
4.75 V.
3.3+
REVISIONS
DATE 5-18-90
APPD. JBH/ETR
BY G.A. SERRANO
ARECIBO OBSERVATORY
CORNELL UNIVERSITY
NAME CONTROLLER RI14
SCALE PAGE 9 of 9
DWG. NO. D721C25B0

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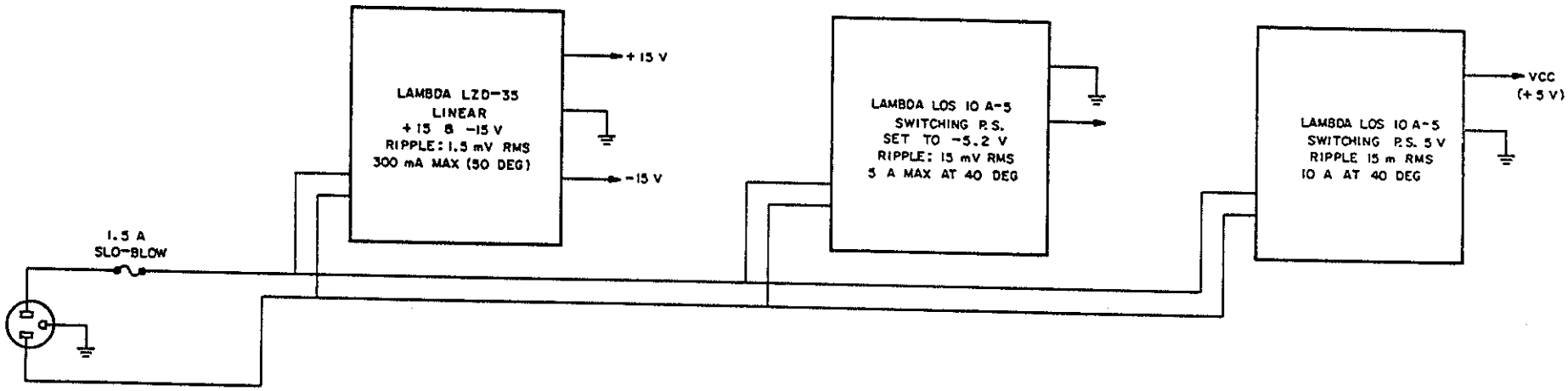
DWG. NO. D721C27 B0



REVISIONS	DATE 5-18-90	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE PAGE 1 of 1
	APPD. JBH/ETR	NAME POWER SUPPLY RI15	DWN. NO. D721C27
	BY G.A. SERRANO		

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11.0 APPENDIX

J4 - Connector

1-	CLR*	21-	M1
2-		22-	
3-	To U23	23-	M2
4-		24-	
5-	FIFO full 2	25-	M3
6-		26-	
7-	FIFO empty 2	27-	Select Digital Input
8-		28-	
9-	IRIG Data available	29-	Counter CLR
10-		30-	
11-	READ 2	31-	Counter Enable
12-		32-	
13-	READ	33-	Attenuator Enable
14-		34-	
15-	Select IRIG time	35-	Sinewave ON
16-		36-	
17-	Select IRIG Day	37-	Select Sinewave
18-		38-	
19-	M0	39-	IRIG Code
20-		40-	

J5 Connector

1-	DTC00	26-	
2-		27-	DTC13
3-	DTC01	28-	
4-		29-	DTC14
5-	DTC02	30-	
6-		31-	DTC15
7-	DTC03	32-	
8-		33-	DTC16
9-	DTC04	34-	
10-		35-	DTC17
11-	DTC05	36-	
12-		37-	DTC18
13-	DTC06	38-	
14-		39-	DTC19
15-	DTC07	40-	
16-		41-	DTC20
17-	DTC08	42-	
18-		43-	DTC21
19-	DTC09	44-	
20-		45-	DTC22
21-	DTC10	46-	
22-		47-	DTC23
23-	DTC11	48-	
24-		49-	IRIG Code Input
25-	DTC12	50-	

J6 - Connector

1-	Serial In 6	18-	Ground
2-	Ground	19-	Serial Out 02
3-	Serial In 5	20-	Ground
4-	Ground	21-	Serial Out 03
5-	Serial In 4	22-	Ground
6-	Ground	23-	Serial Out 04
7-	Serial In 3	24-	Ground
8-	Ground	25-	Serial Out 05
9-	Serial In 2	26-	Ground
10-	Ground	27-	Serial Out 06
11-	Serial In 1	28-	Ground
12-	Ground	29-	Spare
13-	Serial In 0	30-	Ground
14-	Ground	31-	Spare
15-	Serial Out 00	32-	Ground
16-	Ground	32-	Spare
17-	Serial Out 01	34-	Ground

J7 - Connector

1-	20 MHz Fixed Clock	18-	
2-		19-	Digital Out 01
3-	RTG Tick	20-	
4-		21-	Digital Out 02
5-	Interface A	22-	
6-		23-	Digital Out 03
7-	Interface B	24-	
8-		25-	MUX Advance
9-	SPS IPP	26-	
10-		27-	MUX Reset
11-	RTG IPP	28-	
12-		29-	IRIG Code Input
13-	SPS GW	30-	
14-		31-	Spare
15-	RTG GW	32-	
16-		33-	Spare
17-	Digital Out 00	34-	

J8 Connector - Front Panel

1-	DATU	17-	IPP
2-	Ground	18-	Ground
3-	ODH	19-	Sample Pulse
4-	Ground	20-	Ground
5-	CDH	21-	WCC
6-	Ground	22-	Ground
7-	DAVFU	23-	IRIG Code
8-	Ground	24-	Ground
9-	INT A	25-	Spare
10-	Ground	26-	Ground
11-	INT B	27-	Spare
12-	Ground	28-	Ground
13-	Serial In	29-	Spare
14-	Ground	30-	Ground
15-	Serial Out	31-	Spare
16-	Ground	32-	Ground

Signal	Location	Ribbon Conn.	Winchester
CDH*	D	10	36
CDH+	D	9	39
CNCT*	D	14	48
CNCT+	D	15	51
DATU*	D	8	30
DATU+	D	7	33
DAVFU*	D	18	60
+	D	17	64
DFU00*	D	18	52
+	D	17	55
DFU01*	D	20	58
+	D	19	62
DFU02*	D	22	65
+	D	21	70
DFU03*	D	24	73
+	D	23	76
DFU04*	D	26	2
+	D	25	5
DFU05*	D	28	10
+	D	27	13
DFU06*	D	30	16
+	D	29	20
DFU07*	D	32	23
+	D	31	26
DFU08*	C	34	29
+	C	33	32
DFU09*	C	36	35
+	C	35	38
DFU10*	C	38	41
+	C	37	44
DFU11*	C	40	47
	C	39	50
DFU12*	C	42	53
+	C	41	56
DFU13*	C	44	59
+	C	43	63
DFU14*	C	46	66
+	C	45	71
DFU15*	C	48	74
+	C	47	77
DFU16*	C	50	3
+	C	49	7
DFU17*	C	26	11
+	C	25	14
DFU18*	C	28	17
+	C	27	21
DFU19*	C	30	24
+	C	29	27
DFU20*	C	32	30
+	C	31	33

Signal	Location	Ribbon Conn	Winchester
DFU21*	C	34	36
+	C	33	39
DFU22*	C	36	42
+	C	35	45
DFU23*	C	38	48
+	C	37	51
DISC *	D	4	17
+	D	3	21
DTU00*	D	2	1
+	D	1	4
DTU01*	D	4	8
+	D	3	12
DTU02*	D	6	15
+	D	5	18
DTU03*	D	8	22
+	D	5	25
DTU04*	D	10	28
+	D	9	31
DTU05*	D	12	34
+	D	11	37
DTU06*	D	14	40
+	D	13	43
DTU07*	D	16	46
+	D	15	49
DTU08*	C	2	1
+	C	1	4
DTU09*	C	4	8
+	C	3	12
DTU10*	C	6	15
+	C	5	18
DTU11*	C	8	22
+	C	7	25
DTU12*	C	10	28
+	C	9	31
DTU13*	C	12	34
+	C	11	37
DTU14*	C	14	40
+	C	13	43
DTU15*	C	16	46
+	C	15	49
DTU16*	C	18	52
+	C	17	55
DTU17*	C	20	58
+	C	19	62
DTU18*	C	22	65
+	C	21	70
DTU19*	C	24	73
+	C	23	76
DTU20*	C	26	2
+	C	25	5

Signal	Location	Ribbon Conn.	Winchester
DTU21*	C	28	10
+	C	27	13
DTU22*	C	28	16
+	C	29	20
DTU23*	C	30	23
+	C	31	26
ECBEI*	D	22	75
+	D	21	78
IIFU *	D	24	82
+	D	23	80
MCL *	D	6	24
+	D	5	27
ODACP*	D	16	54
+	D	15	57
ODH *	D	12	42
+	D	11	45
SFU00*	D	34	29
+	D	33	32
SFU01*	D	36	35
+	D	35	38
SFU02*	D	38	41
+	D	37	44
SFU03*	D	40	47
+	D	39	50
SFU04*	D	42	53
+	D	41	56
SFU05*	D	44	59
+	D	43	63
SFU06*	C	40	54
+	C	39	57
SFU07*	C	42	60
+	C	41	64
UOIE *	D	20	67
+	D	19	72
UR0 *	D	46	66
+	D	45	71
UR1 *	D	48	74
+	D	47	77
UR2 *	D	50	3
+	D	49	7
UR3 *	D	2	11
+	D	1	14
WCCI *	C	44	67
+	C	43	72

DIGITAL INPUTS

Signal	Winchester	Ribbon Conn.
Digital Input 00+	A	1
*	C	2
01+	E	3
*	H	4
02+	K	5
*	M	6
03+	P	7
*	S	8
04+	U	9
*	W	10
05+	Y	11
*	a	12
06+	c	13
*	e	14
07+	h	15
*	k	16
08+	n	17
*	r	18
09+	t	19
*	v	20
10+	x	21
*	z	22
11+	BB	23
*	DD	24
12+	B	25
*	D	26
13+	F	27
*	J	28
14+	L	29
*	N	30
15+	R	31
*	T	32
16+	V	33
*	X	34
17+	Z	35
*	b	36
18+	d	37
*	f	38
19+	j	39
*	m	40
20+	p	41
*	s	42
21+	u	43
*	w	44
22+	y	45
*	AA	46
23+	CC	47
*	EE	48
24+	HH	49
*	FF	50

12.0 GLOSSARY

Adage Interface:
Predecessor of the Radar Interface. Provided two 12-bit 500 KHz digitizers, no FIFO buffer. Provided parallel 24-bit control for two HP synthesizers.

BCD:
Binary-coded-decimal, the 4-bit 8421 format used in the fields of the IRIG timecode.

BNC:
Bayonet "N" Connector, the coaxial jacks used on the RI.

DMA:
Direct Memory Access, for automatic block transfers of data to/from the computer.

FIFO:
First-In-First-Out memory used in the RI to buffer the digitizer data. Provides fast burst sampling and faster continuous sampling.

Gatewidth:
The external pulse used to trigger the RI's digitizers.

IRIG Time Code:
The serial time code provided by the station clock to the RI. The name is NASA for Inter Range Instrumentation Group. The IRIG A format has a frame rate of 10 Hz.

IPP:
Interpulse Period, the external pulse used to enable the RI to accept Gatewidth pulses (the IPP synchronizes the start of data taking).

Radar Multiplexer (RMUX):
Companion unit to the Radar Interface. Provides dual 8-to-1 analog multiplexers to expand the number of port pairs on the RI. The RMUX connects to one of the serial ports of the RI for programming.

Radar Timing Generator (RTG):
Companion unit to the Radar Interface. Programmable timing generator to provide GW, IPP, and Time Tick pulses to the Radar Interface. The RTG connects to one of the serial ports of the RI for programming.

13.0 INDEX