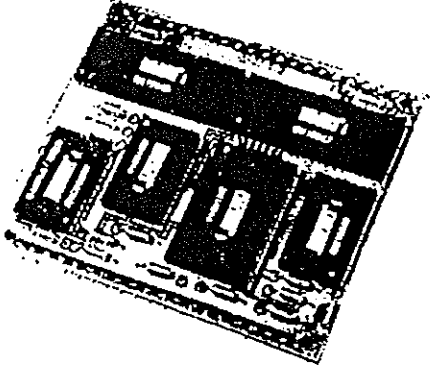
9.0 MANUFACTURERS' DATA SHEETS

BURR-BROWN®



ADC600

12-BIT ULTRA-HIGH SPEED A/D CONVERTER

FEATURES

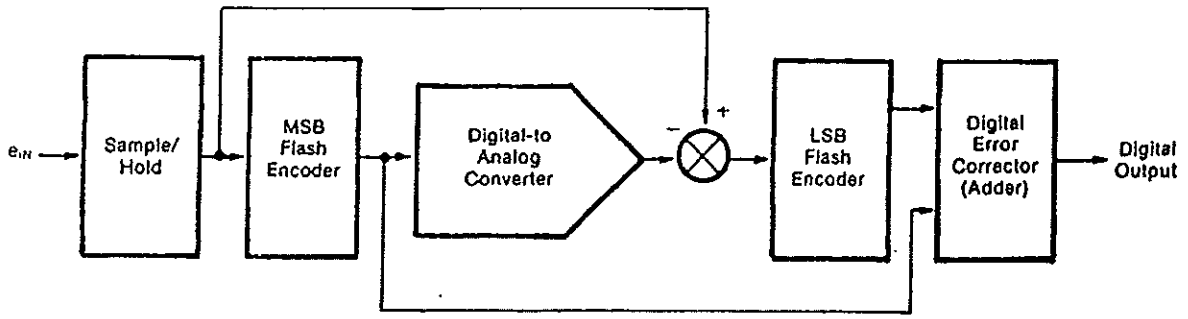
- HIGH RESOLUTION: 12 bits
- SAMPLE RATE: DC to 10MHz
- HIGH SINAD RATIO: 67dB
- LOW HARMONIC DISTORTION: −71dB
- LOW INTERMODULATION DISTORTION: −70dB
- INPUT RANGE: ±1.25V
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- LOW DISSIPATION: 8.5W
- 0°C TO +70°C AND −25°C TO +85°C

- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- JAM-RESISTANT SYSTEMS
- SIGINT, ECM, AND EW SYSTEMS
- DIGITAL COMMUNICATIONS
- DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC600 is an ultra-high speed analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding dynamic range has been achieved by minimizing noise and distortion.

The ADC600 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry. Laser-trimmed ceramic submodules are mounted on a 17-square-inch multilayer PC motherboard. Logic is ECL.



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PDS-642B

Printed in U.S.A. September, 1988

SPECIFICATIONS

ELECTRICAL

T_A = −25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = 15V, V_{DD1} = +5V, V_{DD2} = −5.2V, and 15-minute warmup in normal convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC600K MIN	ADC600K TYP	ADC600K MAX	ADC600B MIN	ADC600B TYP	ADC600B MAX	UNITS
RESOLUTION				12			•	Bits
INPUTS								
ANALOG								
Input Range	Full scale	−1.25		+1.25	•		•	V
Input Impedance			1.5			•		MΩ
Input Capacitance			5			•		pF
DIGITAL								
Logic Family			ECL 10k-Compatible			•		
Convert Command			Negative Edge			•		
Pulse Width		10			•			ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	F = 200Hz		±0.1	±0.5		•	•	% FSR
Input Offset	DC		±0.1	±0.5		•	•	% FSR[1]
Integral Linearity Error	F = 200Hz			1.25			•	LSB
Differential Linearity Error	F = 200Hz: 68.3% of all codes			0.25			•	LSB
	99.7% of all codes			1.00			•	LSB
	100% of all codes			1.25			•	LSB
				−1.00			•	LSB
Missing Codes				none			•	
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	•		•	Samples/s
Conversion Time	First conversion	115	150	160	•	•	•	ns
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	F = 4.9MHz: 68.3% of all codes			0.5			•	LSB
	99.7% of all codes			1.5			•	LSB
	100% of all codes			2.0			•	LSB
Total Harmonic Distortion[2]								
F = 4.8MHz (0dB)	F_S = 10MHz		−71			•		dBC[3]
F = 0.58MHz (0dB)			−74			•		dBC
F = 2.4MHz (0dB)	F_S = 5MHz		−73			•		dBC
F = 0.58MHz (0dB)			−74.5			•		dBC
Two-Tone Intermodulation Distortion[2,4]								
F = 4.88MHz (−6dB) 4.65MHz (−6dB)	F_S = 10MHz		−70.5			•		dBC
F = 2.40MHz (−6dB) 2.25MHz (−6dB)	F_S = 5MHz		−74.5			•		dBC
Signal-to-Noise and Distortion (SINAD) Ratio								
F = 4.8MHz (0dB)	F_S = 10MHz		66.8			•		dB
F = 0.58MHz (0dB)			68.6			•		dB
F = 2.4MHz (0dB)	F_S = 5MHz		67.2			•		dB
F = 0.58MHz (0dB)			69			•		dB
Aperture Time			6			•		ns
Aperture Jitter			5			•		ps RMS
Analog Input Bandwidth								
Small Signal	-20dB input		70			•		MHz
Full Power	0dB input		40			•		MHz
OUTPUTS								
Logic Family			ECL with pull-down to $-V_{DD2}$ (see text)					
Logic Coding			Offset Binary, Twos Complement					
Logic Levels	Logic "LO"		−1.7			•		V
	Logic "HI"		−0.9			•		V
EOC Delay Time	Data Out to DV	5	35		•	•		ns
Tr and Tf	20% to 80%		5			•		ns
Data Valid Pulse Width	50%	5	8		•	•		ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	•	•	•	V
$-V_{CC}$		−14.25	−15	−15.75	•	•	•	V
V_{DD1}		+4.75	+5	+5.25	•	•	•	V
V_{DD2}		−4.95	−5.2	−5.46	•	•	•	V
Supply Currents, $+V_{CC}$	Operating		75			•		mA
$-V_{CC}$			45			•		mA
V_{DD1}			400			•		mA
V_{DD2}			900			•		mA
Power Consumption	Operating		6.5			•		W

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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

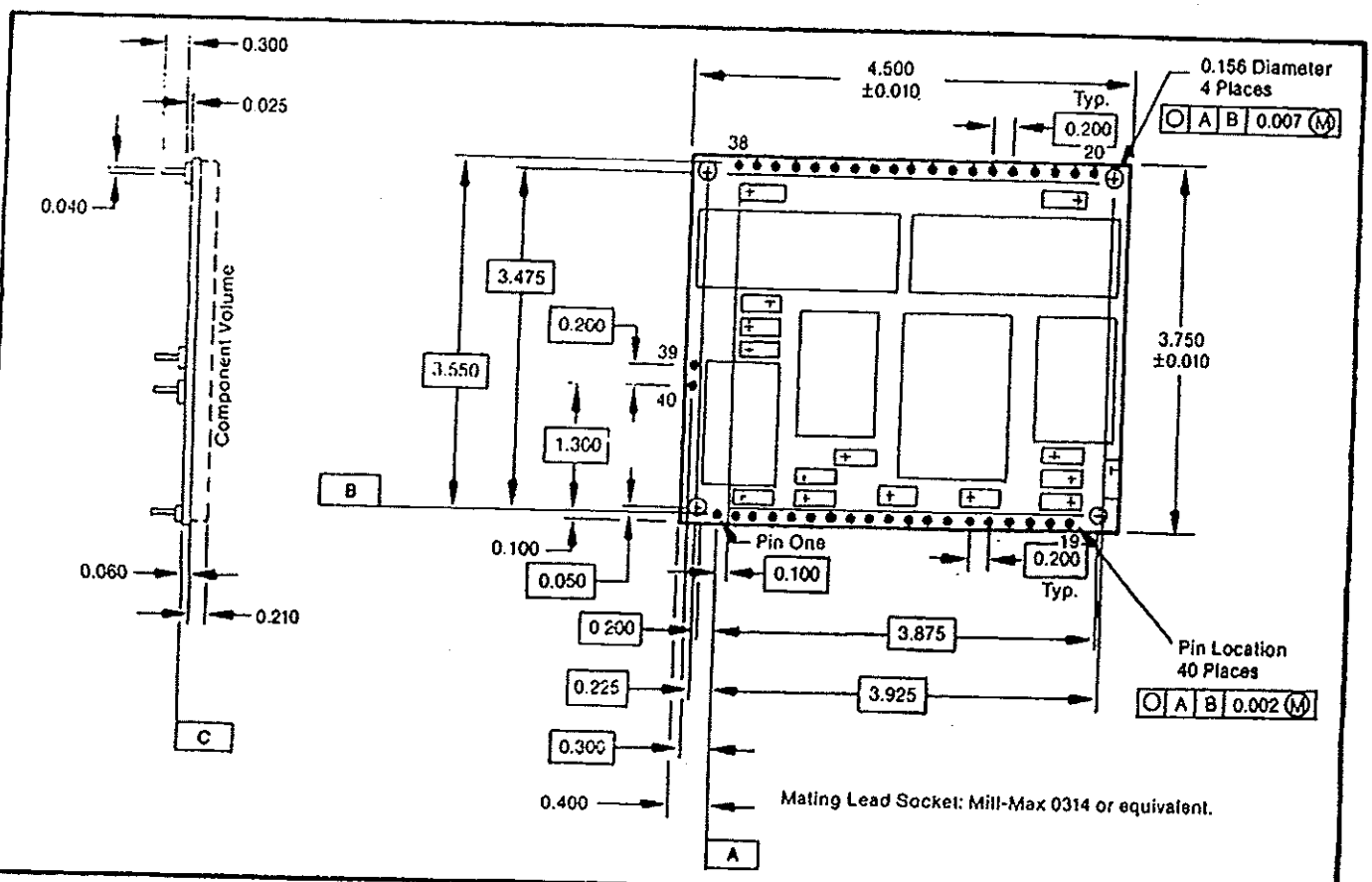
V_{CC} = ±15V, V_{OD1} = +5V, V_{OD2} = -5.2V, R_S = 50Ω, 15-minute warmup, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	ADC600K MIN	ADC600K TYP	ADC600K MAX	ADC600B MIN	ADC600B TYP	ADC600B MAX	UNITS
TEMPERATURE RANGE								
Specification	T_{CASE} max	0		+70	−25		+85	°C
Storage	$T_{AMBIENT}$	−40		+100	*		*	°C
ACCURACY								
Gain Error	F = 200Hz		±30			*		ppm/°C
Input Offset	DC		±50			*		µV/°C
Integral Linearity Error	F = 200Hz			1.5			*	LSB
Differential Linearity Error	F = 200Hz							
	63% of all codes			0.5			*	LSB
	98% of all codes			1.25			*	LSB
	100% of all codes			1.5			*	LSB
Sample Rate		DC		10	*		*	MHz

*Same as ADC600K

NOTE: (1) FSR: full-scale range = 8.6Vp-p. (2) Units with tested and guaranteed distortion specifications are available on special order—inquire. (3) dBC = level referred to carrier (input signal = 0dB); F = input signal frequency; F_S = sampling frequency. (4) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (= 0dB), the intermodulation products will be 6dB lower.

MECHANICAL



ABSOLUTE MAXIMUM RATINGS

V_{CC}	±16.5V
V_{OD1}	+7.0V
V_{OD2}	−7.0V
Analog Input	±5.0V
Logic Input	V_{OD2} to +0.5V
Case Temperature	100°C
Junction Temperature[1]	150°C
Storage Temperature	−40°C to +100°C

Stresses above these ratings may cause permanent damage to the device.

(1). See Table I for thermal resistance data.

ORDERING INFORMATION

ADC600 X Q

Basic Model Number

Performance Grade Code
K = 0°C to +70°C
B = −25°C to +85°C

Reliability Screening
Q = Q-Screened

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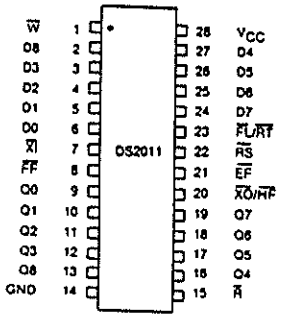
Dallas Semiconductor
2048 x 9 FIFO

DS2011

FEATURES

- First-in, first-out memory based architecture
- Flexible 2048 x 9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 35ns, 50ns, 65ns and 80ns access times
- Industrial temperature range −40°C to +85°C available designated IND

PIN CONNECTIONS



PIN NAMES

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL/RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO/HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground

DESCRIPTION

The DS2011 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full, empty and half-full flags, and unlimited expansion capability in both word size and depth. The main application of the DS2011 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

OPERATION

Unlike conventional shift register based FIFOs, the DS2011 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the DS2011 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

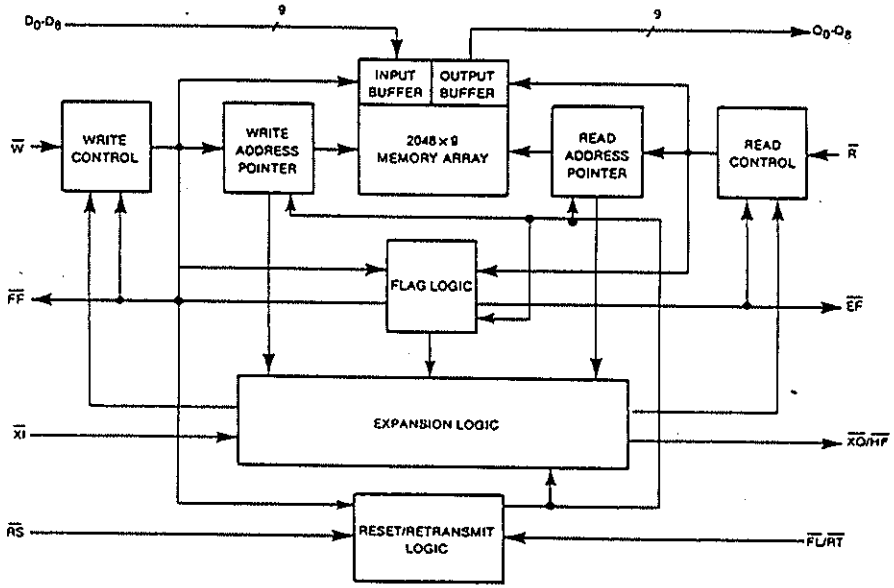
Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 2047. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The DS2011 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the DS2011 allows connecting the read, write, data in, and data out lines of the DS2011 in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins, as appropriate (see the Expansion Timing section for a more complete discussion).

BLOCK DIAGRAM Figure 1



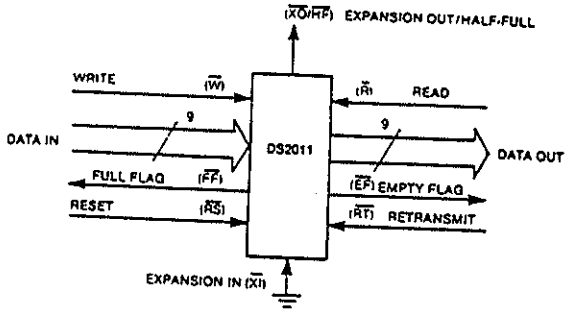
SINGLE DEVICE CONFIGURATION

A single DS2011 may be used when application requirements are for 2048 words or less. The DS2011 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 2).

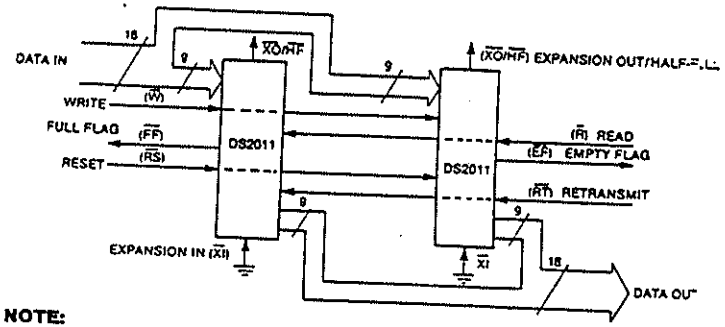
WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 3 demonstrates an 18-bit word width by using two DS2011s. Any word width can be attained by adding additional DS2011s.

A SINGLE 2048 x 9 FIFO CONFIGURATION Figure 2



A 2048 x 18 FIFO CONFIGURATION (WIDTH EXPANSION) Figure 3



NOTE:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

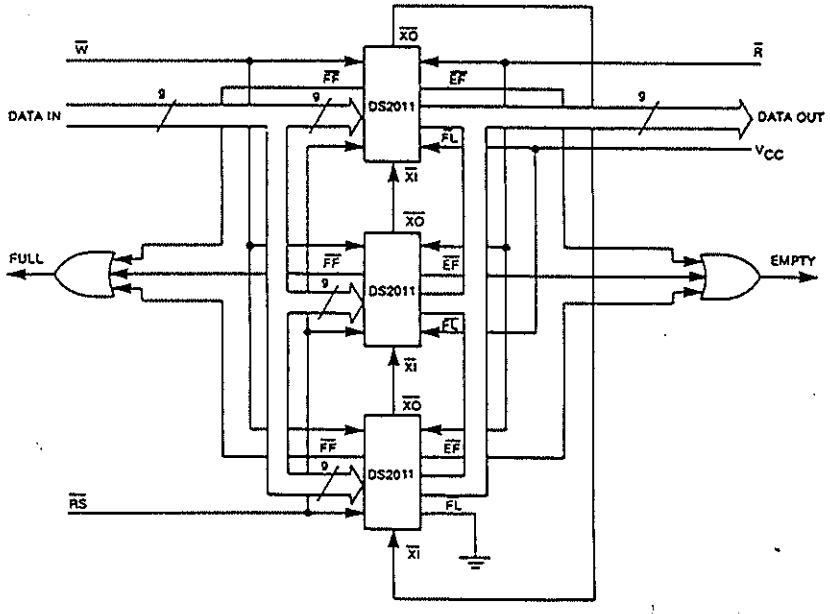
The DS2011 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 4 demonstrates Depth Expansion using three DS2011s. Any depth can be attained by adding additional DS2011s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The DS2011 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The half-full capability is not allowed in depth expansion.

A 6144 x 9 FIFO CONFIGURATION (DEPTH EXPANSION) Figure 4



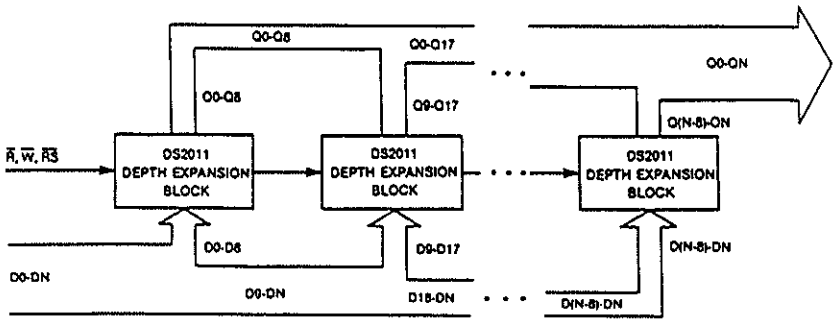
COMPOUND EXPANSION

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 5).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing DS2011s, as shown in Figure 6. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

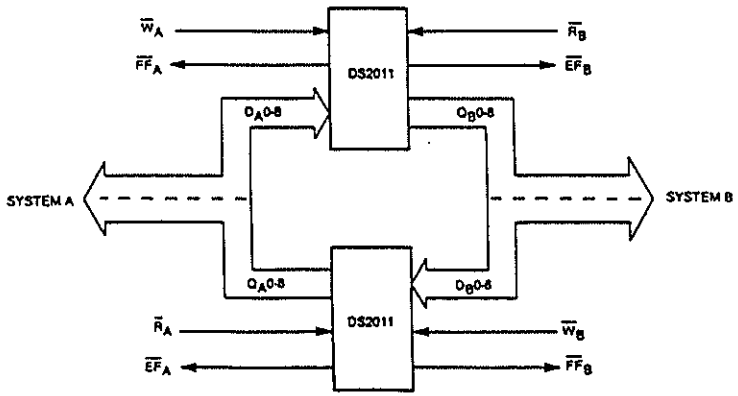
COMPOUND FIFO EXPANSION Figure 5



NOTES:

1. For depth expansion block see DEPTH EXPANSION section and Figure 4.
2. For flag operation see WIDTH EXPANSION section and Figure 3.

BIDIRECTIONAL FIFO APPLICATION Figure 6



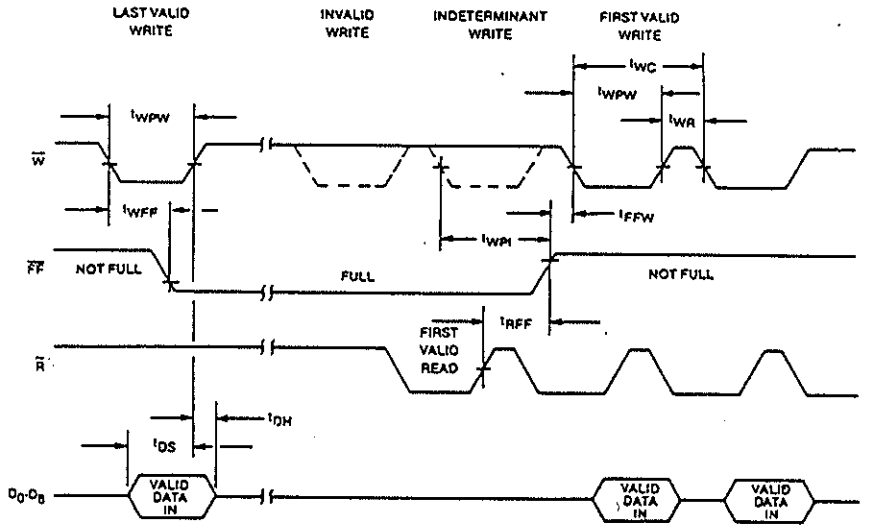
HALF-FULL CAPABILITY

In the single-device and width-expansion modes, the $\overline{XO}/\overline{HF}$ output acts as an indication of a half-full memory. ($\overline{XI}$ must be tied low.) After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain low until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset (forced high) by the rising edge of the read operation.

WRITE MODE

The DS2011 initiates a Write Cycle (see Figure 7) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the DS2011 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

WRITE AND FULL FLAG TIMING Figure 7



WRITE A.C. ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC} = 5.0V ± 10%)

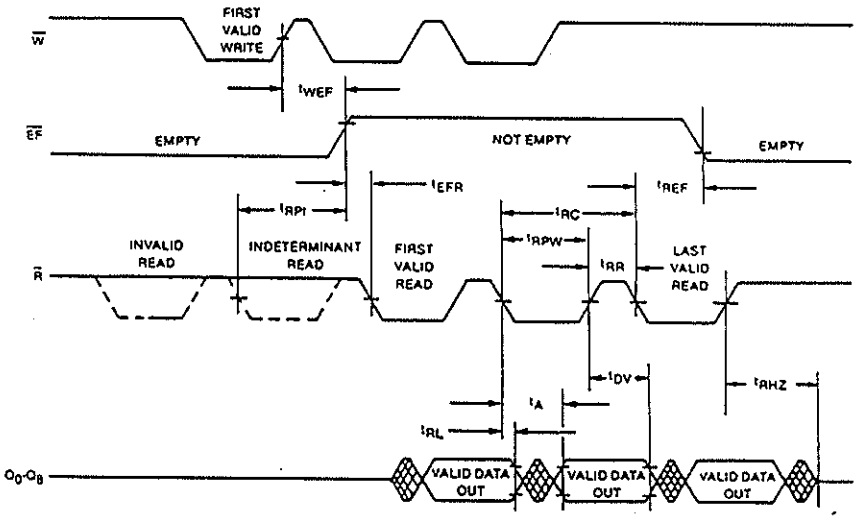
		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Cycle Time	t_{WC}	45		65		80		100		ns	
Write Pulse Width	t_{WPW}	35		50		65		80		ns	1
Write Recovery Time	t_{WR}	10		15		15		20		ns	
Data Set Up Time	t_{DS}	15		20		25		30		ns	
Data Hold Time	t_{DH}	5		5		10		10		ns	
$\overline{W}$ Low to $\overline{FF}$ Low	t_{WFF}		30		45		60		70	ns	2
$\overline{FF}$ High to Valid Write	t_{FFW}		5		5		10		10	ns	2
$\overline{R}$ High to $\overline{FF}$ High	t_{RFF}		30		45		60		70	ns	2
Write Protect Indeterminant	t_{WPI}		15		20		25		25	ns	2

READ MODE

The DS2011 initiates a Read Cycle (see Figure 8) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the DS2011 provides a fast access to data from 9 of 18,432 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

READ AND EMPTY FLAG TIMING Figure 8



READ A.C. ELECTRICAL CHARACTERISTICS

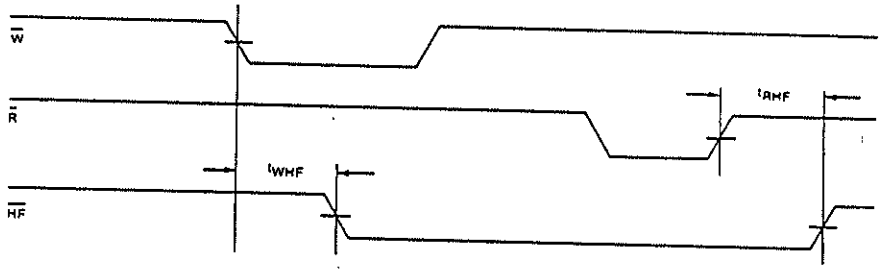
(0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read Cycle Time	t_{RC}	45		65		80		100		ns	
Access Time	t_A		35		50		65		80	ns	2
Read Recovery Time	t_{RR}	10		15		15		20		ns	
Read Pulse Width	t_{RPW}	35		50		65		80		ns	1
$\overline{R}$ Low to Low Z	t_{RL}	5		10		10		10		ns	2
Data Valid from $\overline{R}$ High	t_{DV}	5		5		5		5		ns	2
$\overline{R}$ High to High Z	t_{RHZ}		20		25		25		25	ns	2
$\overline{R}$ Low to $\overline{EF}$ Low	t_{REF}		30		45		60		70	ns	2
$\overline{EF}$ High to Valid Read	t_{EFR}		5		5		10		10	ns	2
$\overline{W}$ High to $\overline{EF}$ High	t_{WEF}		30		45		60		70	ns	2
Read Protect Indeterminant	t_{RPI}		15		20		25		25	ns	2

HALF-FULL MODE

Unlike the Full Flag and Empty Flag, the Half-Full Flag does not prevent device reads and writes. The flag is set by the next falling edge of write when the memory is 1024 locations full. The flag will remain set until the memory is less than or equal to 1024 locations full. The read operation (rising edge), which results in the memory being 1024 locations full, removes the flag.

HALF-FULL FLAG TIMING Figure 9



HALF-FULL FLAG A.C. CHARACTERISTICS

(0°C to +70°C, V_{CC} = 5.0V ± 10%)

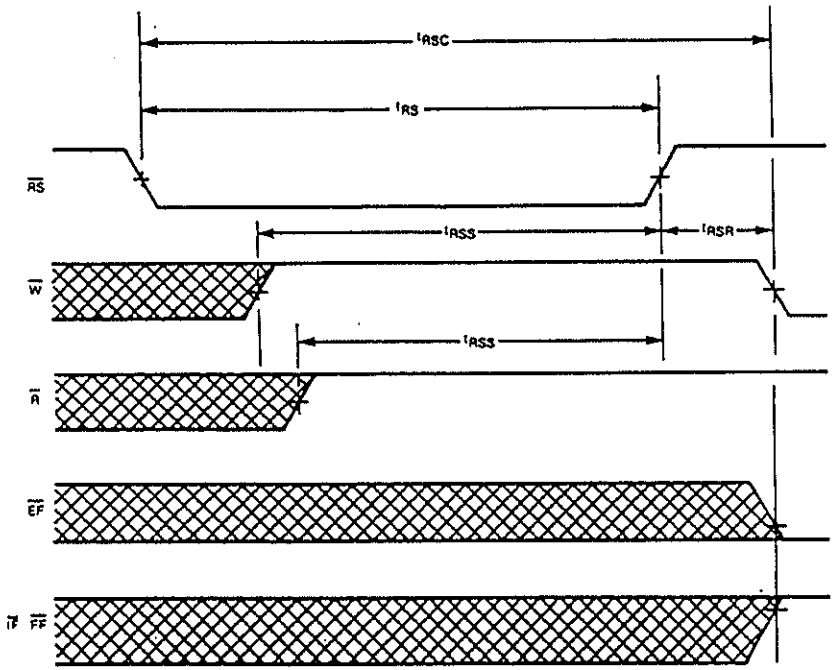
		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write Low to Half-Full Flag Low	t_{WHF}		45		65		80		100	ns	
Read High to Half-Full Flag High	t_{RHF}		45		65		80		100	ns	

RESET

The DS2011 is reset (see Figure 10) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after a power up, before a Write operation can begin.

Although neither $\overline{W}$ nor $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

RESET Figure 10



NOTE:
$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.

RESET A.C. ELECTRICAL CHARACTERISTICS (0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Reset Cycle Time	t_{RSC}	45		65		80		100		ns	
Reset Pulse Width	t_{RS}	35		50		65		80		ns	1
Reset Recovery Time	t_{RSR}	10		15		15		20		ns	
Reset Set Up Time	t_{RSS}	30		40		50		60		ns	

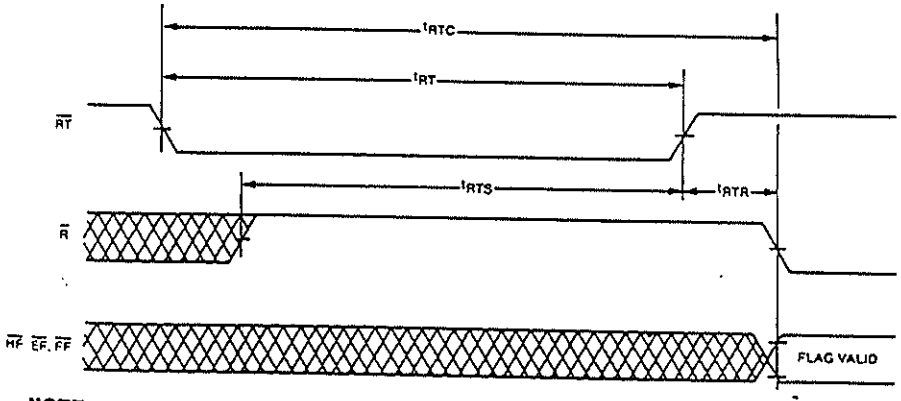
RETRANSMIT

The DS2011 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low (see Figure 11).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

RETRANSMIT Figure 11



NOTE:
$\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

RETRANSMIT
A.C. ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Retransmit Cycle Time	t_{RTC}	45		65		80		100		ns	
Retransmit Pulse Width	t_{RT}	35		50		65		80		ns	1
Retransmit Recovery Time	t_{RTR}	10		15		15		20		ns	
Retransmit Set Up Time	t_{RTS}	30		40		50		60		ns	

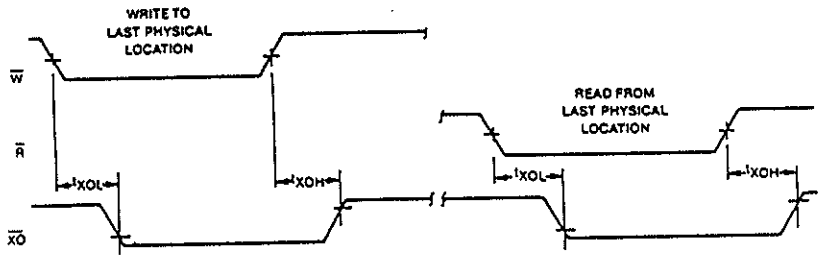
EXPANSION TIMING

Figures 12 and 13 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

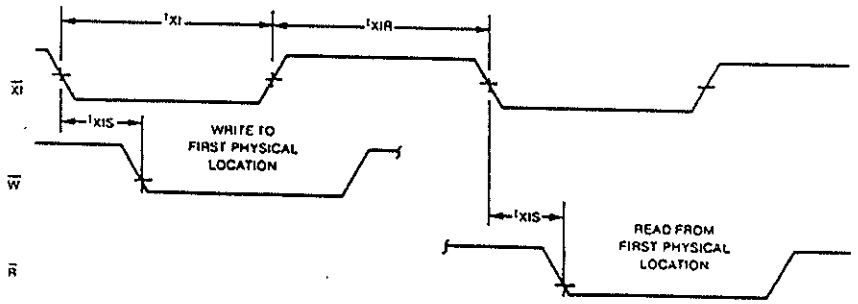
Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

When in Depth Expansion mode, a given DS2011 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A DS2011 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

EXPANSION OUT TIMING Figure 12



EXPANSION IN TIMING Figure 13



EXPANSION LOGIC
A.C. ELECTRICAL CHARACTERISTICS

(0°C to +70°C, V_{CC} = 5.0V ± 10%)

		DS2011-35		DS2011-50		DS2011-65		DS2011-80			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Expansion Out Low	t_{XOL}		30		45		55		70	ns	
Expansion Out High	t_{XOH}		30		45		55		70	ns	
Expansion In Pulse Width	t_{XI}	35		50		65		80		ns	1
Expansion In Recovery Time	t_{XIR}	10		15		15		20		ns	
Expansion In Set Up Time	t_{XIS}	15		20		25		30		ns	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin relative to Ground -0.5V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C
Total Device Power Dissipation 1 Watt
Output Current per Pin 20 mA

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Ground	GND		0		V	
Logic "1" Voltage All Inputs	V_{IH}	2.0		$V_{CC}+0.3$	V	3
Logic "0" Voltage	V_{IL}	−0.3		+0.8	V	3,4

D.C. ELECTRICAL CHARACTERISTICS (0°C to 70°C) (V_{CC} = 5.0 volts ± 10%)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current (Any Input)	I_{IL}	−1	1	uA	5
Output Leakage Current	I_{OL}	−10	10	uA	6
Output Logic "1" Voltage I_{OUT} = −1 mA	V_{OH}	2.4		V	3
Output Logic "0" Voltage I_{OUT} = 4 mA	V_{OL}		0.4	V	3
Average V_{CC} Power Supply Current	I_{CC1}		120	mA	7
Average Standby Current ($\overline{R}$ = W = $\overline{RST}$ = FL/$\overline{RT}$ = V_{IH})	I_{CC2}		8	mA	7
Power Down Current (All Inputs = V_{CC} − 0.2V)	I_{CC3}		2	mA	7

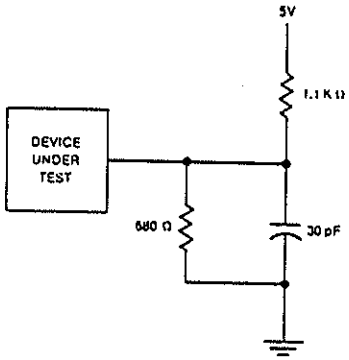
CAPACITANCE (t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Capacitance on Input Pins	C_I	7	pF	
Capacitance on Output Pins	C_O	12	pF	8

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to Ground.
4. −1.5 volt undershoots are allowed for 10ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.

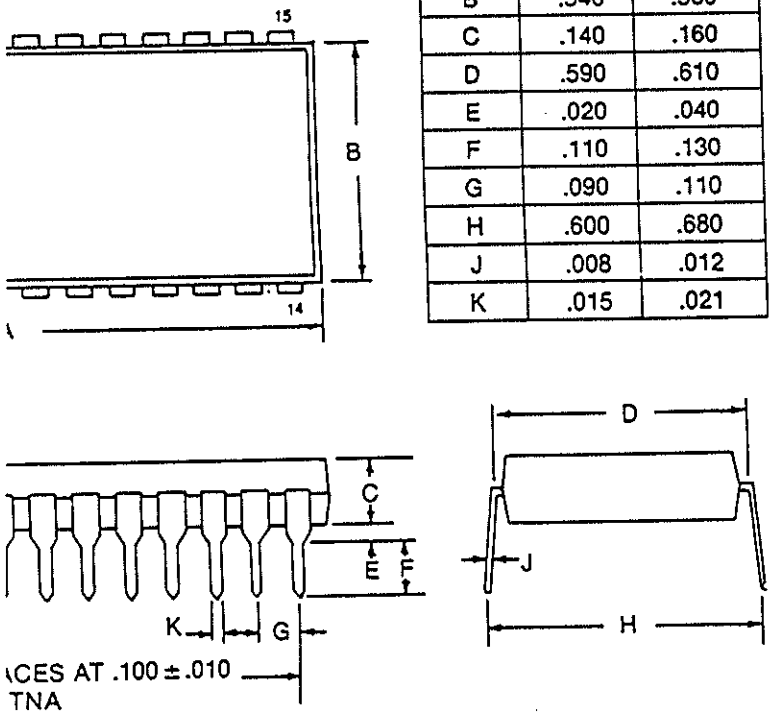
OUTPUT LOAD Figure 14



A.C. TEST CONDITIONS:

Input Levels ..... GND to 3.0 V
Transition Times ..... 5 ns
Input Signal Timing Reference Level ..... 1.5 V
Output Signal Timing Reference Level .. 0.8 V and 2.2 V
Ambient Temperature ..... 0°C to 70°C
V_{CC} ..... 5.0 V ± 10%

28 PINS Figure 15



DIM.	INCHES	
	MIN.	MAX.
A	1.440	1.480
B	.540	.560
C	.140	.160
D	.590	.610
E	.020	.040
F	.110	.130
G	.090	.110
H	.600	.680
J	.008	.012
K	.015	.021

(47)

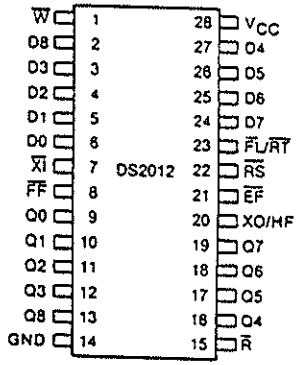
Dallas Semiconductor
4096 x 9 FIFO

PRELIMINARY
DS2012

FEATURES

- First-in, first-out memory based architecture
- Flexible 4096 x 9 organization
- Low power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- High performance
- Available in 50ns, 65ns and 80ns access times
- Industrial temperature range −40°C to +85°C available designated IND
- Military temperature range −55°C to +125°C available designated MIL

PIN CONNECTIONS



PIN NAMES

$\overline{W}$	- WRITE
$\overline{R}$	- READ
$\overline{RS}$	- RESET
$\overline{FL}/\overline{RT}$	- First Load/Retransmit
D_{0-8}	- Data In
Q_{0-8}	- Data Out
$\overline{XI}$	- Expansion In
$\overline{XO}/\overline{HF}$	- Expansion Out/Half Full
$\overline{FF}$	- Full Flag
$\overline{EF}$	- Empty Flag
V_{CC}	- 5 Volts
GND	- Ground

DESCRIPTION

The DS2012 implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the DS2012 is as a rate buffer, sourcing and absorbing data at different rates (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. A half-full flag is available in the single-device and width-expansion configurations. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the WRITEs and READs are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher-density devices. The ninth bit is provided to support control or parity functions.

Refer to DS2011 data sheet for detailed device description.