Manual No. 8609

Copy No.

INSTRUCTION MANUAL

RADAR INTERFACE

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1.0 INTRODUCTION

This manual explains the theory, operation, and testing of the Radar Interface (RI), a peripheral for the Harris data taking computer. The RI, together with the Radar Timing Generator (RTG) and Radar Multiplexer (RMUX), replaces the old Adage Interface and the old timing system. The RI includes four A-to-D converters (12-bit, 10 MHz) with FIFO buffer memories (8K 24-bit words) for on-line data taking. The RI also serves as a general purpose I/O hub providing computer control for up to eight peripheral units including the RTG, the RMUX, and two HP frequency synthesizers.

2.0 RELATED DOCUMENTATION

The manuals for the RI's companion units are listed below in 2.1 through 2.5. References 2.6 and 2.7 cover the Harris computers and their DMA channels.

2.1 Radar Timing Generator Instruction Manual (Manual No. 8610), Arecibo Observatory, Electronics Department, 1986.

2.2 Radar Multiplexer Instruction Manual (Manual No. 8611), Arecibo Observatory, Electronics Department, 1986.

2.3 Reference Manual, Input/Output Interface for Slash 6 Digital Computer, Harris Corp., Computer System Div., 1976.

2.4 Apple to RI-232 Converter, Instruction Manual (Manual No. 8801) Arecibo Observatory, Electronics Dept, 1988.

2.5 RS-232 to RI-232 Converter, Instruction Manual (Manual No. 8803) Arecibo Observatory, Electronics Dept, 1988.

2.6 Reference Manual, Input/Output Interface for Slash 6 Systems, Harris Corp., Computer Systems Div., 1977.

2.7 Adage Interface Instruction Manual (Manual No. 8306), Arecibo Observatory, Electronics Dept, 1983 (Describes the earlier system).

3.0 GENERAL DESCRIPTION

3.1 Function

The Radar Interface (RI) provides five functions:

1. It is an analog data acquisition device containing four internal Analog-to-Digital converters. Each of these 12-bit 10 MHz converters is followed by an 8k FIFO (First-In-First-Out) buffer memory. The FIFOs permit taking data continuously at the maximum average input rate of the computer. They also permit burst sampling at rates up to 10 MHz.

2. It provides a parallel input port which can be selected in place of the A-to-D converters to read digital data from an external device (e.g. special processor, etc).

3. It provides computer control via a 5 MHz serial format for up to eight peripheral units such as the Radar Timing Generator (RTG), the Radar Multiplexer (RMUX), HP frequency synthesizers, etc.

4. It contains an IRIG A serial time code decoder which is fed from the station clock.

5. It contains, a counter, the Drifter Monitor, which measures the elapsed time between externally supplied Time Tick and IPP pulses.

Figure 3.1 is the complete block diagram of the RI. Four 12-bit digitizers are triggered in parallel. Each pair of digitizers normally produces a pair of 12-bit words packed into a single 24-bit word. Optionally, one can use only the six MSBs from each digitizer to fill a 24-bit word every two conversions or the four MSBs to fill a word every three conversions, etc. This allows faster rates for continuous sampling and, for burst sampling, effectively lengthens the FIFOs.

MUX Advance and MUX Reset outputs are provided for the RMUX which is an external analog multiplexer whose channel number sequence is programmable.

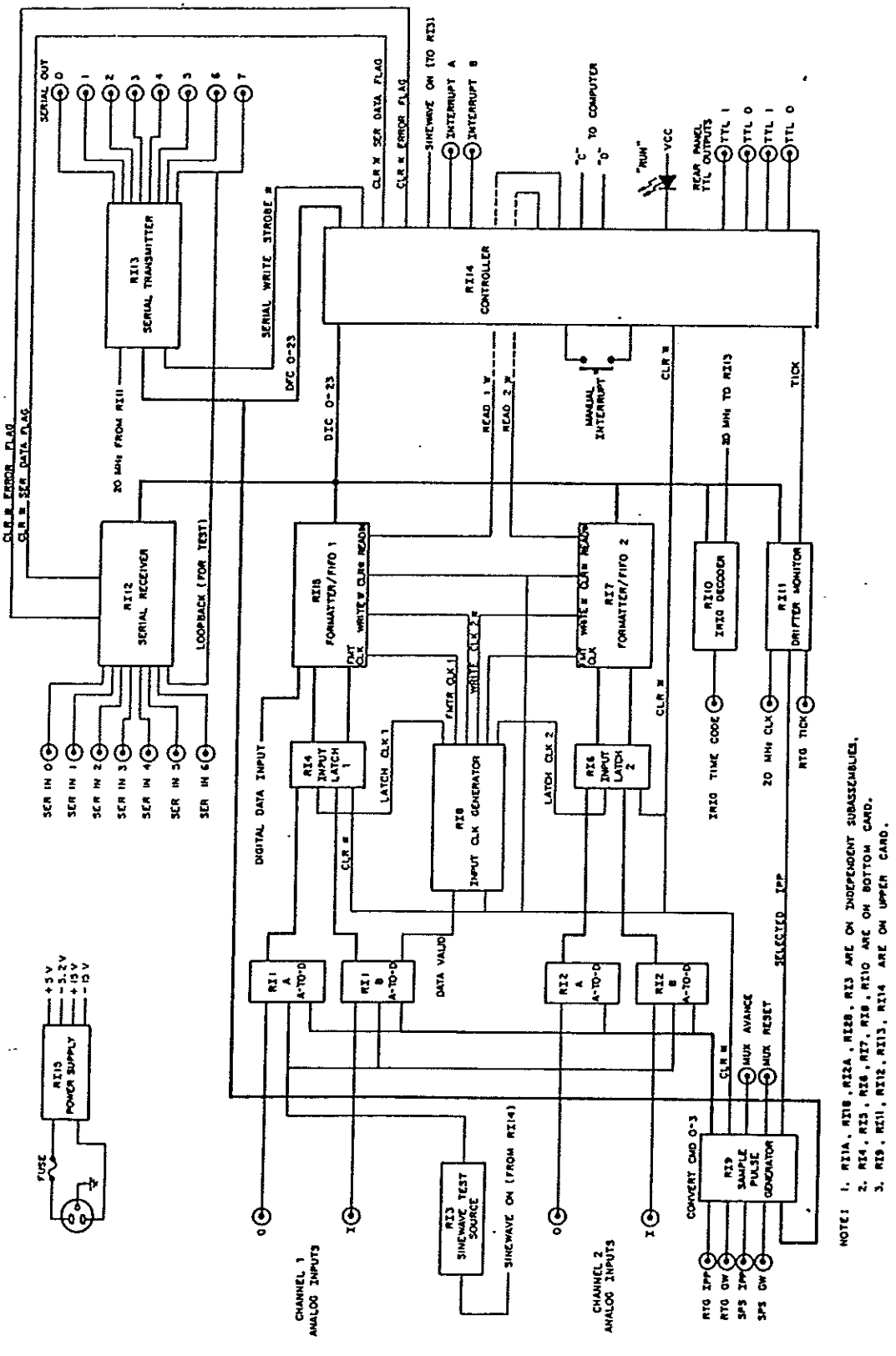

Figure 3.1 RADAR INTERFACE GENERAL BLOCK DIAGRAM

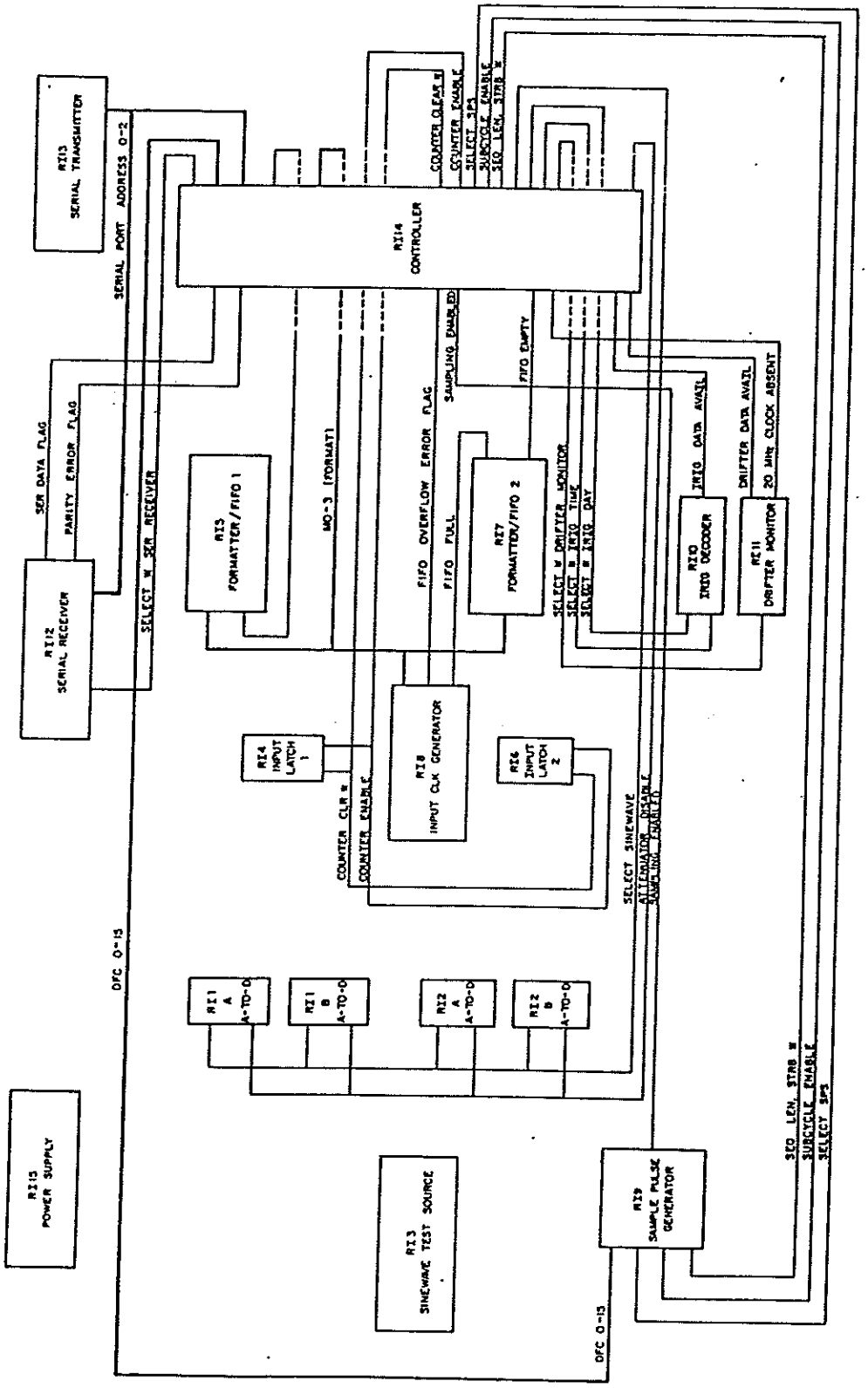

Figure 3.1 RADAR INTERFACE GENERAL BLOCK DIAGRAM (cont.)

3.2 Physical Description

Figure 3.2 shows the front and rear panel views of the Radar Interface. Figure 3.3 shows the relationship between the RI, the RTG, and the RMUX: A set of BNC connectors provides serial control for up to eight peripheral units. A corresponding set of connectors receives serial status information (when available) from these peripherals.

Two BNC connectors are provided for interrupt lines to the computer. Interrupt programming is explained in Section 4.

3.3 The Computer Connection

Communication between the RI and the computer uses the standard Harris protocol: Command words (24-bits) can be sent to the RI and a Status byte can be read from the RI. Data words (24-bit) can be transferred to or from the RI, either as single word transfers (programmed I/O) or as automatic block transfers (Direct Memory Access). Data to the RI include two "Configuration Words" to set sampler and interrupt options. Two dedicated interrupt outputs (with separate BNC connectors) allow the RI to interrupt the Harris at different priority levels.

Since the RI contains a variety of internal registers, it has an internal address pointer, set by the computer through a field in the command word (See table 4.1). The Configuration Words mentioned above are included in these addresses. Data to or from the external peripherals are transferred through the

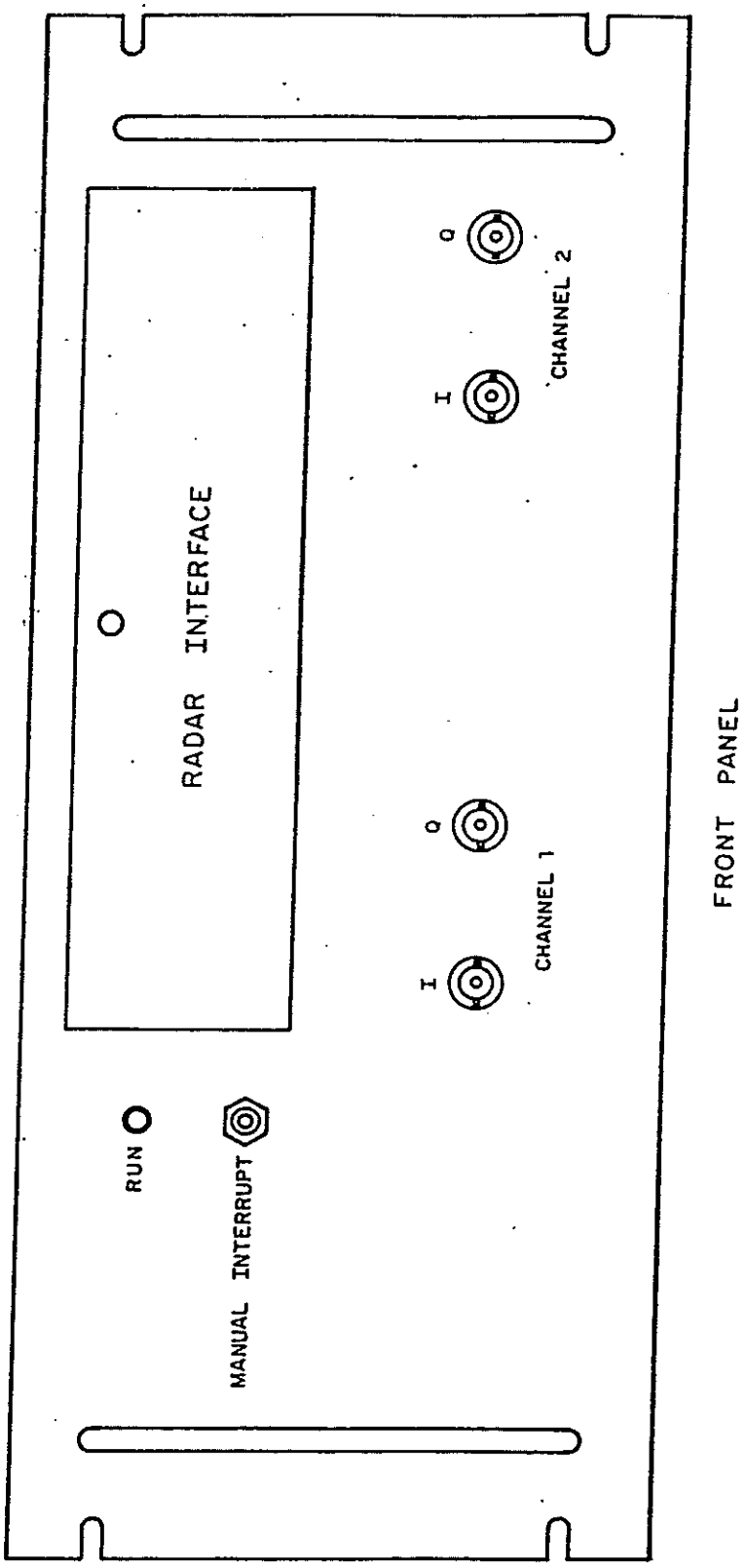

Figure 3.2 Radar Interface Front and Rear Panel Layouts

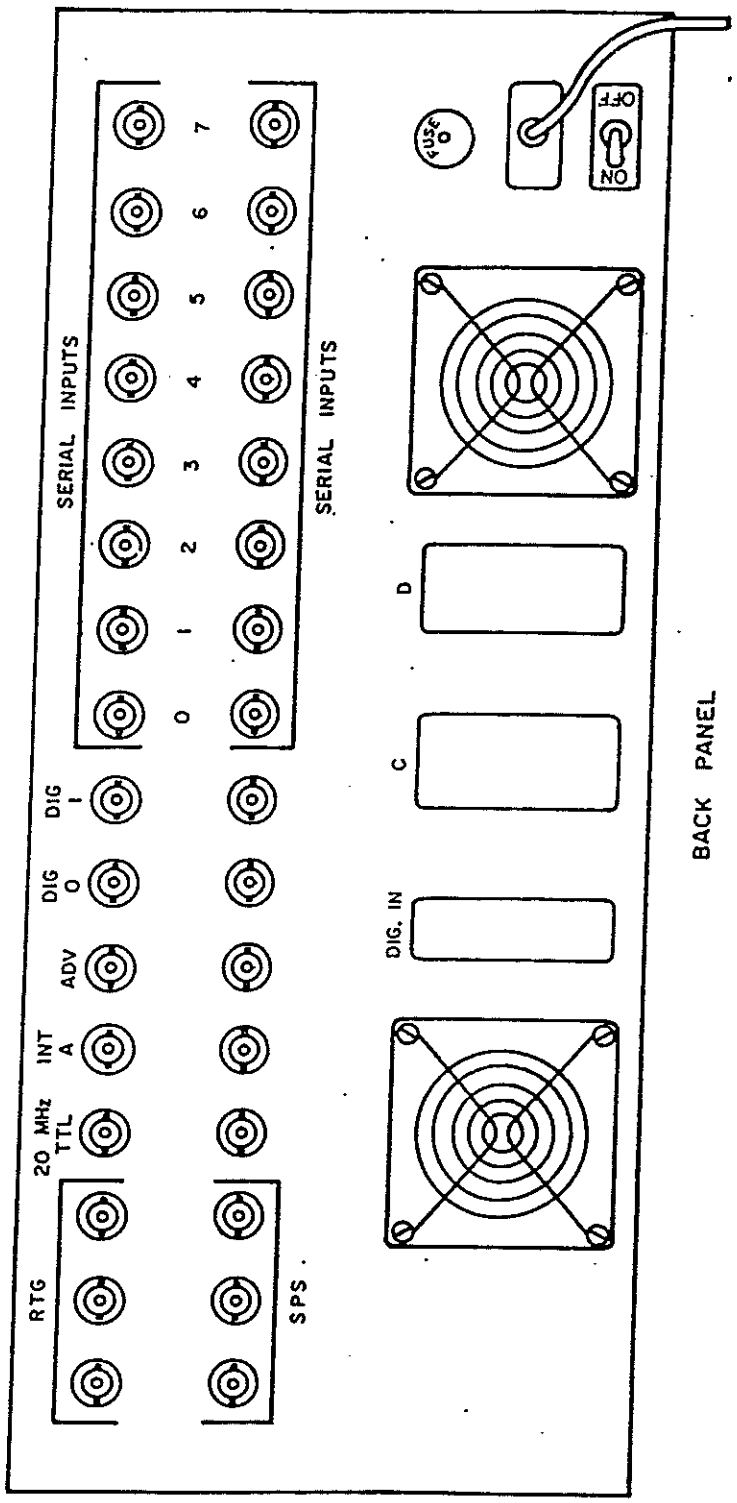

Figure 3.2 Radar Interface Front and Rear Panel Layouts (Cont.)

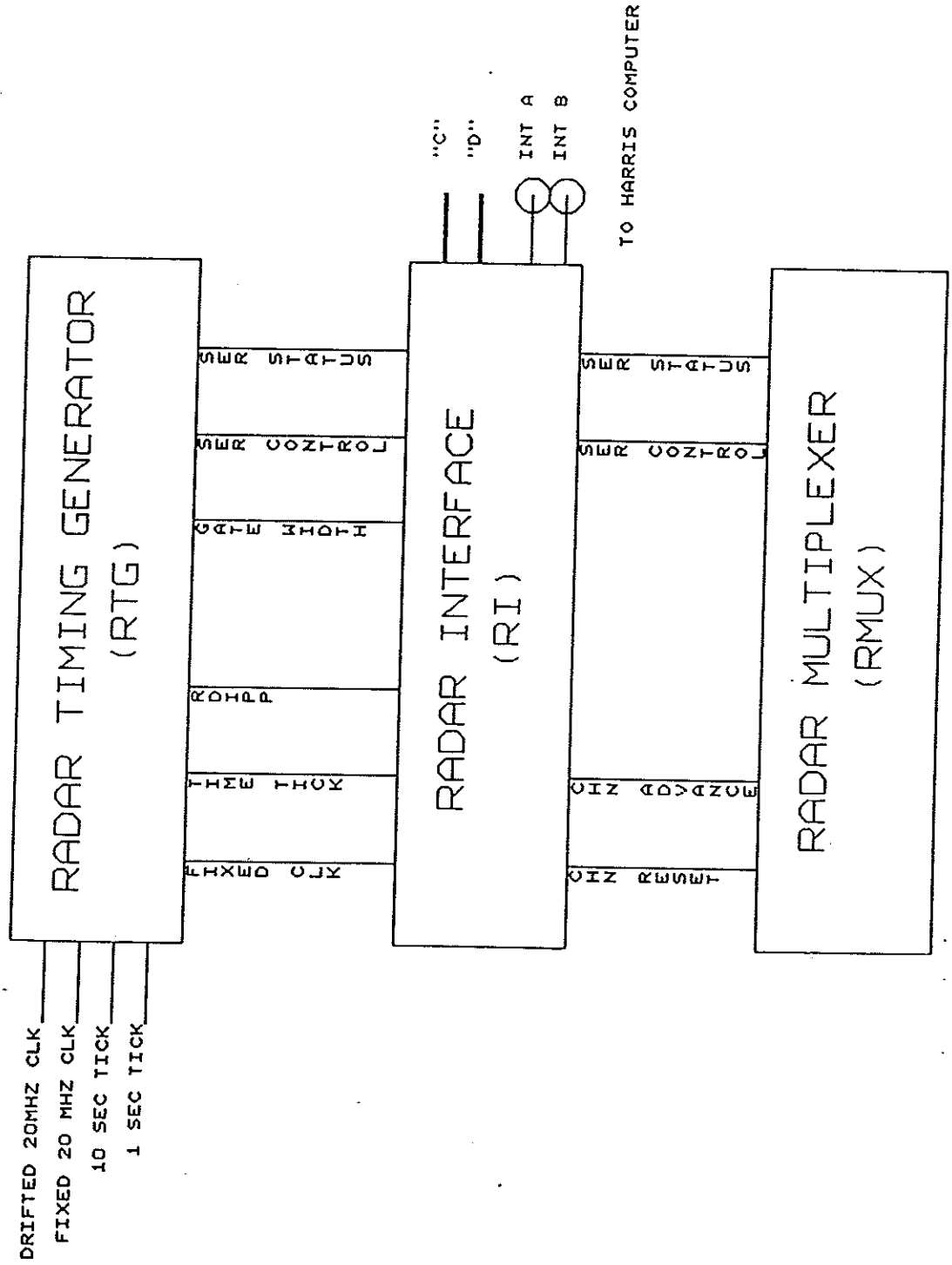

Figure 3.3 Interconnections between RI, RTG, & RMUX

serial or receiver and transmitter (internal addresses 10 and 11). Internal addresses 0, 1, and 2 access the FIFOs, either separately or alternately. When a word is read, the FIFO advances automatically.

3.4 Digitizer Timing and Control

The digitizer control circuitry uses two externally supplied timing signals, the "GW" (Gate Width) and the "IPP" (InterPulse Period), which are nominally the sampler trigger and a trigger enable or start pulse. Two sets of GW and IPP inputs are provided: one set to be connected from the Radar Timing Generator (RTG) and an alternate set from the SPS (Synchronous Programmable Sequencer) or other timing source. The selected set controls all four digitizers simultaneously.

One can enable the RI to begin sampling (i.e. to accept GW pulses) immediately, or one can arm it to be automatically enabled by the next IPP pulse. Once sampling has begun, the formatter assembles the digitizer output into 24-bit words which are clocked into the FIFO buffer memories. Typical data-taking methods are discussed below in 3.5, 3.6, and 3.7..

3.5 Pulse Radar Data-Taking

To emulate Adage data taking, one sends a single command word before each IPP that (1) clears the samplers, (2) arms the samplers to be enabled at the next IPP, and (3) sets up a block transfer from the appropriate FIFO address.

Note: For each IPP the channel has advance notice of the word count but the RI does not and it continues to present data even after the count is met. This unwanted data will not displace good data; when the FIFO fills, sampling is disabled. The FIFO is automatically cleared when sampling is restarted.

3.6 Continuous Sampling

To sample continuously, one begins as above with the command word that starts the digitizers and requests the first block of data. Once this first block has been read, it is necessary to continue requesting blocks, checking status whenever possible to know that the FIFO has not overflowed. The command words for the subsequent block reads will have a NOP in the sampler control field to leave the samplers running undisturbed.

Note: The RTG has provision for continuous sampling in that it can be programmed to provide a continuous train of Gate Width pulses (only one IPP pulse occurs; subsequent IPP pulses which would resynchronize the GW train are absent in this mode).

3.7 Using the External Digital Input

A single 24-bit parallel digital input is provided on the rear panel. Bit 16 in the Sampler Configuration Word causes FIFO1 to receive this data rather than the data from digitizer 1a and 1b. The data input is strobed in by the Gatewidth and synchronized by the IPP exactly as in analog data taking.

3.8 Using the Analog Multiplexer

The RMUX is a separate unit but is controlled from the RI. The RMUX contains two 8-to-1 analog multiplexers operating in tandem to select one of 8 port pairs. The RMUX output lines must be externally connected to the RI's analog inputs. A 8K byte memory in the RMUX is preloaded (from the RI) with the desired port pair sequence.

The RI advances the RMUX's sequence pointer when sampling is underway. For this purpose, the RI is preloaded with the MUX cycle length (a field in the configuration word). If the cycle length is one (zero is not allowed), the sequence pointer never advances and the multiplexer selects the port number indicated by the first memory location. If the cycle length is greater than one, the sequence is advanced after every conversion, cycling through the port numbers contained in the first N locations in the RMUX memory. The memory is reset to the first location when sampling begins and after every N sample pulses. The maximum MUX switching rate (for full 12-bit accuracy) is 5 MHz.

3.8.1 Subcycle Sampling

One often wants to sample several analog port pairs simultaneously at each gate width. The RI, like the Adage, can approximate this by executing a fast (5 MHz) subcycle, triggered by each gate width. The length of the subcycle is set through the same MUX cycle length field in the configuration word. At the end of each subcycle the RMUX RESET line is pulsed.

The subcycle is enabled through bit 12 in the Sampler Configuration Word. Note: the programmed gatewidth must be long enough to let the subcycle complete, that is,

Gate Width ≥ (0.2us * subcycle length) + 0.1us.

3.8.2 Filterbank Multiplexers

The RI can be used with multiplexers other than the RMUX. In particular, external filter banks can have built-in multiplexers. These multiplexers can be slaved to the RMUX, i.e. they connect to the RMUX's port number memory. To use these external multiplexers, one simply connects their data cables to the RI front panel in place of the cables from the RMUX and their address lines to the port number (address lines) outputs provided on the RMUX.

3.9 Drifter Monitor

This counter measures the time from each time tick to the next IPP. The IPP stops the counter and transfers the total into a register, from which it can be read by the computer. In order to read the count, a command word is first sent to select internal address 4, the Drifter Monitor. The tick-to-IPP time is given in units of 0.25 microseconds. The maximum count that does not overflow the 24-bit word is 2.097151 seconds.

3.10 IRIG A Decoder

The RI receives a serial time code, IRIG A, from the station clock (J4 on the rear panel of the EECO clock). This code enters a shift register whose parallel contents are then automatically transferred into two registers which can be read by the computer. Updates occur every 0.1 second. In order to read the time, a command word is first sent to select internal address 3 or 4, the IRIG receiver registers. Address 3 supplies HHMMSS in six BCD fields. Address 4 supplies DDDXXT, day of year and tenths of seconds, in four BCD fields.

4.0 SOFTWARE REQUIREMENTS

TABLE 4.1 Command Word Bit Assignments

Bit(s)	Description
23,22	**DMA Control** 0,1: NOP 2: Start Block Transfer to Computer 3: Start block Transfer from computer
21	Unassigned
20	0: NOP 1: Clear (*)
19,18,17	**SAMPLER CONTROL** 0,2,5: NOP 1,3: STOP; disable & disarm samplers (mostly for test). 4: ARM SAMPLER; disable sampling & clear (*) sampler, then arm sampler to be enabled by the next IPP. 6: ENABLE SAMPLER; clear (*) and immediately enable sampler (enable GW input). 7: SOFTWARE GATE WIDTH; clear (*) and immediately generate one internal gatewidth pulse to trigger the digitizers. If the subcycle mode is enabled many samples will be digitized.
16,15	**INTERRUPT FLAG CLEAR** 0: NOP 1: Clear interrupt B flag 2: Clear interrupt A flag 3: Clear both interrupt flags

TABLE 4.1 Command Word Bit Assignments (cont.)

Bit(s)	Description
14,13	**INTERRUPT A ENABLE** 0: NOP 1: Arm interrupt A (see table 4.3). 2: Disarm interrupt A 3: Trigger interrupt A (software interrupt for test) Note: software interrupt must first be selected (see Table 4.3).
12,11	**INTERRUPT B ENABLE** 0: NOP 1: Arm interrupt B (see table 4.3). 2: Disarm interrupt B 3: Trigger interrupt B (software interrupt for test) Note: software interrupt must first be selected (see Table 4.3).
10	**CLEAR SERIAL DATA FLAG IN STATUS BYTE** 0: NOP 1: Clear serial data flag
09	**CLEAR ERROR FLAGS IN STATUS BYTE & AUX STATUS WORD** 0: NOP 1: Clear flags
08	**CHANGE INTERNAL ADDRESS POINTER** 0: NOP 1: Select Internal Address specified by bits 07-04

TABLE 4.1 Command Word Bit Assignments (cont.)

Bit(s)	Description
7,6,5,4	**INTERNAL ADDRESS SELECTION** 0: FIFO 1 (read only) 1: FIFO 2 (read only) 2: FIFO1 & FIFO2 alternating (read only) 3: IRIG BCD time code HHMMSS (read only) 4: IRIG BCD Time code DDDXXT Day of Year & tenths of seconds (read only) 5: Drifter Monitor (read only) 6: Auxiliary Status Word (read) 7: Interrupt Configuration Word (write only) 8: Sampler Configuration Word (read/write) 9: MUX Sequence length (write only) 10: Serial Receiver (read only) 11: Serial Transmitter (write only) 12: Rear Panel Digital TTL Outputs (Data Bits 0-3)
3	**PERIPHERAL PORT ADDRESS STROBE** 0: NOP 1: Select Peripheral Port specified by bits 2-0
2,1,0	**PERIPHERAL PORT ADDRESS** 0: Port 0, normally connected to HP Synthesizer 0 1: Port 1, normally connected to HP Synthesizer 1 2: Port 2, normally for the Radar Timing Generator 3: Port 3, normally for the Radar Multiplexer 4-7 spare ports.

(*) Clear = disable sampling, clear the FIFOs, reset the RMUX, reset format sequence counter, reset test counter, reset overflow flag, reset FIFO1/FIFO2 readout distributor to FIFO1.

TABLE 4.2 Sampler Configuration Word Bt Assignments

Bit(s)	Description
23	**TIMING SOURCE** 0: RTG (Radar Timing Generator) 1: SPS (Synchronous Programmable Sequencer) or External GW & IPP
22	**SINEWAVE TEST** 0: Normal sampling configuration 1: Samplers connected to internal sinewave source
21,20	Unassigned
19	**ANALOG ATTENUATORS AT DIGITIZERS INPUTS** 0: Attenuators in (Full Scale = +/-5v) 1: Attenuators out (Full Scale = +/-1.25v)
18,17	**FORMATTER & FIFO TEST** 0: Normal sampling; formatters receive data from digitizers. 2: Staircase test: formatters are fed with increasing digital numbers (numbers are in bit-reversed format most significant bit changes faster). 1,3: Zero test: formatters are fed with all zeros
16	**ENABLE DIGITAL INPUT PORT** 0: Normal Analog Sampling: FIFOs receive data from formatters. 1: FIFO1 receives data from external digital source. FIFO2 still receives data from formatters I2 & Q2.

TABLE 4.2 Sampler Configuration Word Bit Asignments (cont.)

Bit(s)	Description

15,14,13 **PACKING FORMAT** (applies to both sampler units)

Format	Step size w/o atten. (±1.25V FS)	Step size w/atten. (±5V FS)
7: Single 12-bit (I only, sign extended to 24bits)	.610 mV	2.44 mV
5: Dual 12-bit (I & Q, each 12 bits)	.610 mV	2.44 mV
4: Dual 6-bit (2 samples each of I & Q)	39.1 mV	156 mV
3: Dual 4-bit (3 samples each of I & Q)	156 mV	625 mV
2: Dual 3-bit (4 samples each of I & Q)	312 mV	1.25 V
1: Dual 2-bit (6 samples each of I & Q)	625 mV	2.5 V
0: Dual 1-bit (12 samples each of I & Q)	Polarity only	Polarity only

12 **SUBCYCLE ENABLE**

0: Every gate width pulse produces one sample trigger (pair mode)

1: Every gate width pulse starts a sampling subcycle. Samples are spaced by 0.2 microsecond. For a sequence of N samples, the sequence length word must be set to N-1.

11-0 Serve no internal function but are loaded together with bits 12-23.

Note: The entire Sampler Configuration Word can be read back to the computer to verify the 24-bit two-way connection with the computer.

TABLE 4.3 Interrupt Configuration Word Bit Assignments

Bit(s)	Description
7,6,5	**INTERRUPT A TRIGGER SOURCE** 0,6,7: No Interrupt 1: WCC (Word Count Complete - looped back to computer) 2: IPP (from RTG, SPS or External as selected (see Table 4.2) 3: Time Tick from RTG (1 sec. or 10 sec.) 4: Front Panel Push Button 5: Software Interrupt (triggered by Command Word Bits 13,14)
4	**INTERRUPT A FORMAT** (level or pulse) 0: Interrupt signal is a one microsecond pulse and is retriggerable. Status flag stays HI until reset by a command word. 1: Interrupt signal to computer is identical to the interrupt flag. The trigger sets it HI and it remains HI until reset by a command word.
3,2,1	**INTERRUPT B TRIGGER SOURCE** 0,6,7: No Interrupt 1: WCC (Word Count Complete - looped back to computer) 2: IPP (from RTG, SPS or External as selected (see Table 4.2) 3: Time Tick from RTG (1 sec. or 10 sec.) 4: Front Panel Push Button 5: Software Interrupt (triggered by Command Word Bits 13,14)
0	**INTERRUPT B FORMAT** (level or pulse) 0: Interrupt signal is a one microsecond pulse and is retriggerable. Status flag stays HI until reset by a command word. 1: Interrupt signal to computer is identical to the interrupt flag. The trigger sets it HI and it remains HI until reset by a command word.

TABLE 4.4 Status Byte Bit Assignments

Bit(s)	Description
7	Always 1
6	Serial data Parity Error Flag (error has occurred on serial input)
5	Serial Data Flag (word has been received from the peripheral currently addressed)
4	Sampling is enabled
3	FIFOs are empty
2	FIFO overflow flag (resets automatically at sampling start)
1	Timing error flag
0	20 Mhz clock present

TABLE 4.5 Auxiliary Status Word Bit Assignments

Bit(s)	Description
23	+5 Overvoltage Error Flag (above 5.25 V)
22	+5 Undervoltage Error Flag (below 4.75 V)
21	-5.2 Overvoltage Error Flag (above -4.9 V)
20	-5.2 Undervoltage Error Flag (below -5.5 V)
19	+15 Overvoltage Error Flag (over 16 V)
18	+15 Undervoltage Error Flag (below 14 V)
17	-15 Overvoltage Error Flag (above -14 V)
16	-15 Undervoltage Error Flag (below -16 V)
15	Interrupt flag B
14	Interrupt flag A

5.0 SPECIFICATIONS

5.1 Analog Inputs

No. of Inputs	4 (2 pairs)
Sampling Rate	0 to 10 Megasamples/second
Dynamic Range	12,6,4,3,2,or 1 bits
Converter Code	Two's Complement
Full Scale Voltage	+/- 5V or +/- 1.25V
Input Impedance	8K ohms (5V scale), or 2K ohms (1.25V scale)
Data Format	See Figure 4.1
Buffer Memories	Two 24-bit x 8k FIFOs (The computer can read either a. from a single FIFO, or b. alternate words from alternate FIFOs.)
Analog Test Source	A built-in 1 volt (peak) sine wave at 460.8 KHz can be selected in place of the front panel inputs to the four digitizers.

5.2 Digital Input

No. of Inputs	1 (24 bits) This port may be selected in place of the digitizers 1a/1b to feed FIFO1.
Test Counters	Four built-in up-counters can be selected in place of the digitizers to provide artificial data to test the formatter/FIFOs. These counters are cleared with the FIFOs when data taking starts. Note: In order to test all formats, these counters are bit reversed, i.e. the normal MSBs in the data words will toggle from one sample to the next.

5.3 Digital Output

4 TTL Bits on rear panel BNC jacks.
(see Table 4.1)

5.4 Serial Control Ports for Peripherals

No. of Port Pairs	8 Tx/Rx pairs (BNC connectors)
Code	Biphase (see Fig 6.1)
Data Rate	5 MBaud (24-bits/4.8 microsec)

5.5 IRIG A Serial Time Code Receiver

Allows the computer to read the EECO clock (station clock) via the Radar Interface. The Time Code Receiver is updated every 0.1 seconds with BCD digits giving seconds, minutes, day of year, and tenths of seconds.

5.6 Drifter Monitor

This counter measures the interval from the time tick input to the next IPP. Both the tick and the IPP are provided externally from the Radar Timing Generator. The count is in units of 0.25 us.

6.0 THEORY OF OPERATION

The overall block diagram, Figure 3.1, together with Sections 3, 4, and 5 of this manual should provide a complete description of the functionality and architecture of the Radar Interface. This section presents block diagrams for the internal modules and discusses the circuitry. The detailed schematic diagrams are found in Section 8.

6.1 & 6.2 Digitizers

Each of the four digitizer modules contains a Burr Brown ADC 600 A-to-D converter (see Sec. 9.1 for data sheets). The Burr Brown converters are mounted in shielded boxes which also contain two relays, one to select the sine wave test source, the other to switch in a 12 dB attenuator. Finally, ECL drivers are provided to send the data and the End-of-Conversion pulse out of the boxes on twisted pairs.

6.3 Sine Wave Test Source

This generator provides a 1 volt (peak) sine wave. The frequency of the sine wave is 460.8 KHz (crystal controlled) and its waveform is filtered for 12-bit accuracy (harmonic content down at least 72 dB).

6.4 & 6.6 Input Latch/Test Counter

These modules contain the ECL-to-TTL converters plus counter/latches made of 74LS161s, which load synchronously (for the latch function) and clear asynchronously (to initialize the test count).

6.5 & 6.7 Formatter/FIFO

Each formatter assembles 24-bit words from its pair of 12-bit digitizer words. In the dual 12-bit mode (see Table 4.2), the formatter simply latches the word pair and passes the data to the FIFO. In the sign-extension mode, the upper 12 bit register

latches the sign bit (MSB) of the lower 12 bits. Finally, when six or fewer bits are used, the formatter acts as a series of latches, triggered one after the other until the two 12-bit halves are filled with sequential samples. (Actually, the latch is reconfigured as an n-wide shift register with parallel clocking).

The FIFO chips use internal dual-port RAMs so that input and output can be asynchronous and totally independent. These FIFOs, made by at least six manufacturers, include input and output address pointer registers so the depth of the FIFO does not affect the pinout. Currently these FIFOs are available in depths up to 4K. When deeper FIFOs are available, they can be plugged in without modifying the unit.

6.8 Input Clock Generator

This module delays the End of Conversion pulse from one of the digitizers (the slowest) to produce the Latch Clocks. It is further delayed to produce the Formatter Clock and The FIFO Clock. The FIFO clock is gated in two ways: first, when shorter than 12-bit words are selected, the FIFOs are clocked only when a packed word has been fully assembled, i.e. every 12/n samples; second, if the FIFO fills up, the FIFO clock is disabled to protect the stored data. When this happens, the FIFO overflow error flag is set HI.

6.9 Sample Pulse Generator/RMUX Controller

The prime function of this module is to take in the TTL convert command (Gate Width) and pass it on as an ECL trigger to the four digitizers. This module also holds off the converter commands to synchronize the start of data taking. Finally, the module contains the sequence length counter and generates multiple sampling pulses for the subcycle mode, as well as the Advance and Reset triggers for the external Radar Multiplexer. This unit is edge triggered by both the IPP and GW inputs.

6.10 IRIG Receiver

The Radar Interface is supplied with a serial time code from the EECO station clock. The format of this code is IRIG A, a NASA standard. A new frame of time data arrives every 1/10 second. Module 10 converts this code to two 24-bit words of six BCD fields, HHMMSS, and DDDXXT (day of year and tenths of seconds). In order that the computer not latch changing data, the DAVFU (Data Available From Unit) line is held low for 2 microseconds before and after the data is transferred from the input shift register (SIPO) to the latch.

6.11 Drifter Monitor

This counter measures elapsed time between the time tick, which always clears the counter, and the IPP pulse, which always loads the accumulated count into an output register. The output register is connected to the RI's DTC (Data to Computer) bus

whenever Internal Address 5 is selected. The tick and IPP pulses fire one-shots so that their widths are unimportant. The two-microsecond pulses from the one-shots then produce 50 nanosecond pulses synchronized to the 4 MHz counter clock to prevent timing ambiguity. The Data Available line from the drifter monitor is LO for 2 microseconds around the IPP pulse so that the computer can't read data while it is changing in the output register.

6.12 Serial Receiver

This module, RI12, selects one of eight serial inputs and converts incoming 24-bit serial words to parallel format. (The serial format is shown in Figure 6.1). Whenever a word is received, the Serial Data Flag goes HI (and remains HI until explicitly reset via bit 10 in the Command Word). The parallel output register is connected to the DTC (Data-to-Computer) bus whenever Internal Address 10 is selected. A parity error flag stays HI until reset by bit 9 in the Command word. The input buffers for the serial data accept TTL levels but are differential amplifiers, able to tolerate up to 5 volts of common mode signal. The serial control and status format is shown in Figure 6.1.

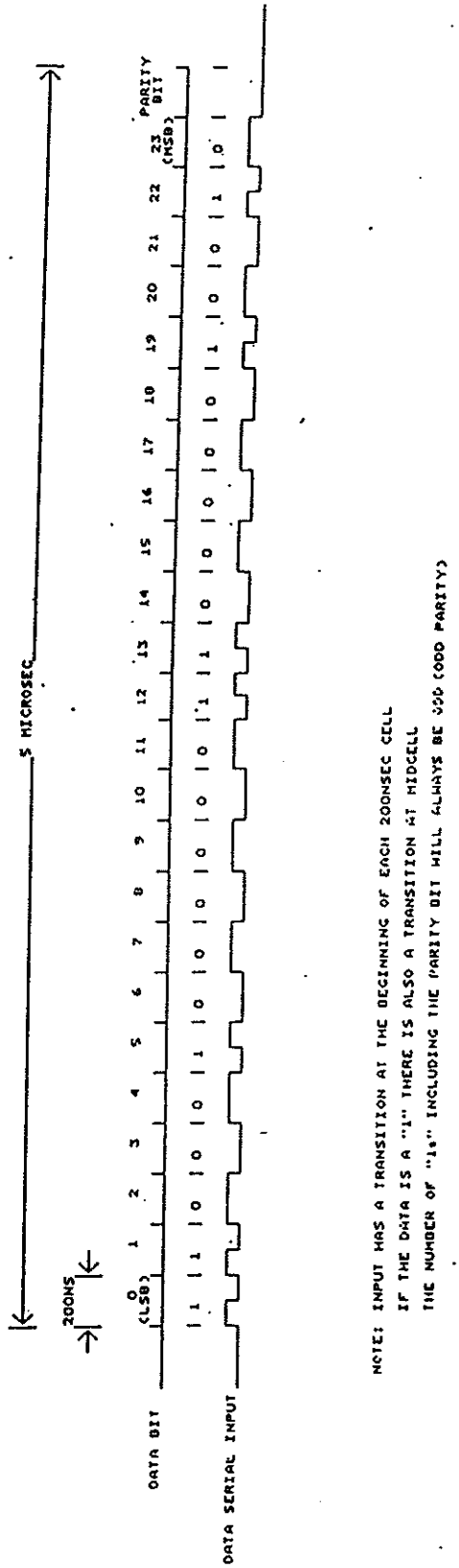

Figure 6.1 Serial Biphase Control Word Format

6.13 Serial Transmitter

This module, RI13, is the companion to the serial receiver. It sends 24-bit serial control words to the selected output port (one-of-eight). The circuit uses an all-synchrounous design and the output ports can drive 50 ohms. A serial word will be transmitted as soon as the computer transfers a data word to the RI (provided, of course, that Internal Address 11 is selected). Handshaking on data words to the RI is delayed 5 microseconds which is the time needed to output a serial control word. This allows a block transfer to send a sequence of control words without overflowing the serial transmitter.

6.14 Control Module

This module is the Radar Interface's own interface. It latches the sampler and interrupt configuration words, the digital output bits, and the serial port address. It provides strobes to latch the sequence length into RI9 and control words into RI13. It also contains the interrupt generator circuit, the power supply monitor, the FIFO output controller, and circuitry to handshake on data words and control words with the computer. Finally this module contains line drivers and receivers to buffer data to and from the Harris computer.

7.0 OPERATIONAL TESTS

This unit has several built-in test provisions by which the computer can check its operation. It is suggested that testing be done in the following order:

7.1 Basic Communications Test

The 24-bit Sampler Configuration Word (SCW) can be read back to verify the operation of the 24 data lines from the computer and the 24 data lines to the computer.

7.2 Power Supply Test

Clear the error flags. Then check that Bits 23-16 of the Aux Status Word are 0. Ones indicate out of range supply voltages (see Table 4.5).

7.3 Serial Data Loop-Back

Serial Input Port 7 is internally connected to Serial Output Port 7, allowing a loop-back test w/o an external cable. (This does make Input Port 7 unavailable for other use, but Port 7 can still be used, for example, to control an HP synthesizer which doesn't return status.) This test exercises all of the Serial RX and Serial TX circuitry except the input and output multiplexers, receivers, and drivers.

7.4 Interrupt Tests

The two interrupt lines to the computer can be tested by first selecting software interrupts in the Interrupt Configuration Word and then triggering the interrupt using the command word. The WCC (Word Count Complete) interrupt can be

tested by reading any block of data, e.g. from the SCW loopback, which always handshakes, or from the FIFOs (which will require Gate Width pulses).

7.5 Formatter/FIFO Tests

The test counters provide deterministic artificial data to verify the formatting/packing and FIFO operation. When this test is selected (via the Sampler Configuration Word), each digitizer is replaced by a 12-bit binary counter. The counters are zeroed automatically at the start of sampling and increment on each sample. Note: the counters are bit-reversed, i.e. the LSB or most radiply changing counter bit appears as the MSB or sign bit in the data. This avoids rounding off the changing bits when testing the modes with fewer than 12 bits. This test can be performed without an external timing source (RTG or SPS) by using the software GW command together with the subcycle mode. If the sequence length is set to 8k, the entire FIFO will be filled with artificial data.

7.6 Digitizer Test

A built-in sinewave generator can be selected in place of the BNC analog input jacks. A block of data is taken (as above in 7.5) and fitted to a theoretical sinewave to check the accuracy of the digitizers. The peak amplitude of the sinewave is 1 volt and the frequency is 460.8 KHz. The digitizers can also be compared against each other.

8.0 PAL SOURCE CODE

Source Code for the two PALs used in the formatters (RI5 and RI7) appears on the following two pages. These PALS are designated RIPAL00 and RIPAL01 and are built with generic 20R6 and 20R8 chips.

8.1 RIPAL00

```
Title     source code for Ripal00, the formatter for
          bits 0-3
Pattern   ripal00
Revision  01
Author    Jon Hagen
Company   Arecibo Observatory
Date      11/30/88
;
chip ripal00 pal20r6
;
; pins 1 through 24
;
clk sgni x3 x2 x1 x0 y9 y8 y7 y6 y5 gnd
/oe y4 m2 nc nc y0 y1 y2 y3 m1 m0 vcc
;
; one bit format, two bit format, etc
;
string one      '/m2 * /m1 * /m0'
string two      '/m2 * /m1 *  m0'
string three    '/m2 *  m1 * /m0'
string four     '/m2 *  m1 *  m0'
string six      ' m2 * /m1 * /m0'
string twelve   ' m2 * /m1 *  m0'
string exti     ' m2 *  m1 * /m0'
string extq     ' m2 *  m1 *  m0'
;
equations
/y3 := one * /y4 + two * /y5 + three * /y6 + four * /y7
     + six * /y9 + twelve * /x3 + exti * /x3 + extq *
     /sgni
;
/y2 := one * /y3 + two * /y4 + three * /y5 + four * /y6
     + six * /y8 + twelve * /x2 + exti * /x2 + extq *
     /sgni
;
```

```
/y1 := one * /y2 + two * /y3 + three * /y4 + four * /y5
      + six * /y7 + twelve * /x1 + exti * /x1 + extq *
      /sgni
;
/y0 := one * /y1 + two * /y2 + three * /y3 + four * /y4
      + six * /y6 + twelve * /x0 + exti * /x0 + extq *
      /sgni
```

8.2 RIPAL01

```
Title       source code for Ripal01, the formatter for
            bits 4-11
Pattern     ripal01
Revision    01
Author      Jon Hagen
Company     Arecibo Observatory
Date        11/30/88
;
chip ripal01 pal20r8
;
; pins 1 through 24
;
clk sgni x11 x10 x9 x8 x7 x6 x5 x4 m2 gnd
/oe m1 y4 y5 y6 y7 y8 y9 y10 y11 m0 vcc
;
; one bit format, two bit format, etc
;
string one      '/m2 * /m1 * /m0'
string two      '/m2 * /m1 *  m0'
string three    '/m2 *  m1 * /m0'
string four     '/m2 *  m1 *  m0'
string six      ' m2 * /m1 * /m0'
string twelve   ' m2 * /m1 *  m0'
string exti     ' m2 *  m1 * /m0'
string extq     ' m2 *  m1 *  m0'
;
equations
/y11 := one * /x11 + two * /x11 + three * /x11 + four *
      /x11 + six * /x11 + twelve * /x11 + exti * /x11 +
      extq * /sgni
;
/y10 := one * /y11 + two * /x10 + three * /x10 + four *
      /x10 + six * /x10 + twelve * /x10 + exti * /x10 +
      extq * /sgni
;
/y9  := one * /y10 + two * /y11 + three * /x9  + four *
      /x9  + six * /x9  + twelve * /x9  + exti * /x9  +
      extq * /sgni
;
```

```
/y8   := one * /y9  + two * /y10 + three * /y11 + four *
      /x8  + six * /x8  + twelve * /x8  + exti * /x8  +
      xtq * /sgni
;
/y7   := one * /y8  + two * /y9  + three * /y10 + four *
      /y11 + six * /x7  + twelve * /x7  + exti * /x7  +
      extq * /sgni
;
/y6   := one * /y7  + two * /y8  + three * /y9  + four *
      /y10 + six * /x6  + twelve * /x6  + exti * /x6  +
      extq * /sgni
;
/y5   := one * /y6  + two * /y7  + three * /y8  + four *
      /y9  + six * /y11 + twelve * /x5  + exti * /x5  +
      extq * /sgni
;
/y4   := one * /y5  + two * /y6  + three * /y7  + four *
      /y8  + six * /y10 + twelve * /x4  + exti * /x4  +
      extq * /sgni
;
```