File : PNCODE.DOC
Date : 10/8/95
Subject : PN Code Generator - Software Requirements

Table 1. IOSelA Address Decoder (A6..A1)

Addr Hex	R/W*	Data	Command	
00	0	D[11..0]	Load Shift Enable Length (Length - 1)	(+)
01	0	D[15..0]	Load Code Length (Length - 1)	(+)
02	0	D[15..0]	Load Code Start Address	(+)
03	0	D[3..0]	Load RAM Data	(+)
04	0	D[1..0]	Write Command Word (Table 2)	
00	1	D[11..0]	Read Shift Enable Length	
01	1	D[15..0]	Read Code Length	
02	1	D[15..0]	Read Code Start Address	
03	1	D[3..0]	Read RAM Data	(+)
04	1	D[0]	Read Status (Table 3)	
05	1	D[15..0]	Read RAM Address	(+)

(+) Shift Enable must be stopped. To load the RAM, load the RAM address using 'Load Code Start Address'. The RAM address is loaded synchronously with the Multiply Clock. Thus, it is best to verify the RAM address using 'Read RAM Address' before loading or reading the RAM data.

Table 2. Command Word

Bits	Command
1,0	Shift Enable Start Mode 0 : NOP 1 : Stop 2 : Start on trigger 3 : Start immediate

Table 3. Status Word

Bit	Description
0	Shift Enable is enabled (Trigger has occurred.)