File : MemoryPNCode128k.wpd
Date : 3/29/2005
Subject : Memory PN Code Generator 128k - Software Requirements

Table 1. IOSelA Address Decoder (A6..A1)

Addr Hex	R/W*	Data	Command
00	0	D[11..0]	Load Shift Enable Length (Length - 1) (+)
01	0	D[15..0]	Load Code Length (Length - 1) (+)
02	0	D[15..0]	Load Code Start Address (+)
03	0	D[3..0]	Load RAM Data (+)
04	0	D[1..0]	Write Command Word (Table 2)
00	1	D[11..0]	Read Shift Enable Length
01	1	D[15..0]	Read Code Length
02	1	D[15..0]	Read Code Start Address
03	1	D[3..0]	Read RAM Data (+)
04	1	D[0]	Read Status (Table 3)
05	1	D[15..0]	Read RAM Address (+)

(+) Shift Enable must be stopped. To load the RAM, load the RAM address using 'Load Code Start Address'. The RAM address is loaded synchronously with the Multiply Clock. Thus, it is best to verify the RAM address using 'Read RAM Address' before loading or reading the RAM data.

Table 2. Command Word

Bits	Command
1,0	Shift Enable Start Mode
	0 : NOP
	1 : Stop
	2 : Start on trigger
	3 : Start immediate

Table 3. Status Word

Bit	Description
0	Shift Enable is enabled (Trigger has occurred.)

Explanation of Operation :

Don Campbell requested a code of length 131071 (called the 128k code for convenience) for a S-Band experiment in April, 2005. We used one of the spare IPack code generator boards and installed it in IPack Slot B of the Motorola 162 Board (dap1) in the datataking VME crate. We also used a spare chassis for an external interface to the IPack board.

The new version has all the same commands as the present memory pncode generator, and no new commands. There are 4 bits on the front panel, Mem3, Mem2, Mem1, Mem0, which usually correspond to the respective memory bits in the 4 x 64k memory. Mem3 is usually used for the code, and this also comes out the rear panel.

In the case of the 128k code, we will also use BNC labelled Mem3 on the external chassis for the code. We will daisy chain 2 memory bits, Bit3 and Bit2 in MACH435 PAL on the code generator board. As usual, the code starts on the programmed start address of Bit3 of the memory. When address counter counts down to zero, the next location is the programmed code length of Bit2. When the address counter counts down to zero, the sequence repeats again starting at programmed start address of Bit3. Thus, we can do an odd length code since the programmed start address and programmed code length can be different.

Mem2, Mem1, and Mem0 correspond as usual to Bit2, Bit1, and Bit0. When the programmed start address is 65535 and the programmed code length is 65534, the most significant memory location of Bit 1 can used as the marker.