IP CORE MANUAL

AXI4-Stream to DDR4 Memory Controller Interface IP

px_axisrq2ddrctlr

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream to DDR4 Memory Controller Interface Core accepts read/write request AXI4-Streams from the user design and transfers them to the Xilinx® DDR4 Memory Controller IP Core in the required format.

This core complies with the ARM® AMBA® AXI4 Specification and also provides a control/status register interface. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream to DDR4 Memory Controller Interface Core.

Features

- Software programmable DDR4 memory size
- Converts AXI4-Stream requests into DDR4 Memory Controller user interface signals
- Register access through AXI4-Lite interface

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite and AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	N/A
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top-level module of the user design.

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Chapter 1: Overview

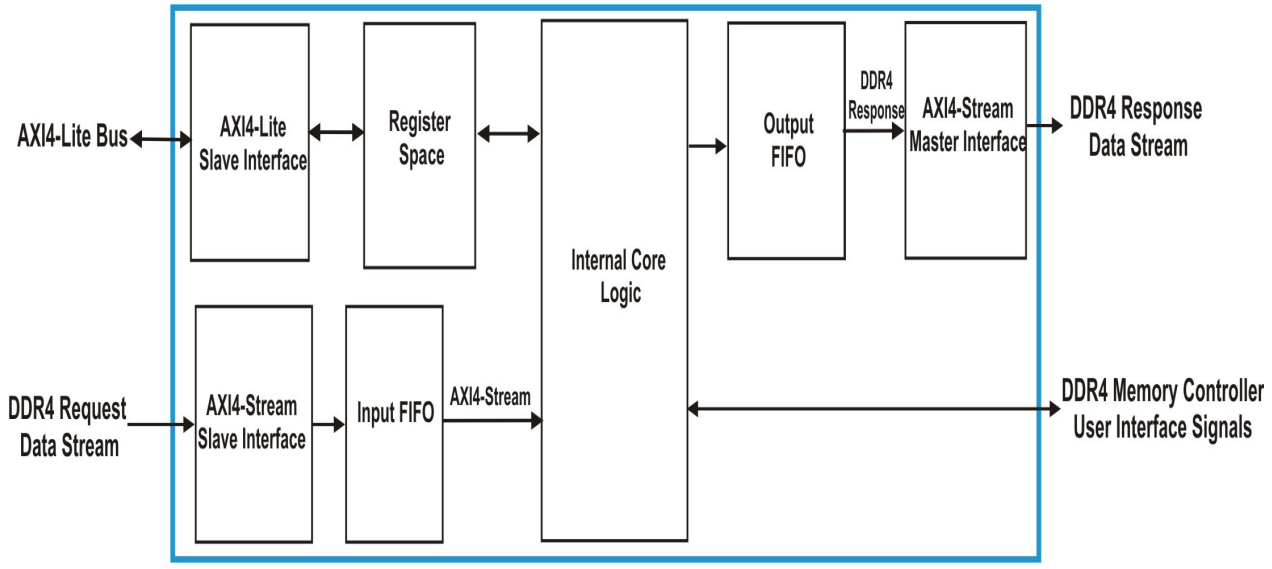
1.1 Functional Description

The AXI4-Stream to DDR4 Memory Controller Interface Core provides a transaction interface to the Xilinx DDR4 SDRAM Memory Controller. This core accepts DDR4 Memory read/ write request AXI4-Streams from the user design and converts them into user interface signals of the Xilinx DDR4 Memory Controller IP Core (*Xilinx DDR4 SDRAM Memory Controller Core Product Guide*). It also accepts the responses from the Xilinx DDR4 Memory Controller Core and converts them into AXI4-Streams which are transferred to the user design.

The size of the DDR4 Memory can be defined by the user through the generic parameter **mem_size** (see Table 2-2). This core also has an AXI4-Lite Interface to access the Register Space of the core.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream to DDR4 Memory Controller Interface Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Stream to DDR4 Memory Controller Interface Core Block



1.1 Functional Description (continued)

- **AXI4-Stream Interface:** The AXI4-Stream to DDR4 Memory Controller Interface Core has two AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive input AXI4-Streams and at the output an AXI4-Stream Master Interface is used to transfer AXI4-Streams through the output ports. For more details about the AXI4-Stream Interfaces refer to Section 3.2 AXI4-Stream Core Interfaces.

- **AXI4-Lite Interface:** This module implements a 32-bit AXI4-Lite Slave interface to access the register space. For more details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

- **Register Space:** This module contains control and status registers of the core. Registers are accessed through the AXI4-Lite interface.

- **Input and Output FIFO:** The Input FIFO is used to store the incoming AXI4-Stream requests from the user design, and the Output FIFO is used to store the response AXI4-Streams that are output to the user design.

1.2 Applications

The AXI4-Stream to DDR4 Memory Controller Interface Core can be used as an interface to transfer DDR4 AXI4-Stream requests from the user design to the Xilinx DDR4 SDRAM Memory Controller Core.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

4) *Xilinx DDR4 Memory Controller Core*

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Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream to DDR4 Memory Controller Interface Core has bus interfaces that comply with the *ARM AMBA AXI4-Lite Protocol Specification* and the *AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream to DDR4 Memory Controller Interface Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Stream to DDR4 Memory Controller Interface Core has a maximum frequency of 250MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream to DDR4 Memory Controller Interface Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	264
Flip-Flops	362

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream to DDR4 Memory Controller Interface Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream to DDR4 Memory Controller Interface Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
mem_size	integer	**DDR4 Memory Size:** This generic parameter indicates the size of the DDR4 Memory in Gigabytes. It can range from 0 to 3. **0 = 2 GB** **1 = 4 GB** **2 = 8 GB** **3 = 16 GB**

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- AXI4-Stream Core Interfaces

3.1 AXI4-Lite Core Interfaces

The AXI4-Stream to DDR4 Memory Controller Interface Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4-Lite Slave Interface that can be used to access the control and status registers in the AXI4-Stream to DDR4 Memory Controller Interface Core. Table 3-1 defines the ports in the CSR interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This signal will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the AXI4-Stream to DDR4 Memory Controller Interface Core.
s_axi_csr_awprot	Input	3	**Protection:** The AXI4-Stream to DDR4 Memory Controller Interface Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The AXI4-Stream to DDR4 Memory Controller Interface Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Stream to DDR4 Memory Controller Interface Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr _wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Stream to DDR4 Memory Controller Interface Core when it is ready to accept data. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The AXI4-Stream to DDR4 Memory Controller Interface Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4-Stream to DDR4 Memory Controller Interface Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the AXI4-Stream to DDR4 Memory Controller Interface Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Stream to DDR4 Memory Controller Interface Core
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The AXI4-Stream to DDR4 Memory Controller Interface Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Stream to DDR4 Memory Controller Interface Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_ arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The AXI4-Stream to DDR4 Memory Controller Interface Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4-Stream to DDR4 Memory Controller Interface Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_ rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 AXI4-Stream Core Interfaces

The AXI4-Stream to DDR4 Memory Controller Interface Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- DDR4 Request (RQST) Interface: This core has an DDR4 Memory Request AXI4-Stream Interface at the input of the core to receive memory read/ write requests from the user design.
- DDR4 Response (RSP) Interface: This core has an DDR4 Memory Response AXI4-Stream Interface at the output of the core to transfer response data streams to the user design.

3.2.1 DDR4 Request (RQST) Interface

The AXI4-Stream to DDR4 Memory Controller Interface Core implements an DDR4 Request Interface across the input to receive memory read/ write request data streams. This is an AXI4-Stream Slave Interface.

Table 3-2 defines the ports in the DDR4 Request Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-2: DDR4 Request Interface Port Descriptions

Port	Direction	Width	Description
s_axis_rqst_tdata	Input	512	**Request Data Bus:** This is the DDR4 Memory Request data received by the core from the user design.
s_axis_rqst_tvalid		1	**Request Data Valid:** Asserted when data is valid on **s_axis_rqst_tdata** bus. The user application can pace the data transfer using the **s_axis_rqst_tready** signal.
s_axis_rqst_tuser		256	**Request User Data:** This is the sideband user information data which contains the DDR4 memory request packet header. Table 3-3 includes the bit definitions of the bits **tuser[256:0].**
s_axis_rqst_tlast		1	**Request Data Last:** Since all request frames are single-clock-cycle in length, this **tlast** signal is asserted on every valid data cycle. It is provided mainly to allow arbitration in AXI Stream switches to use it to arbitrate on **tlast**.
s_axis_rqst_tid		8	**Request Data Stream Identifier:** This is the unique data stream identifier.
s_axis_rqst_tready	Output	1	**Request Data Ready:** Activation of this signal by the core indicates that the it is ready to accept data. Data is received across this interface when both **s_axis_rqst_tvalid** and **s_axis_rqst_tready** are asserted in the same clock cycle.

3.2 AXI4-Stream Core Interfaces (continued)

3.2.1 DDR4 Request (RQST) Interface

Table 3-3 shows the bit definitions of the DDR4 Request Interface user data (**s_axis_rqst_tuser**).

Table 3-3: DDR4 Request Interface User Data Bit Definitions

Bit index	Name	Width	Description
255:128	**DATA**	128	**RAM Data:** These bits carry the upper 128 bits of RAM data to be written to the address location in the DDR4 SDRAM.
127:120	**RES**	9	**Reserved**
119:40	**MSK**	80	**Byte Mask:** These bits indicate the byte masks of the data i.e., the data bits on the data bus to be masked.
39:36	**RES**	4	**Reserved**
35	**OP**	1	**Type of Request:** This bit indicates the type of Memory request. 0 = Write 1 = Read
34:32	**ADDRE**	3	**Future Address Expansion:** These bits indicate the address expansion of the DDR4 SDRAM memory location.
31:0	**ADDR**	32	**DDR4 Memory Address:** This is the address location in the DDR4 SDRAM where the read/ write operation is to be performed. The address must be aligned to request size boundaries.

3.2.2 DDR4 Response (RSP) Interface

The AXI4-Stream to DDR4 Memory Controller Interface Core implements an DDR4 Response Interface across the output of the core to transfer response data streams to the user design. This is an AXI4-Stream Master Interface.

Table 3-4 defines the ports in the DDR4 Response Interface. This interface is an AXI4-Stream Master Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-4: DDR4 Response Interface Port Descriptions

Port	Direction	Width	Description
m_axis_rsp_tdata	Output	512	**Response Data Bus:** This is the Response data transferred to the user design for a DDR4 memory read request.
m_axis_rsp_tvalid		1	**Response Data Valid:** Asserted when data is valid on **m_axis_rsp_tdata**. This bus cannot be throttled and there is no **tready** output from the core. The user design must be ready to accept data if it requested it.
m_axis_rsp_tuser		256	**Request User Data:** This is the sideband user information data which contains the DDR4 response packet header and error indicators. Table 3-5 defines the bit definitions of the bits **tuser[255:0].**
m_axis_rsp_tlast		1	**Request Data Last:** Since all request frames are single-clock-cycle in length, this **tlast** signal is asserted on every valid data cycle. It is provided mainly to allow arbitration in AXI Stream switches to use it to arbitrate on **tlast**.
m_axis_rsp_tid		8	**Response Data Stream Identifier:** This is the unique data stream identifier specified by the user in the request which identifies the request corresponding to the response.

3.2 AXI4-Stream Core Interfaces (continued)

3.2.2 DDR4 Response (RSP) Interface

Table 3-5 shows the bit definitions of the DDR4 Response Interface user data (**m_axis_rsp_tuser**).

Table 3-5: DDR4 Response Interface User Data Bit Definitions

Bit index	Name	Width	Description
255:128	**DATA**	128	**RAM Data:** These bits carry the upper 128 bits of RAM data to be written to the address location in the DDR4 SDRAM.
127:120	**RES**	9	**Reserved**
119:40	**MSK**	80	**Byte Mask:** These bits indicate the byte masks of the data i.e., the data bits on the data bus to be masked.
39:35	**RES**	4	**Reserved**
34:32	**ADDRE**	3	**Future Address Expansion:** These bits indicate the address expansion of the DDR4 SDRAM memory location.
31:0	**ADDR**	32	**DDR4 Memory Address:** This is the address location in the DDR4 SDRAM where the read/ write operation is to be performed. The address must be aligned to request size boundaries.

3.3 I/O Signals

The I/O port/signal descriptions of the AXI4-Stream to DDR4 Memory Controller Interface Core are discussed in Table.

Table 3-6: I/O Signals

Port/Signal Name	Type	Direction	Description
ddr4_app_axis_clk	std_logic	Input	**User Interface Clock:** This is the user interface clock input from the Xilinx DDR4 Memory Controller Core.
ddr4_app_en		Output	**DDR4 Application Enable:** This is the active High strobe for **app_addr[]**, **app_cmd[2:0]**, **app_sz**, and **app_hi_pro** outputs of the core.
ddr4_app_hi_pri			**DDR4 Application High Priority:** This output of the core is reserved for the Xilinx DDR4 Memory Controller and must be tied to 0.
ddr4_app_rdy		Input	**DDR4 Application Ready:** When High, this input indicates that the Xilinx DDR4 Memory Controller Core is ready to accept commands. If this is de-asserted when **ddr4_app_en** is enabled, the current **ddr4_app_cmd** and **ddr4_app_addr** must be retired until **ddr4_app_rdy** is asserted.
ddr4_app_addr [27+mem_size : 0]	std_logic _vector	Output	**DDR4 Application Address:** This is address output of the request.
ddr4_app_cmd[2:0]			**DDR4 Application Command:** These bits indicate the command of the current request. **000 - Write request** **001 - Read request**
ddr4_app_wdf_data [639:0]			**DDR4 Application Write Data FIFO Write Data:** This is the output write data for the write commands.
ddr4_app_wdf_mask [79:0]			**DDR4 Application Write Data FIFO Byte Mask:** Each bit in this vector corresponds to a byte of **ddr4_app_wdf _data[]**. **ddr4_app_wdf_mask[0]** corresponds to **ddr4_app_wdf_data[7:0]** and **ddr4_app_wdf_mask[79]** corresponds to **ddr4_app_wdf_data[639:632]**. Setting a bit of **ddr4_app_wdf_mask** to logic ‘1’ prevents the corresponding byte of **ddr4_app_wdf_data** from being written into the DDR4 SDRAM memory.

Table 3-6: I/O Signals (Continued)

Port/Signal Name	Type	Direction	Description
ddr4_app_wdf_end	std_logic	Output	**DDR4 Application Write Data FIFO End Marker:** Active High. This indicates that the current clock cycle is the last clock cycle of output data on **ddr4_app_wdf_data[]**.
ddr4_app_wdf_wren			**DDR4 Application Write Data FIFO Write Enable:** Active High strobe for **ddr4_app_wdf_data**.
ddr4_app_wdf_rdy		Input	**DDR4 Application Write Data FIFO Ready:** This input indicates that the Write Data FIFO is ready to receive data. Write data is transferred when **ddr4_app_wdf_rdy** and **ddr4_app_wdf_wren** are both High.
ddr4_app_rd_data[639:0]	std_logic _vector		**DDR4 Application Read Data:** This is the input read data from the Xilinx DDR4 Memory Controller for a read request.
ddr4_app_rd_data_valid	std_logic		**DDR4 Application Read Data Valid:** Active High. When High, this bit indicates that the data on **ddr4_app_rd _data** is valid.
ddr4_app_rd_data_end			**DDR4 Application Read Data End:** Active High. When High, this bit indicates that the current clock cycle is the last cycle of input data on **ddr4_app_rd_data[]**.
init_calib_complete	std_logic	Input	**DDR4 SDRAM Initialization and Calibration Complete:** Asserted by the Xilinx DDR4 Memory Controller core when the initialization and calibration of the DDR4 memory is complete.
ddr4_sys_rst		Output	**DDR4 System Reset:** This is an asynchronous system reset output to the Xilinx DDR4 Memory Controller Core.

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Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the AXI4-Stream to DDR4 Memory Controller Interface Core. The memory map is provided in Table 4-1.

Table 4-1: Register Space Memory Map

Register Name	Address (Base Address +)	Access	Description
Control Register	0x00	R/W	Controls the system reset of the Xilinx DDR4 Memory Controller IP and the input/ output FIFOs of the core.
Status Register	0x04	R	Indicates the calibration status of the DDR4 memory.

4.1 Control Register

This register controls the system reset of the Xilinx DDR4 Memory Controller IP Core, and the reset of the input and output FIFOs within AXI4-Stream to DDR4 Memory Controller Interface Core. The Control Register is illustrated in Figure 4-1 and described in Table 4-2.

Figure 4-1: Control Register

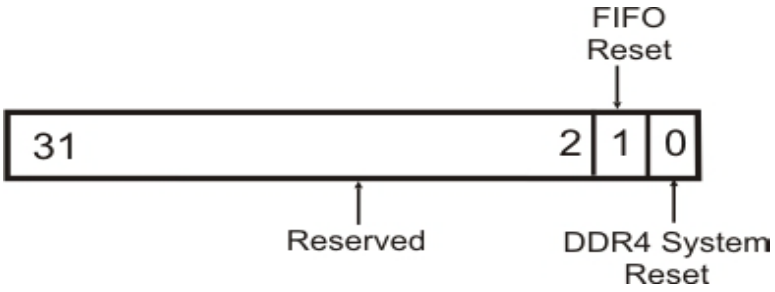

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Table 4-2: Control Register (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	N/A	N/A	**Reserved**
1	fifo_rst	0	R/W	**FIFO Reset:** This bit will reset the input and output FIFOs of the core in conjunction with the CSR reset. This bit is ORed with the CSR reset of the core to generate the FIFO reset. 0 = Run 1 = Reset
0	rst			**DDR4 System Reset:** This bit controls the reset of the DDR4 Memory Controller IP Core. It maps to the system reset port of the Xilinx DDR4 Memory Controller Core. 0 = Run 1 = Reset

4.2 Status Register

This register indicates the status of the initialization and calibration of the DDR4 SDRAM memory. The Status Register is illustrated in Figure 4-2 and described in Table 4-3.

Figure 4-2: Status Register

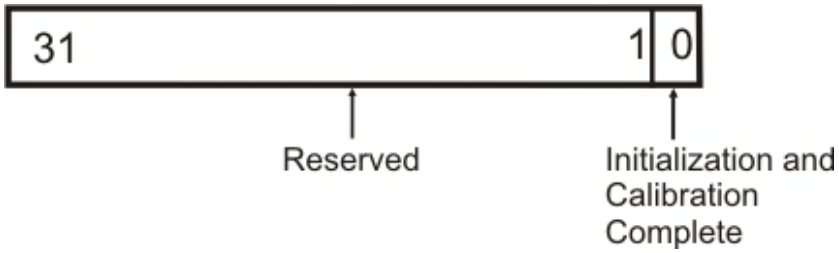

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Table 4-3: Status Register (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:0	Reserved	N/A	N/A	**Reserved**
0	init_calib_complete	0	R	**Initialization and Calibration Complete: T**his bit indicates whether the initialization and calibration of the DDR4 memory are complete. 0 = In progress 1 = Complete

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream to DDR4 Memory Controller Interface Core.

5.1 General Design Guidelines

The AXI4-Stream to DDR4 Memory Controller Interface Core is used to convert DDR4 requests from the user design into user interface signals of the Xilinx DDR4 SDRAM Memory Controller Core. The memory size of the DDR4 SDRAM memory can be specified by the user through the generic parameter as described in Section 2.5.

5.2 Clocking

Main Clock: **s_axi_aclk**

This clock is used to clock all the ports of the core.

5.3 Resets

CSR Reset: **s_axi_csr_aresetn**

This is an active low reset synchronous with **s_axi_aclk**.

5.4 Interrupts

This section is not applicable to this IP core.

5.5 Interface Operation

CSR Interface: This is the Control/Status Register Interface and is associated with **s_axi_aclk**. It is a standard AXI4-Lite Slave Interface. See Chapter 4 for the control register memory map, which provides more details on the registers that can be accessed through this interface.

DDR4 Request (RQST) Interface: This is an AXI4-Stream Slave Interface used to receive DDR4 request data streams and is associated with **s_axi_aclk**. For more details about this interface refer to Section 3.2.1.

5.5 Interface Operation (continued)

DDR4 Response (RSP) Interface: This is an AXI4-Stream Slave Interface used to transfer DDR4 response data streams to the user design and is associated with **s_axi_aclk**. For more details about this interface refer to Section 3.2.2.

5.6 Programming Sequence

This section briefly describes the programming sequence of registers in the AXI4-Stream to DDR4 Memory Controller Interface Core.

1) Assign the desired value to the generic parameter.

2) Set the Control Register with the required values.

3) Write/read data to/from the DDR4 SDRAM.

5.7 Timing Diagrams

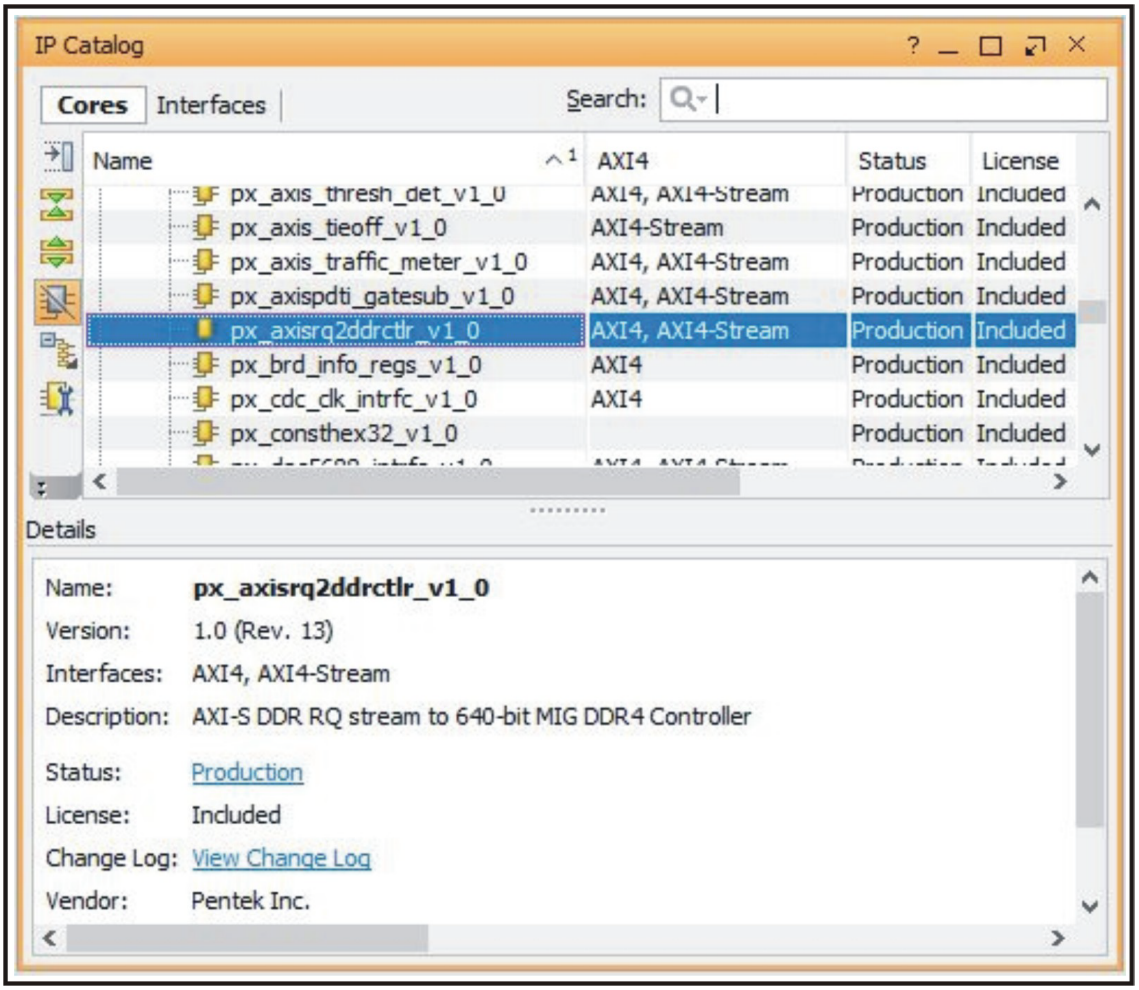
This section is not applicable to this IP core.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream to DDR4 Memory Controller Interface Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axisrq2ddrctlr_v1_0** as shown in Figure 6-1.

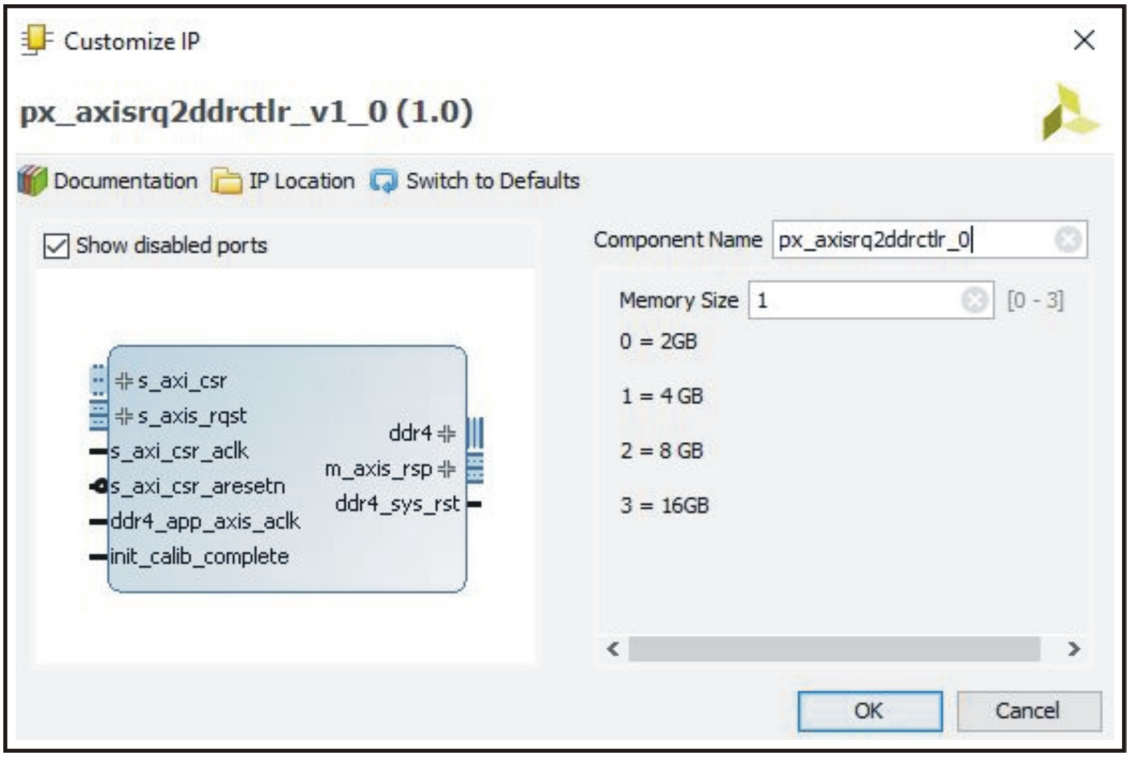
Figure 6-1: AXI4-Stream to DDR4 Memory Controller Interface Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_axisrq2ddrctlr_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6-2). The core's symbol is the box on the left side.

Figure 6-2: AXI4-Stream to DDR4 Memory Controller Interface Core IP Symbol



6.2 User Parameters

The user parameter of this IP core is described in Section 2.5 of this user manual.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

6.4 Constraining the Core

This section contains information about constraining the AXI4-Stream to DDR4 Memory Controller Interface Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream to DDR4 Memory Controller Interface Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The clock frequency (**s_axi_aclk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

The testbench and simulation results for this IP core will be available in the next release of the IP core and the IP user manual.

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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