IP CORE MANUAL

AXI4-Stream Data Tie Off IP

px_axis_tieoff

PENTEK

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458
(201) 818-5900
http://www.pentek.com/

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream Data Tie Off Core assigns the user-defined, constant values of generic parameters to an AXI4-Stream output.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Data Tie Off Core.

Features

- User-programmable width of payload data and sideband information of the AXI4-Stream output
- User-defined values for the output AXI4-Stream payload data and sideband information
- AXI4-Stream interface signals, namely **tlast**, **tkeep** and **tready**, can be enabled (or disabled) by the user
- AXI4-Stream interface signals, namely **tlast**, **tkeep** and **tvalid**, can be set to remain always asserted (or negated) based on the user requirement

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	N/A
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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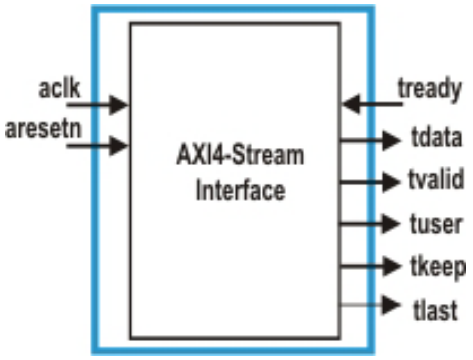
Chapter 1: Overview

1.1 Functional Description

The AXI4-Stream Data Tie Off Core Core generates an AXI4-Stream output based on the generic parameters defined by the user (see Section 2.5). Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Data Tie Off Core when the core has **tready**, **tlast**, and **tkeep** signals enabled.

Figure 1-1: AXI4-Stream Data Tie Off Core Block Diagram



1.2 Applications

The AXI4-Stream Data Tie Off Core can be incorporated into any Kintex Ultrascale FPGA to tie off AXI4-Stream output to user-defined values.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Data Tie Off Core has bus a interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

This section is not applicable to this IP core.

2.3 Resource Utilization

This IP core utilizes only the I/O resources of the FPGA it is incorporated into.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Data Tie Off Core are described in Table 2-1. These parameters can be set as required by the user application while customizing the core.

Table 2-1: Generic Parameters

Port/Signal Name	Type	Description
num_data_bytes	Integer	**Number of Data Bytes:** This parameter defines the width of the payload data of the AXI4-Stream in bytes.
num_user_bits		**Number of User Bits:** This parameter defines the width (in bits) of the user sideband information that is transmitted alongside the data stream.
tdata_value		**Output Data Value:** This is the user-defined value of the output AXI4-Stream data (**m_axis_tdata**). It is defined as an integer which is converted to binary format internally by the core.
tuser_value	Integer	**Output Sideband Data Value:** This is the user-defined value of the output AXI4-Stream sideband data (**m_axis_tuser**). It is defined as an integer which is converted to binary format internally by the core.

Table 2-1: Generic Parameters (Continued)		
Port/Signal Name	**Type**	**Description**
has_tlast	Boolean	**Has Data Last Output:** This parameter is used to enable the Data Last (**m_axis_tlast**) signal in the output AXI4-Stream. Data Last indicates the boundary of the data packet.
has_tkeep		**Has Data Keep Output:** This parameter is used to enable the Data Keep (**m_axis_tkeep**) signal in the output AXI4-Stream. Data Keep is a byte qualifier which indicates whether the data in the associated byte of **m_axis_tdata** is processed as a part of the data stream.
has_tready		**Has Data Ready Input:** This parameter is used to enable the Data Ready input from a slave in the user design, receiving the output AXI4-Stream data of this core.
tlast_asserted		**Data Last always Asserted:** This parameter, when set to True, keeps the output Data Last signal always asserted. This parameter is valid only when the generic parameter **has_tlast** is set to True.
tvalid_asserted		**Data Valid always Asserted:** This parameter, when set to True, maintains the output Data Valid signal in a constant asserted state. This indicates that this core is always driving a valid AXI4-Stream transfer.
tkeep_asserted		**Data Keep always Asserted:** This parameter, when set to True, keeps the output Data Keep signal always asserted. This parameter is valid only when the generic parameter **has_tkeep** is set to True.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

The AXI4-Stream Data Tie Off Core implements an AXI4-Stream Master Interface at the output to transfer data streams across the output ports.

Table 3-1 defines the ports in the AXI4-Stream Master Interface. See the *AMBA AXI4-Stream Specification* for more details on operation of the AXI4-Stream interfaces.

Table 3-1: AXI4-Stream Master Interface Port Descriptions

Port	Direction	Width	Description
aclk	Input	1	**Clock**
aresetn			**Reset:** Active Low.
m_axis_tdata	Output	depends on the generic parameter **num_data_bytes**	**Output Data**
m_axis_tvalid		1	**Output Data Valid:** This signal is asserted when data is valid on **m_axis_tdata** bus. This signal can remain always asserted by setting the generic parameter **tvalid_asserted** to True.
m_axis_tready	Input	1	**Data Ready**: Active High. This is an input **tready** signal from a slave in the user design indicating that it is ready to accept data. This input can be enabled by setting the generic parameter **has_tready** to True. When **has_tready** is True, data is transferred across the AXI4-Stream interface when both **m_axis_tvalid** and **m_axis_tready** are High on the same cycle. If the slave deasserts the ready signal when **m_axis_tvalid** is High, the core maintains the data on the bus and keeps the valid signal asserted until the slave re-asserts the ready signal.

Table 3-1: AXI4-Stream Master Interface Port Descriptions (Continued)

Port	Direction	Width	Description
m_axis_tuser	Output	depends on the generic parameter **num_user_bits**	**Sideband Data:** This is the user-defined sideband output information which is transmitted alongside the data stream.
m_axis_tkeep		depends on the generic parameter **num_data_bytes**	**Data Keep:** This is an byte qualifier signal and is valid only when the generic parameter **has_tkeep** is set to True. Each bit of this signal corresponds to a byte in **m_axis_tdata** i.e., bit 0 corresponds to the least significant byte of **m_axis_tdata** and the most significant bit to the most significant byte. When a bit is asserted, the data on **m_axis_tdata** is considered valid. All **m_axis_tkeep** bits must be '1' contiguously until **m_axis_tlast** is asserted. When **m_axis_tlast** is asserted, and the number of data samples is not a multiple of the **tdata** width, **tkeep** bits are set to '0' to indicate which data bytes are to be ignored. All bits in the **tkeep** signal can be held in a constant asserted state by setting the generic parameter **tkeep_asserted** True.
m_axis_tlast		1	**Data Last:** This signal is valid when the generic parameter **has_tlast** is set to True. When asserted, **m_axis_tlast** marks the last data in the current data frame. This signal can remain always asserted by setting the generic parameter **tlast_asserted** True.

Chapter 4: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Data Tie Off Core.

4.1 General Design Guidelines

The AXI4-Stream Data Tie Off Core generates an AXI4-Stream output from user-defined values.

4.2 Clocking

Clock: **aclk**

The clock (**aclk**) input is not used within this IP core. This input is available in order meet the Vivado IP Integrator requirements. It should have a clock frequency equivalent to the clock frequency of the Slave in the user design receiving the AXI4-Stream.

4.3 Resets

Main reset: **aresetn**

This is an active low AXI4-Stream reset input and is not used within this IP core. This input is available in order meet the Vivado IP Integrator requirements.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

AXI4-Stream Interface: This core has an AXI4-Stream Master Interface to transfer data streams. For more details about this interface, refer to Section 3.1.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

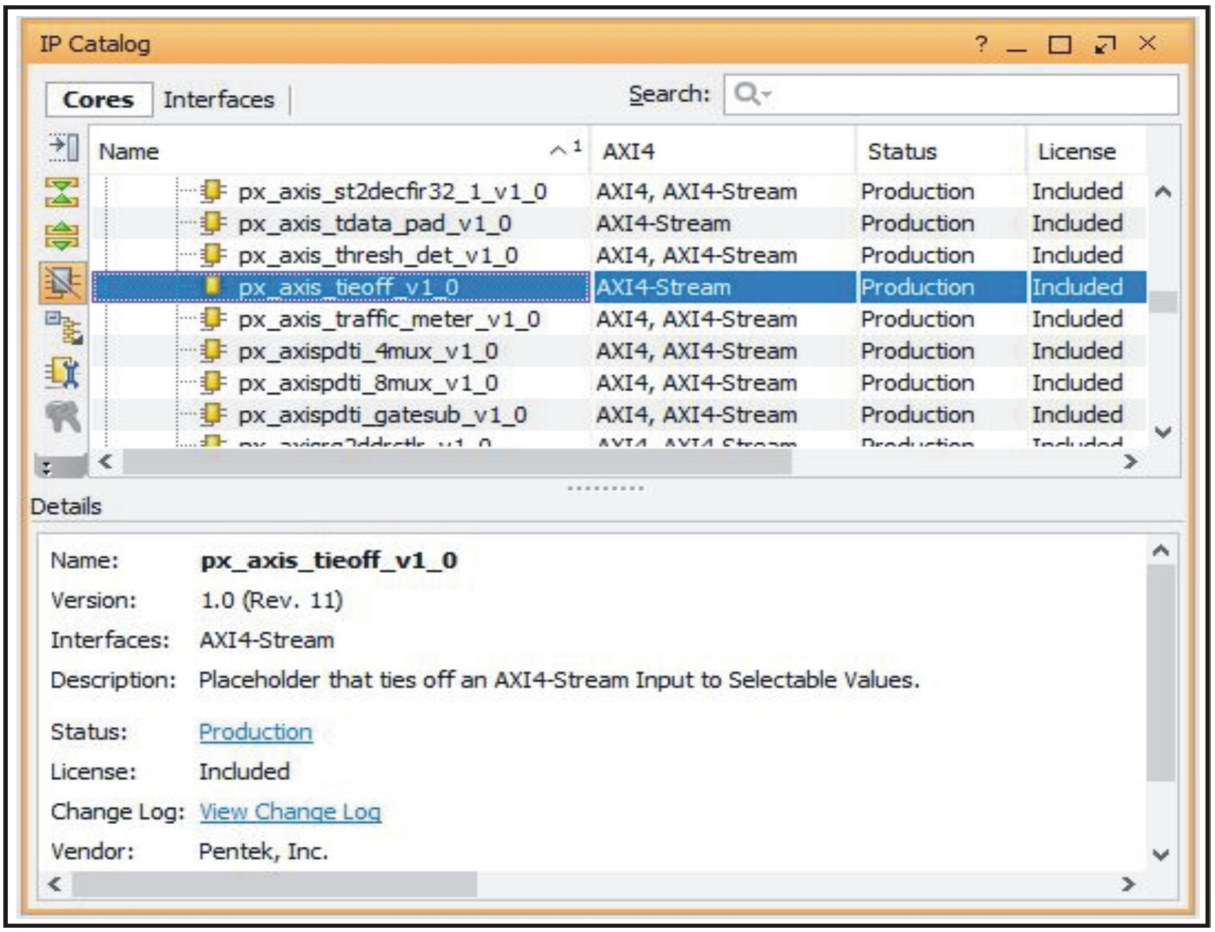
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Data Tie Off Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_tieoff_v1_0** as shown in Figure 5-1.

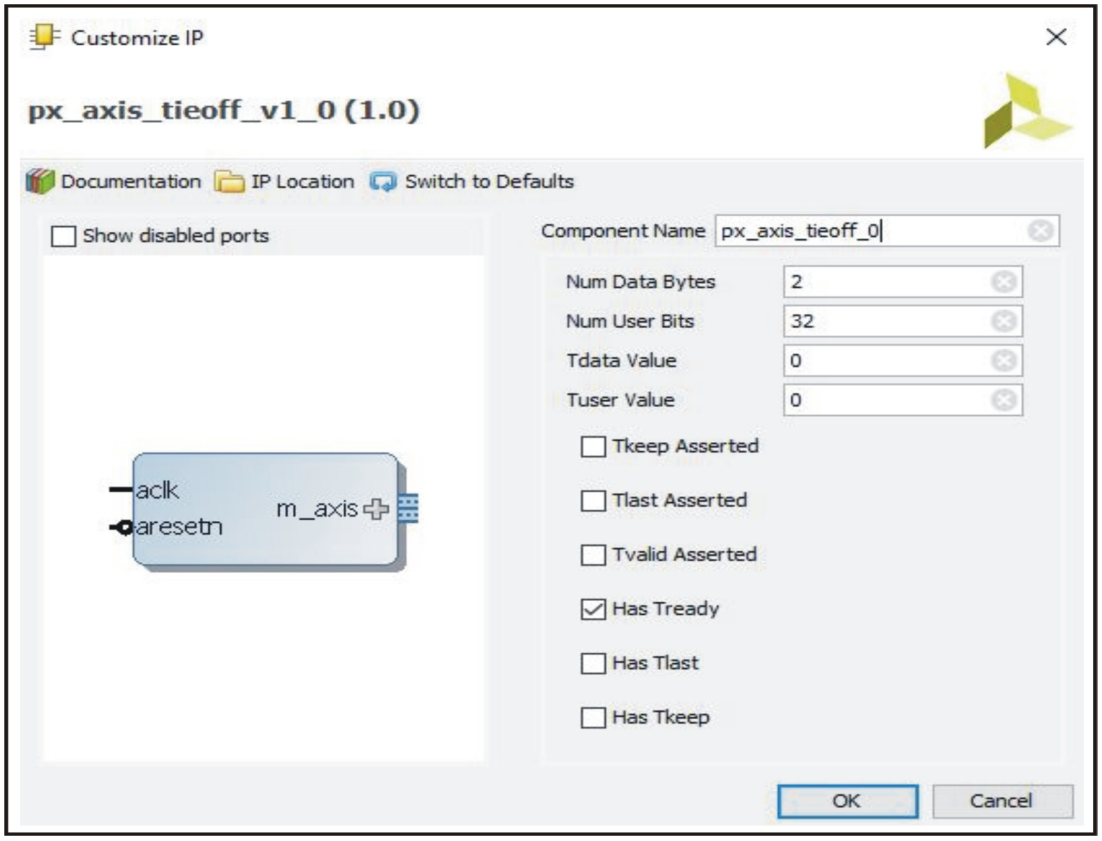
Figure 5-1: AXI4-Stream Data Tie Off Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_tieoff_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Stream Data Tie Off Core IP Symbol



5.2 User Parameters

The user parameters of this core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

5.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Data Tie Off Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Data Tie Off Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The clock frequency of the **s_axis_aclk** signal of this core should match the frequency of the AXI4-Stream Slave in the user design which is receiving the data streams.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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