IP CORE MANUAL

AXI4-Stream Threshold Detector IP

px_axis_thresh_det

PENTEK

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Table of Contents

Page

Table of Contents

Page

Chapter 4: Register Space

Chapter 5: Designing with the Core

Table of Contents

Page

Chapter 6: Design Flow Steps

Table of Contents

Page

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IP Facts

Description

Pentek Navigator™ AXI4-Stream Threshold Detector Coreperforms a threshold detection with hysteresis on the input AXI4-Stream data (unsigned) of the core. This core also generates an output AX4-Stream indicating threshold detection based on the generic parameters defined by the user (see Section 2.5).

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Threshold Detector Core.

Features

- Supports generation of output AXI4-Stream indicating the threshold detection
- Register access through AXI4-Lite interface
- User-programmable input data width, default threshold, and default hysteresis amount below threshold
- Supports generation of an interrupt output
- Provides register access to control threshold value, hysteresis below threshold value, and the reset of threshold detection state machine

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite and AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

The AXI4-Stream Threshold Detector Core accepts input AXI data streams with unsigned data values and generates a **detection status signal** which goes High when the data input is greater than the threshold. It remains High until the input data value falls below the hysteresis value (threshold value minus hysteresis below threshold value).

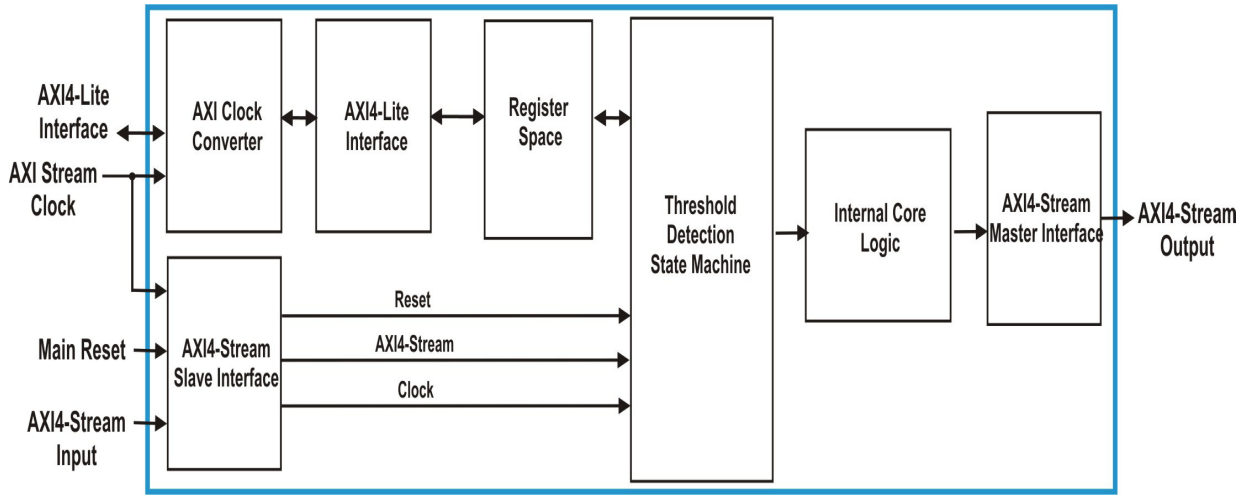
The generation and control of the detection status signal is performed by the **Threshold detection State Machine** of the AXI4-Stream Threshold Detector core as shown in Figure 1-1. The initial values of threshold and hysteresis amount below threshold can be defined by the user through generic parameters as described in Table 2-2.

This core has an **AXI4-Lite interface** to access the **control/status registers** within the core. The **Register Space** within this core has control/status registers which can be used to control the state machine reset, threshold value, and hysteresis below threshold value. The input data width can be defined by the user through the generic parameter **data_width** (see Table 2-2). An AXI4-Stream data output with the detection status can also be enabled by the user through the generic parameters.

The AXI4-Stream Threshold Detector core has an AXI Clock Converter core which is connected to the AXI4-Lite Interface in order to operate the Register Space in the AXI4-Stream Clock domain. An interrupt output can also be enabled by the user for rising and falling edges of the detection status signal

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Threshold Detector Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Stream Threshold Detector Core Block Diagram



1.1 Functional Description (continued)

- **AXI Clock Converter Core:** The AXI clock converter core is included in the Xilinx® AXI Interconnect Core and is used to connect one AXI memory-mapped slave to another AXI memory-mapped master which is operating in a different clock domain. In the Threshold Detector core, the AXI Clock converter is used to operate the Register Space in the AXI4-Stream Clock domain (**axis_aclk**).

- **AXI4-Stream Interface:** The AXI4-Stream Threshold Detector Core has three AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive input AXI data streams and at the output an AXI4-Stream Master Interface is used to transfer AXI data streams through the output ports. For more details about the AXI4-Stream Interfaces refer to Section 3.2 AXI4-Stream Core Interfaces.

- **AXI4-Lite Interface:** This core implements a 32-bit AXI4-Lite Slave Interface to access the Register Space. For more details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

- **Register Space:** This module contains control and status registers including Interrupt Enable, Interrupt Status and Interrupt Flag registers. Registers are accessed through the AXI4-Lite interface.

- **Threshold Detection State Machine:** This state machine is used control the detection status signal and has two states which are Reset and Threshold states.

  - **Reset State:** Resets the state machine based on the reset defined by the user in the Control Register 0 with the detection status signal set to Low. When reset is de-asserted, the state machine checks whether the input data is greater than the threshold value. If it is True, the detection status signal goes High and the state machine moves to the Threshold state.

  - **Threshold State:** In this state, the input data is compared to the hysteresis value (threshold value minus hysteresis below threshold value). As long as the input data is greater than the hysteresis value, the detection status remains High. When the input data falls below the hysteresis value, the detection status goes Low and the state machine moves to the Reset State.

1.2 Applications

The AXI4-Stream Threshold Detector Core can be used for threshold detection with hysteresis of AXI Data Streams and can be incorporated into any Kintex Ultrascale FPGA.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

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Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Threshold Detector Core has bus interfaces that comply with the A*RM AMBA AXI4-Lite Protocol Specification* and the *AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Threshold Detector Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Stream Threshold Detector Core has two incoming clock signals. The input AXI4-Stream clock has a maximum frequency of 250MHz and the clock across the AXI4-Lite Interface also has a maximum frequency of 250MHz on a Kintex Ultra-scale -2 speed grade FPGA. 250 MHz is typically the PCI Express® (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream Threshold Detector Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	536
Flip-Flops	1174
Memory LUTs	70

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream Threshold Detector Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Threshold Detector Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
data_width	Integer	**Input Data Width:** This parameter indicates the width of the input data across the AXI4-Stream Slave Interface in bits. It can take the values 8, 16, 24 or 32.
default_thresh		**Default Threshold Value at Reset:** This parameter defines the default threshold value at reset.
default_hyst		**Default Hysteresis below Threshold at Reset:** This parameter defines the default hysteresis amount below threshold at reset. It must be less than the **default_thresh** value.
has_det_axis	Boolean	**Has Detect AXI4-Stream output:** This parameter is used to enable (or disable) an AXI4-Stream output of the core with data containing the threshold detection status.
has_irq_out		**Has Interrupt Output:** This parameter is used to enable (or disable) generation of an interrupt output for the rising and falling edges of the detection status signal.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- AXI4-Stream Core Interfaces

3.1 AXI4-Lite Core Interfaces

The AXI4-Stream Threshold Detector Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR Interface is an AXI4-Lite Slave Interface that can be used to access the control and status registers in the AXI4-Stream Threshold Detector Core. Table 3-1 defines the ports in the CSR interface. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This signal will reset the control register to it's initial state.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the AXI4-Stream Threshold Detector Core.
s_axi_csr_awprot	Input	3	**Protection:** The AXI4-Stream Threshold Detector Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The AXI4-Stream Threshold Detector Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Stream Threshold Detector Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr _wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Stream Threshold Detector Core when it is ready to accept data. The value on **s_axi_csr_wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The AXI4-Stream Threshold Detector Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4-Stream Threshold Detector Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the AXI4-Stream Threshold Detector Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Stream Threshold Detector Core.
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on **s_axi_csr_araddr**. The core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Stream Threshold Detector Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The AXI4-Stream Threshold Detector Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4-Stream Threshold Detector Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output	1	**Interrupt:** This is an active high, edge-type interrupt output. This output can be enabled by setting the generic paramter **has_irq_out** to True.

3.2 AXI4-Stream Core Interfaces

The AXI4-Stream Threshold Detector core implements two AXI4-Stream core interfaces across the input and output to receive and transfer data streams. An AXI4-Stream Slave interface at the input is used to receive data streams across the input ports. An AXI4-Stream Master Interface at the output is used to transfer data streams across the output ports.

Table 3-2, defines the ports in the AXI4-Stream Slave and Master interfaces of the AXI4-Stream Threshold Detector Core. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-2: Combined Sample Data/ Timestamp/ Information Streams Interface Port Descriptions

Port	Direction	Width	Description
AXI4-Stream Slave Interface			
axis_aclk	Input	1	**AXI4-Stream Clock**
axis_aresetn			**Reset:** Active Low.
s_axis_tdata		depends on the generic parameter **data_width**	**Input Data:** Unsigned value.
s_axis_tvalid		1	**Input Data Valid:** This signal is asserted by the user logic when data is valid on **s_axis_tdata** bus.
AXI4-Stream Master Interface			
m_axis_detect_tdata	Output	8	**Output Data:** This is the output data generated by the core which carries the detection status. The detection status is defined by the least significant bit of this data output. Other bits are tied to '0'. When bit[0] is '1', it indicates that the input data is greater than the threshold value or the hysteresis value. When it is '0', it indicates that input data fell below the hysteresis value.
m_axis_detect_tvalid		1	**Output Data Valid:** This signal is asserted when data is valid on **m_axis_detect_tdata** bus.

Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the AXI4-Stream Threshold Detector Core. The memory map is provided in Table 4-1.

Table 4-1: Register Space Memory Map

Register Name	Address (Base Address +)	Access	Description
Control Register 0	0x00	R/W	Controls the reset of the state machine within the core.
Threshold Control Register	0x04		Controls the threshold value of the core.
Hysteresis Control Register	0x08		Controls the value of hysteresis amount below threshold.
Detect Status Register	0x0C	R	Indicates the detection status .
Interrupt Enable Register	0x10	R/W	Interrupt enable bits
Interrupt Status Register	0x14	R	Interrupt source status bits
Interrupt Flag Register	0x18	R/Clr	Interrupt flag bits

4.1 Control Register 0

This register controls the reset of the Threshold Detection State Machine within the Threshold Detector core. The Control Register 0 is illustrated in Figure 4-1 and described in Table 4-2.

Figure 4-1: Control Register 0

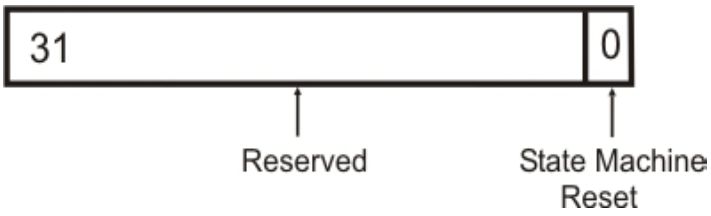

Table 4-2: Control Register 0 (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	rst	0	R/W	**State Machine Reset:** This bit is used to reset the Threshold Detection State Machine of the core. 0 = Run 1 = Reset

4.2 Threshold Control Register

This register controls the threshold value of the core. The Threshold Control Register is illustrated in Figure 4-2 and described in Table 4-3.

Figure 4-2: Threshold Control Register

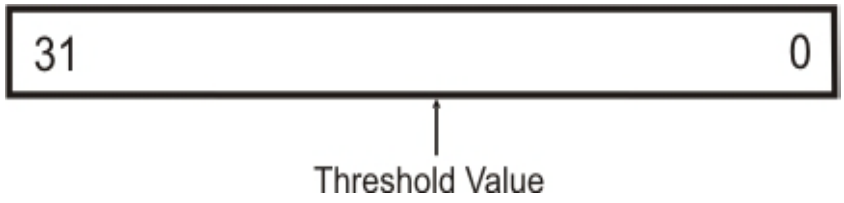

Table 4-3: Threshold Control Register (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:0	thresh	defined by the generic parameter **default_thresh**	R/W	**Threshold value:** These bits indicate the threshold value of the core.

4.3 Hysterisis Control Register

This register controls the value of the hysteresis amount below threshold for the Threshold Detector core. The Hysterisis Control Register is illustrated in Figure 4-3 and described in Table 4-4.

Figure 4-3: Hysterisis Control Register

Table 4-4: Hysterisis Control Register (Base Address + 0x08)

Bits	Field Name	Default Value	Access Type	Description
31:0	hyst	defined by the generic parameter **default_hyst**	R/W	**Hysteresis Below Threshold value:** These bits indicate the hysteresis amount below threshold of the core. This value must be less than the threshold value.

4.4 Detection Status Register

The Threshold Detector Core generates a detection status signal which is '1' when the input data is greater than the threshold value. It remains '1' until the input data falls below the hysterisis value (threshold value minus hysterisis below threshold value). This register indicates the value of the detection status signal. The Detetction Status Register is illustrated in Figure 4-4 and described in Table 4-5.

Figure 4-4: Detection Status Register

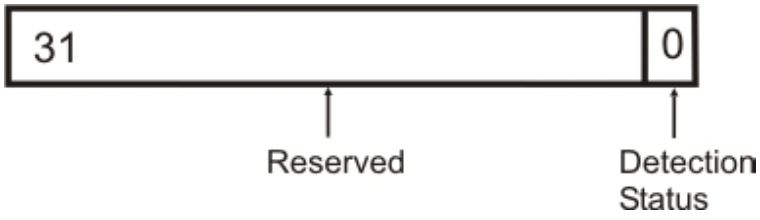

Table 4-5: Detection Status Register (Base Address + 0x0C)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	det	0	R	**Detection Status:** 0 = Input data value below hysterisis value 1 = Input data greater than threshold or hysterisis value

4.5 Interrupt Enable Register

The bits in the interrupt enable register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources. When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source's Interrupt Status Register bit (see Section 4.6). This register is illustrated in Figure 4-5 and described in Table 4-6.

Figure 4-5: Interrupt Enable Register

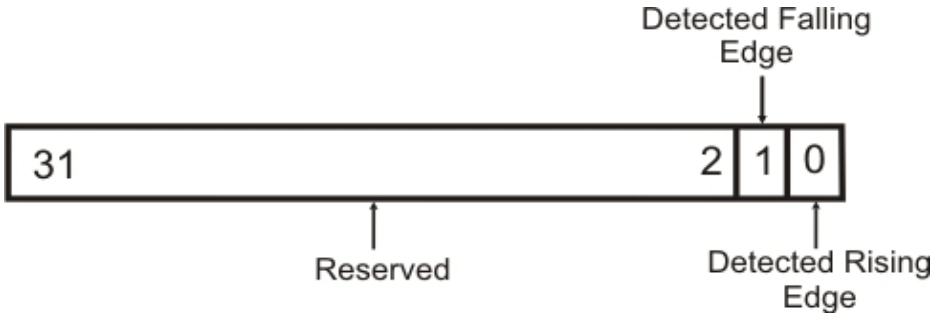

Table 4-6: Interrupt Enable Register (Base Address + 0x10)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	N/A	N/A	**Reserved**
1	det_fe	0	R/W	**Detected Falling Edge:** This bit enables/ disables the detection status signal falling edge interrupt source. The detection status signal falling edge interrupt source is asserted when the detection status signal falls from logic '1' to logic '0'. 0 = Disable interrupt 1 = Enable interrupt
0	det_re			**Detected Rising Edge:** This bit enables/ disables the detection status signal rising edge interrupt source. The detection status signal rising edge interrupt source is asserted when the detection status signal rises from logic '0' to logic '1'. 0 = Disable interrupt 1 = Enable interrupt

4.6 Interrupt Status Register

The Interrupt Status Register has read-only access associated with each interrupt condition. A status bit changes to '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Interrupt Flag Register is set to '1'. A status bit in this register clears to '0' when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic '1' until it is explicitly cleared by the user.

Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases, use the Interrupt Flag Register to see the interrupt conditions that have occurred. This Interrupt Status Register is illustrated in Figure 4-6 and described in Table 4-7.

Figure 4-6: Interrupt Status Register

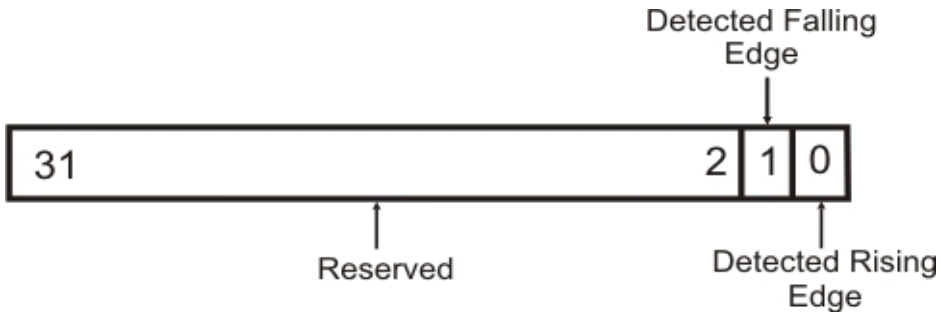

Table 4-7: Interrupt Status Register (Base Address + 0x14)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	N/A	N/A	**Reserved**
1	det_fe	0	R	**Detected Falling Edge:** This bit indicates the status of the detection status signal falling edge interrupt source. The detection status signal falling edge interrupt source is asserted when the detection status signal falls from logic '1' to logic '0'. 0 = No interrupt 1 = Interrupt condition asserted
0	det_re			**Detected Rising Edge:** This bit indicates the status of the detection status signal rising edge interrupt source. The detection status signal rising edge interrupt source is asserted when the detection status signal rises from logic '0' to logic '1'. 0 = No interrupt 1 = Interrupt condition asserted

4.7 Interrupt Flag Register

The Interrupt Flag Register has read/clear access associated with each interrupt condition. When reset, this register has all bits set to '0' (cleared). Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred.

Note that when any status bit in the Interrupt Status Register, changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Interrupt Status Register clears from '1' to '0', the corresponding latched flag bit in this register does not clear, but remains at '1'. To clear the flag bits, write '1's to the desired bits. The flags are not affected by the enable register. This Interrupt Flag Register is illustrated in Figure 4-7 and described in Table 4-8.

Figure 4-7: Interrupt Flag Register

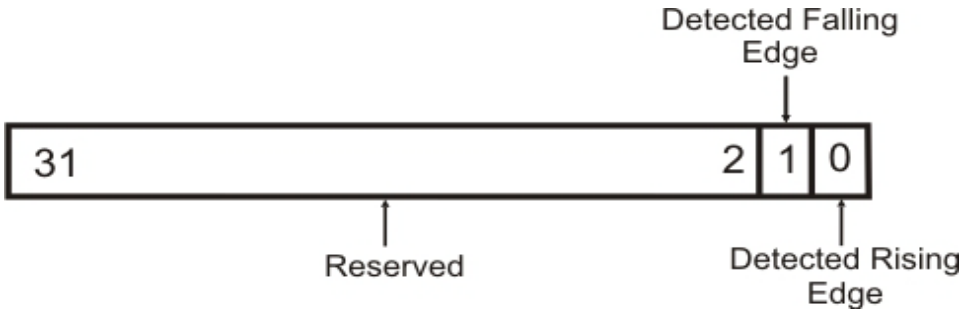

Table 4-8: Interrupt Flag Register (Base Address + 0x18)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	N/A	N/A	**Reserved**
1	det_fe	0	R/Clr	**Detected Falling Edge:** This bit indicates the detection status signal falling edge interrupt flag. **Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch
0	det_re			**Detected Rising Edge:** This bit indicates the detection status signal rising edge interrupt flag. **Read:** 0 = No interrupt 1 = Interrupt latch **Clear:** 1 = Clear latch

Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Threshold Detector Core.

5.1 General Design Guidelines

The AXI4-Stream Threshold Detector core provides the required logic for threshold detection of the input data. It also supports generation of an AXI4-Stream output showing the detection status. This IP core supports AXI4-Lite and AXI4-Stream user interfaces. The user can customize the core by setting the generic parameters, as described in Section 2.5. The core also has control registers which are used to control the threshold detection of the core (see Chapter 4). The output AXI4-Stream is generated after a delay of 3 clock cycles.

5.2 Clocking

AXI4-Stream Clock: **axis_aclk**

This clock is used to clock all ports in the AXI4-Stream Threshold Detector Core.

CSR Clock: **s_axi_csr_aclk**

This clock is the input AXI4-Lite interface clock of the core which is converted using the AXI Clock Converter Core to operate the other modules within the Threshold Detector core in the AXI4-Stream Clock domain.

5.3 Resets

Main reset: **axis_aresetn**

This is an active low reset synchronous with **axis_aclk**.

CSR Reset: **s_axi_csr_aresetn**

This is an active low reset synchronous with **s_axi_csr_clk**. The CSR Interface of the core runs on the CSR reset which is in the AXI4-Stream Clock domain. When asserted, the control/status registers and the interrupt registers are reset.

5.4 Interrupts

This core has an edge-type (rising edge-triggered) interrupt output. It is synchronous with the **s_axis_aclk**. On the rising edge of any interrupt signal, a one-clock-cycle-wide pulse is output from the core on it's **irq** output. Each interrupt event is stored in two registers, accessible on the **s_axi_csr** bus.

The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Register latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared. The Interrupt flags can be cleared by writing '1' to the associated bit's location. All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR ed" onto the **irq** output.

NOTE: All interrupt sources are latched in the interrupt flag register, even when an interrupt source is not enabled to create an interrupt.

NOTE: Because this core uses edge-triggered interrupts, the fact that an interrupt condition may remain active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

5.5 Interface Operation

CSR Interface: This is the Control/Status Register Interface. It is associated with **axis_aclk**. It is a standard AXI4-Lite Slave Interface. See Chapter 4 for the Register Space memory map, for more details on the registers that can be accessed through this interface.

AXI4-Stream Interfaces: This core has AXI4-Stream Slave and Master Interfaces at the input and output respectively to receive and transfer data streams as described in Section 3.2.

5.6 Programming Sequence

This section briefly describes the programming sequence for the AXI4-Stream Threshold Detector Core.

1) Ensure that the Interrupt Flag Register is cleared.

2) Enable the interrupt enable bits based on the user design requirement.

3) Assign the desired values to the generic parameters.

4) Set the control register with the required values.

5) Observe the outputs across the outputs ports.

6) When done, check the Interrupt Flag Register and clear the interrupts.

5.7 Timing Diagrams

The timing diagram for the AXI4-Stream Threshold Detector Core is shown in Figure 6-3. This timing diagram is obtained by running the simulation of the test bench of the core in the Vivado VSim environment. For more details about the test bench, refer to Section 6.5.

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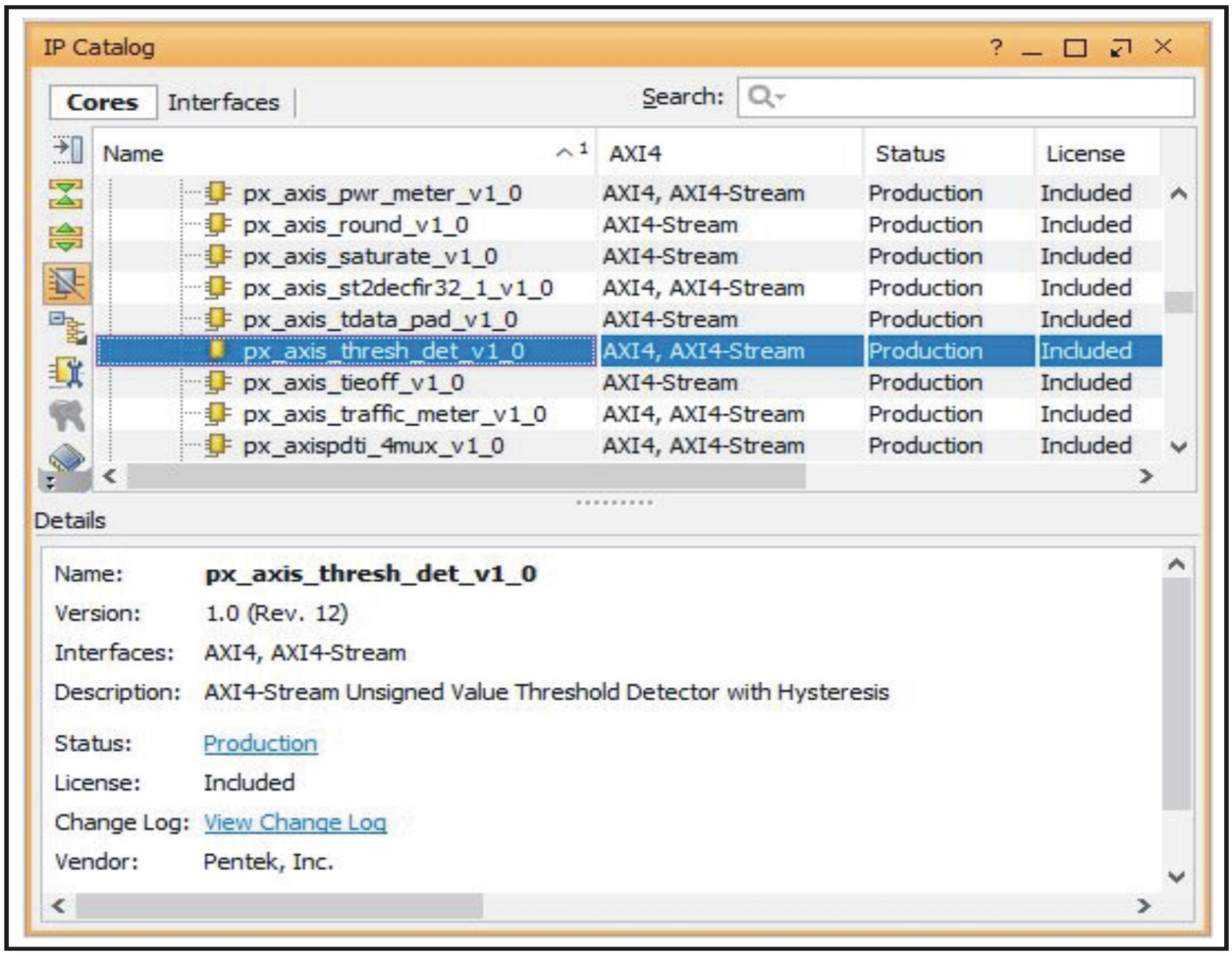
Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Threshold Detector Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_thresh_det_v1_0** as shown in Figure 6-1.

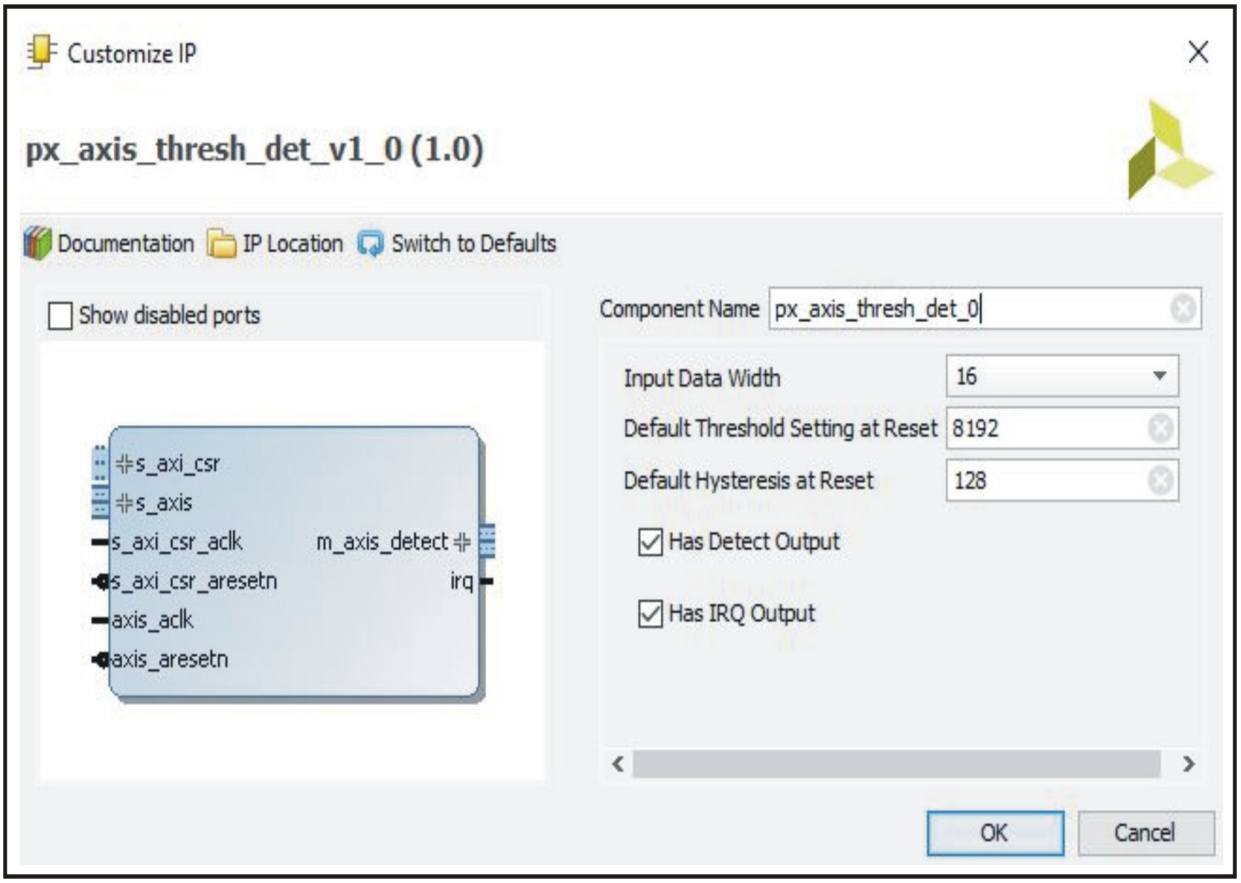
Figure 6-1: AXI4-Stream Threshold Detector Core in Pentek IP



6.1 Pentek IP Catalog (continued)

When you select the **px_axis_thresh_det_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6-2). The core's symbol is the box on the left side.

Figure 6-2: AXI4-Stream Threshold Detector Core IP Symbol



6.2 User Parameters

The user parameter of this core is described in Section 2.5 of this user manual.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Threshold Detector Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Threshold Detector Core. Clock constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The CSR clock (**s_axi_csr_aclk**) and the AXI4-Stream clock (**axis_aclk**) have maximum frequencies of 250 MHz for this core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

The AXI4-Stream Threshold Detector core has a test bench which generates the output waveforms using the Vivado VSim environment. The test bench is designed to run at 250 MHz CSR clock frequency and 200 MHz AXI4-Stream clock frequency. The test bench sets the input data width to 16 bits, default threshold value to 8192, and default hysteresis amount below threshold to 128. It generates both interrupt and AXI4-Stream output. The input data to the core is generated by the test bench using a counter that counts from 0 to 10000 and then back to 0. The state machine is reset once in the beginning by writing 1 to the control register.

6.5 Simulation (continued)

The programming procedure is the same as described in Section 5.6. When run, the simulation produces the results shown in Figure 6-3. The following figure has two markers, one of which is at the origin (as seen on the scale in the bottom of the Figure 6-3) where the input data has reached a value of 8193 and the other marker is at 15ns where the output data stream changes from 0x00 to 0x01 i.e., the core has detected that the input data value is greater than the threshold. This indicates a delay of 3 clock cycles in the generation of the output as mentioned in Section 5.1.

Figure 6-3: AXI4-Stream Threshold Detector Core Test Bench Simulation Output

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.