IP CORE MANUAL

AXI4-Stream Power Meter IP

px_axis_pwr_meter

PENTEK

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Table of Contents

Page

Table of Contents

Page

Chapter 3: Port Descriptions (continued)

Chapter 4: Register Space

Chapter 5: Designing with the Core

Table of Contents

Page

Chapter 6: Designing with the Core (continued)

Chapter 6: Design Flow Steps

Table of Contents

Page

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream Power Meter Core performs a power calculation on an input Combined Sample Data/ Timestamp/ Data Information AXI4-Stream when the data is complex, and has one-sample-per-clock-cycle. It generates an output power AXI data stream by calculating a moving average of the power of input samples.

This core complies with the ARM® AMBA® AXI4 Specification and also provides a control/status register interface. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Power Meter Core.

Features

- Supports calculation of the magnitude of the input samples
- User-programmable averaging filter time constant, and reset mode of the core
- AXI4-Streams across input port follow a format that combines sample data with its time-aligned timestamp and data information
- Generates output ready status signal to indicate that the power average result has reached a stable value and can be used by the user design

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite and AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

The AXI4-Stream Power Meter Core performs a power calculation ($I^2 + Q^2$) on every input sample. The core introduces an **Infinite Impulse Response (IIR)** moving average filter to implement the calculation of moving average of the power for all input samples. The simple IIR filter used for the averaging requires 8 clock cycles of delay between input samples due to the latency in it's Xilinx® DSP48 macro.

The core includes an Accumulator block as shown in Figure 1-1 to average 8 input samples ahead of the IIR filter, in order to reduce it's input rate. A ready output (**rdy_out**) signal is available from the core to indicate that the output power average has almost reached a constant value and is ready for use by the user design.

This IP core also includes a **Register Space** which can be accessed through an AXI4-Lite Interface. It also has an AXI Clock Converter Core which is connected to the AXI4-Lite Interface in order to operate the Register Space in the AXI4-Stream Clock (**axis_aclk**) domain. This core can be programmed to be reset manually or on rising edges of gate/ sync/ PPS signals based on the user requirement. The reset mode can be defined by setting the Control Register 0 bits (see Table 4-2).

This core is compatible only with input AXI4-Streams in the combined Sample Data/ Timestamp/ Information Stream format (see Section 3.2.1), with complex data having one-sample-per-clock-cycle. This type of data streams combine sample data with its time-aligned timestamp and data information (see Section 3.2.1), although timestamp information is not used by this core.

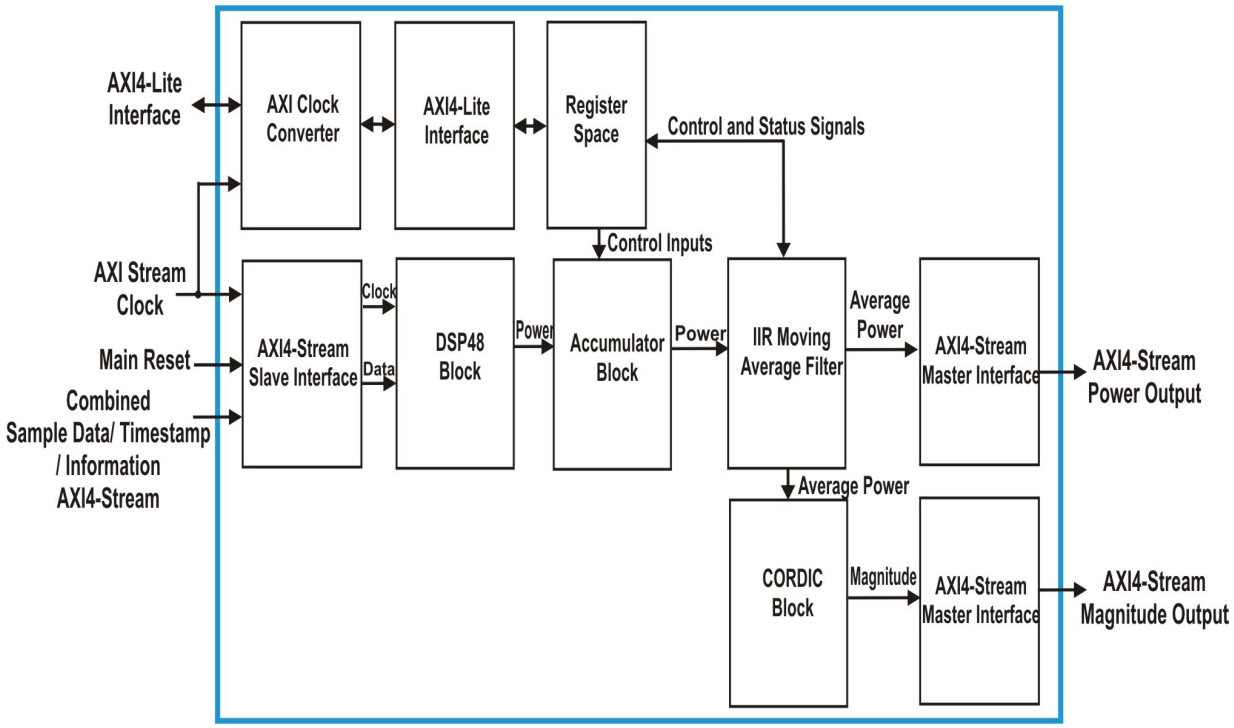
Figure 1-1 is a top level block diagram of the Pentek AXI4-Stream Power Meter Core with both Power and Magnitude output AXI4-Streams. The modules within the block diagram are explained in the later sections of this user manual.

- **AXI Clock Converter Core:** The AXI clock converter core is included in the Xilinx AXI Interconnect Core and is used to connect one AXI memory mapped slave to another AXI memory mapped master which is operating in a different clock domain. In the AXI4-Stream Power Meter core, the AXI Clock converter is used to operate the Register Space in the AXI4-Stream Clock domain.

- **AXI4-Stream Interfaces:** The AXI4-Stream Power Meter core has three AXI4-Stream Interfaces. At the input, an AXI4-Stream Slave Interface is used to receive data streams and at the output two AXI4-Stream Master Interfaces are used to transfer power and magnitude data streams through the output ports. For more details on the AXI4-Stream Interfaces, refer to Section 3.2 AXI4-Stream Core Interfaces.

1.1 Functional Description (continued)

Figure 1-1: AXI4-Stream Power Meter Core Block Diagram



- **AXI4-Lite Interface:** This module implements a 32-bit AXI4-Lite Slave interface to access the Register Space. For additional details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

- **Register Space:** This module contains control and status registers, including Interrupt Enable, Interrupt Status and Interrupt Flag registers. Registers are accessed through the AXI4-Lite interface.

- **DSP48 Block:** The Power Meter Core calculates the power ($I^2 + Q^2$) for every sample before calculating a moving average of the power. This power is calculated in the DSP48 Block. The DSP48 Block has two Xilinx DSP48 Macro cores, which are used to compute $I^2 + Q^2$ for every input sample.

- **Accumulator Block:** A simple IIR filter implemented in the core for calculating the moving average of power, has a delay of 8 clock cycles between input samples, due to latency in the Xilinx DSP48 macro of the filter. Therefore, in order to reduce the input rate to the averaging filter, the accumulator block is used to average 8 input samples. This average of 8 input samples is given as an input to the IIR Moving Average Filter.

1.1 Functional Description (continued)

- **IIR Moving Average Filter:** This block implements a moving average IIR filter used to calculate the moving average of power.

- **CORDIC Block:** The AXI4-Stream Power Meter core includes an optional Xilinx Cordic Core to implement the square root function, required to calculate the magnitude of the averaged input samples. This block is enabled by setting the generic parameter **calc_magnitude** to True (see Table 2-2).

1.2 Applications

The AXI4-Stream Power Meter Core can incorporated into any Kintex Ultrascale FPGA to calculate the moving average of the power of the input data streams.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

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Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Power Meter Core has bus interfaces that comply with the *ARM AMBA AXI4-Lite Protocol Specification* and the *AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Power Meter Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Stream Power Meter Core has two incoming clock signals. The AXI4-Stream clock and the clock across the AXI4-Lite interface both have a maximum frequencies of 250MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream Power Meter Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	876
Flip-Flops	1996
Memory LUTs	114
DSP	10

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream Power Meter Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Power Meter Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
calc_magnitude	Boolean	**Calculate Magnitude:** This parameter is used to enable the calculation of magnitude of the averaged input data samples.
has_axis_pwr_out		**Has AXI4-Stream Power Output:** This parameter is used to enable (or disable) the output of the average power calculated by the core, through a Power Output AXI4-Stream Master Interface.
has_axis_mag_out		**Has AXI4-Stream Magnitude Output:** This parameter is used to enable (or disable) the output of the magnitude calculated by the core, through a Magnitude Output AXI4-Stream Master Interface. This parameter is valid only when the generic parameter **calc_magnitude** is set to True.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- AXI4-Stream Core Interfaces
- I/O Signals

3.1 AXI4-Lite Core Interfaces

The AXI4-Stream Power Meter Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4-Lite Slave Interface that can be used to access the control and status registers in the AXI4-Stream Power Meter Core. Table 3-1 defines the ports in the CSR interface. See Chapter 4 for a Control/Status Register memory map and bit definitions. See the *AMBA AXI4-Lite Specification* for more details on operation of the AXI4-Lite interfaces.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	**Clock**
s_axi_csr_aresetn	Input	1	**Reset:** Active low. This signal will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	7	**Write Address:** Address used for write operations. It must be valid when **s_axi_csr_awvalid** is asserted and must be held until **s_axi_csr_awready** is asserted by the AXI4-Stream Power Meter Core.
s_axi_csr_awprot	Input	3	**Protection:** The AXI4-Stream Power Meter Core ignores these bits.
s_axi_csr_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_csr_awaddr**. The AXI4-Stream Power Meter Core asserts **s_axi_csr_awready** when it is ready to accept the address. The **s_axi_csr_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_csr_awready**.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_awready	Output	1	**Write Address Ready:** This output is asserted by the AXI4-Stream Power Meter Core when it is ready to accept the write address.The address is latched when **s_axi_csr_awvalid** and **s_axi_csr_awready** are high on the same cycle.
s_axi_csr_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_csr_awaddr** when **s_axi_csr_wvalid** and **s_axi_csr _wready** are both asserted. The value must be valid when **s_axi_csr_wvalid** is asserted and held until **s_axi_csr_wready** is also asserted.
s_axi_csr_wstrb	Input	4	**Write Strobes:** This signal, when asserted, indicates the number of bytes of valid data on the **s_axi_csr_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_csr_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle.
s_axi_csr_wready	Output	1	**Write Ready:** This signal is asserted by the AXI4-Stream Power Meter Core when it is ready to accept data. The value on **s_axi_csr _wdata** is written into the register at address **s_axi_csr_awaddr** when **s_axi_csr_wready** and **s_axi_csr_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	**Write Response:** The AXI4-Stream Power Meter Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the AXI4-Stream Power Meter Core when the write operation is complete and the Write Response is valid. It is held until **s_axi_csr_bready** is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	**Read Address:** Address used for read operations. It must be valid when **s_axi_csr_arvalid** is asserted and must be held until **s_axi_csr_arready** is asserted by the AXI4-Stream Power Meter Core.
s_axi_csr_arprot	Input	3	**Protection:** These bits are ignored by the AXI4-Stream Power Meter Core
s_axi_csr_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_csr_araddr**. The AXI4-Stream Power Meter Core asserts **s_axi_csr_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_csr_arready**.
s_axi_csr_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Stream Power Meter Core when it is ready to accept the read address. The address is latched when **s_axi_csr_arvalid** and **s_axi_csr_ arready** are high on the same cycle.
s_axi_csr_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_csr_araddr** when **s_axi_csr_arvalid** and **s_axi_csr_arready** are high on the same cycle.
s_axi_csr_rresp	Output	2	**Read Response:** The AXI4-Stream Power Meter Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_csr_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_csr_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the AXI4-Stream Power Meter Core when the read is complete and the read data is available on **s_axi_csr_rdata**. It is held until **s_axi_csr_ rready** is asserted by the user logic.
s_axi_csr_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output	1	**Interrupt:** This is an active high, edge-type interrupt output.

3.2 AXI4-Stream Core Interfaces

The AXI4-Stream Power Meter Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- Combined Sample Data/ Timestamp/ Information Stream (PDTI) Interface: This core implements an combined Sample Data/ Timestamp/ Information AXI4-Stream Interface across the input to receive PDTI AXI4-Streams.
- Power Output (PWR) Interface: This is an AXI4-Stream Interface used to transfer the generated power average data streams across the output ports.
- Magnitude Output (MAG) Interface: This is an optional interface and is used to transfer the magnitude of the averaged data across the output ports.

3.2.1 Combined Sample Data/ Timestamp/ Information Streams (PDIT) Interface

The Pentek Jade series board products have AXI4-Streams that follow a combined Sample data/ Timestamp/ Information Stream format. This type of data stream combines sample data with its time-aligned timestamp and data information. This interface is an AXI4-Stream Slave Interface across the input to receive AXI4-Streams in the above mentioned format.

Table 3-2 defines the ports in the Combined Sample Data/ Timestamp/ Information AXI4-Stream Interface. This interface is an AXI4-Stream Slave Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-2: Combined Sample Data/ Timestamp/ Information Stream Interface Port Descriptions

Port	Direction	Width	Description
axis_aclk	Input	1	**AXI4-Stream Clock**
axis_aresetn			**Reset:** Active Low.
s_axis_pdti_tdata		32	**Input Data:** This is the input data stream to the core. **s_axis_pdti_tdata [15:0] - I [15:0]** **s_axis_pdti_tdata [31:16] - Q[15:0]**

Table 3-2: Combined Sample Data/ Timestamp/ Information Stream Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axis_pdti_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on **s_axis_pdti_tdata**.
s_axis_pdti_tuser		128	**Sideband Information:** This is the user defined sideband information transmitted alongside the data stream. It contains timestamp, Gate/ Sync/ PPS positions and data information. In this core only the Gate/ Sync/ PPS events information is used. **tuser [64] - Gate** **tuser [72] - Sync** **tuser [80] - PPS**

3.2.2 Power Output (PWR) Interface

The Power Output Interface is an AXI4-Stream Master Interface across the output to transfer the generated power average AXI data streams. This interface can be enabled (or disabled) by the generic parameter **has_axis_pwr_out** (see Table 2-2).

Table 3-3 defines the ports in the AXI4-Stream Master Power Output Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-3: Power Output Interface Port Descriptions			
Port	**Direction**	**Width**	**Description**
m_axis_pwr_tdata	Output	32	**Power Output:** This is the moving average of power calculated for the input samples. It is a 32-bit unsigned number.
m_axis_pwr_tvalid		1	**Power Output Valid:** Asserted when data is valid on **m_axis_pwr_tdata**.

3.2.3 Magnitude Output (MAG) Interface

The Magnitude Output Interface is an AXI4-Stream Master Interface across the output to transfer the generated magnitude output of the averaged input samples. This interface is enabled (or disabled) by setting the generic parameter **has_axis_mag_out** to True (see Table 2-2).

Table 3-4 defines the ports in the AXI4-Stream Master Magnitude Output Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-4: Magnitude Output Interface Port Descriptions

Port	Direction	Width	Description
m_axis_mag_tdata	Output	16	**Magnitude Output:** This is the output magnitude of averaged samples. It is a 16-bit unsigned number.
m_axis_mag_tvalid		1	**Power Output Valid:** Asserted when data is valid on **m_axis_mag_tdata**.

3.3 I/O Signals

The I/O port/signal descriptions of the top level module of the AXI4-Stream Power Meter core are discussed in Table 3-5.

Table 3-5: I/O Signals

Port	Direction	Width	Description
rdy_out	Output	1	**Ready Output:** This is Ready status output from the AXI4-Stream Power Meter core. When High, it indicates that the power average output is almost constant and is ready for use by the user design.

Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the AXI4-Stream Power Meter Core. The memory map is provided in Table 4-1.

Table 4-1: Register Space Memory Map

Register Name	Address (Base Address +)	Access	Description
Control Register 0	0x00	R/W	Control the reset mode of the core.
Average Control Register	0x04		Controls the time constant of the averaging filter.
Power Reading Register	0x08	R	Indicates the power average output reading.
Magnitude Reading Register	0x0C		Indicates the magnitude output reading.
Interrupt Enable Register	0x10	R/W	Interrupt enable bits
Interrupt Status Register	0x14	R	Interrupt source status bits
Interrupt Flag Register	0x18	R/Clr	Interrupt flag bits

4.1 Control Register 0

This control register is used to control the power measurement reset, measurement when gate is active, and the reset mode of the Power Meter core. The Control Register 0 is illustrated in Figure 4-1 and described in Table 4-2.

Figure 4-1: Control Register 0

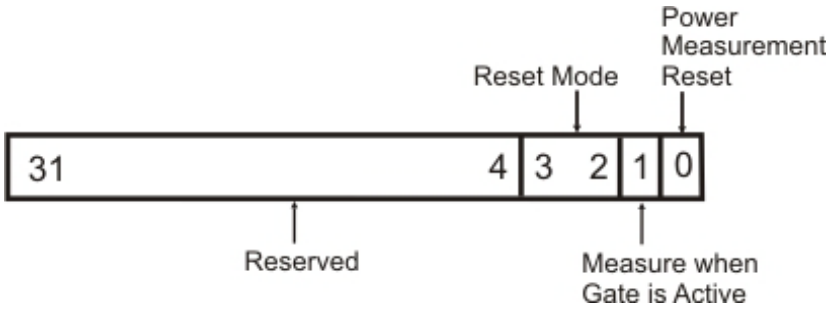

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Table 4-2: Control Register 0 (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:4	Reserved	N/A	N/A	**Reserved**
3:2	reset_mode	00	R/W	**Reset Mode:** These bits are used to define the reset mode of the Power Meter core. 00 - Manual Reset Only (defined by bit[0] - **pwr_reset**) 01 - Reset on Sync sinal 10 - Reset on Rising Edge of Gate signal 11 - Reset on Rising Edge of PPS signal
1	gate_active	0		**Measure only when Gate is Active:** This bit is used to enable measurement only when the Gate signal is active. It is used to set the data valid signal with respect to the Gate signal. 0 = Disable 1 = Enable
0	pwr_reset			**Power Measurement Reset:** This bit is used to manually control the reset of the core. 0 = Run 1 = Reset

4.2 Average Control Register

The Power Meter core includes a moving average filter to calculate the average power. This register controls the time constant of the averaging filter. This value also determines the number of samples averaged before the ready output signal goes High. This register is illustrated in Figure 4-2 and described in Table 4-3.

Figure 4-2: Average Control Register

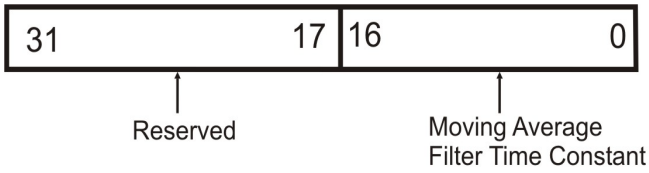

Table 4-3: Average Control Register (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:17	Reserved	N/A	N/A	**Reserved**

16:0	k	0x00000	R/W	**Moving Average Filter Time Constant:** This is the moving average filter time constant. This value also determines the number of samples have been averaged before the ready signal goes High. The most significant bit has the highest priority and thereby the number of samples is determined based on the bit that is High relative to the most significant bit position.In this core the number of samples for k[0], k[1] and k[16] are shown below:
				k[0] = 1 => no. of samples = 4,194,304;
				k[1] = 1 => no. of samples = 2,097,152;
				k[16] = 1 => no. of samples = 64;
				The number of samples for the intermediate k values can be computed from the values listed above.

4.3 Power Reading Register

This register is a read-only status register which indicates the average power calculated by the core for every sample. The Power Reading Register is illustrated in Figure 4-3 and described in Table 4-4.

Figure 4-3: Power Reading Register

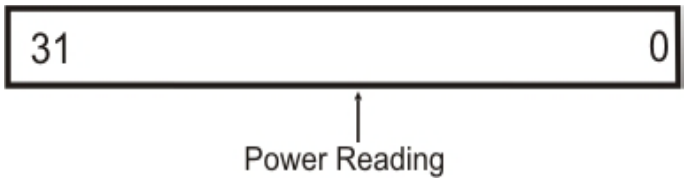

Table 4-4: Power Reading Register (Base Address + 0x08)

Bits	Field Name	Default Value	Access Type	Description
31:0	pwr	0x00000000	R	**Power Reading:** These bits indicate the averaged power reading of the core for every sample.

4.4 Magnitude Reading Register

This register is a read-only status register which indicates the magnitude of the averaged data calculated by the core for every sample. The Magnitude Reading Register is illustrated in Figure 4-4 and described in Table 4-5.

Figure 4-4: Magnitude Reading Register

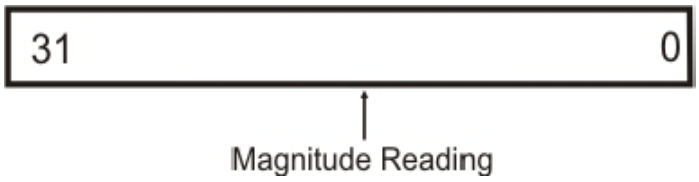

Table 4-5: Magnitude Reading Register (Base Address + 0x0C)

Bits	Field Name	Default Value	Access Type	Description
31: 16	reserved	N/A	N/A	**Reserved**
15:0	mag	0x0000 0000	R	**Magnitude Reading:** These bits indicate the averaged magnitude reading of the core for every sample.

4.5 Interrupt Enable Register

The bits in the Interrupt Enable Register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources. When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source's Interrupt Status Register bit (See Section 4.6). This register is illustrated in Figure 4-5 and described in Table 4-6.

Figure 4-5: Interrupt Enable Register

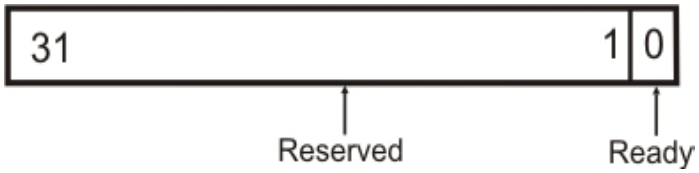

Table 4-6: Interrupt Enable Register (Base Address + 0x10)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	rdy	0	R/W	**Ready:** This bit enables/ disables the ready interrupt source. The ready interrupt source indicates that the averaged power output is ready on the output power data bus for use. 0 = Disable interrupt 1 = Enable interrupt

4.6 Interrupt Status Register

The Interrupt Status Register has read-only access associated with each interrupt condition. A status bit changes to '1' when the source interrupt occurs. When a status bit in this register changes to '1' the corresponding flag bit in the Interrupt Flag Register is set to '1'. A status bit in this register clears to '0' when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic '1' until it is explicitly cleared by the user.

Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases, use the Interrupt Flag Register to see the interrupt conditions that have occurred. This Interrupt Status Register is illustrated in Figure 4-6 and described in Table 4-7.

Figure 4-6: Interrupt Status Register

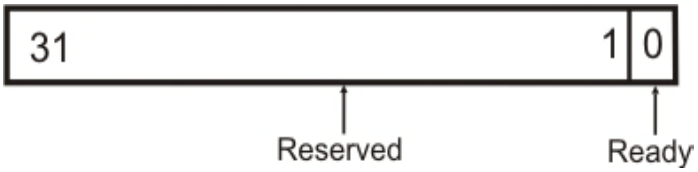

Table 4-7: Interrupt Status Register (Base Address + 0x14)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	rdy	0	R	**Ready:** This bit indicates the status of the ready interrupt source. The ready interrupt source indicates that the averaged power output is ready on the output power data bus for use. 0 = No interrupt 1 = Interrupt condition asserted

4.7 Interrupt Flag Register

The Interrupt Flag Register has read/clear access associated with each interrupt condition. When reset, this register has all bits set to '0' (cleared). Each flag bit in this register latches an interrupt occurrence. A '1' in any flag bit in this register indicates that an interrupt has occurred.

Note that when any status bit in the Interrupt Status Register, changes to '1' the corresponding flag bit in this register will also be set to '1'. However, when a status bit in the Interrupt Status Register clears from '1' to '0', the corresponding latched flag bit in this register does not clear, but remains at '1'. To clear the flag bits, write '1's to the desired bits. The flags are not affected by the enable register. This Interrupt Flag Register is illustrated in Figure 4-7 and described in Table 4-8.

Figure 4-7: Interrupt Flag Register

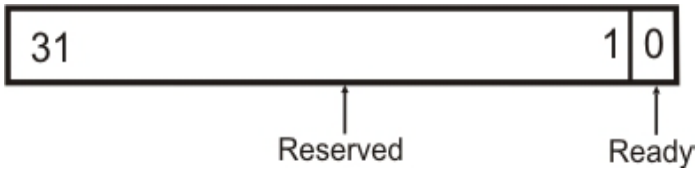

Table 4-8: Interrupt Flag Register (Base Address + 0x18)

Bits	Field Name	Default Value	Access Type	Description
31:1	Reserved	N/A	N/A	**Reserved**
0	rdy	0	R/Clr	**Ready:** This bit indicates the ready interrupt flag. The ready interrupt source indicates that the averaged power output is ready on the output power data bus for use. **Read:** 0 = No interrupt 1 = Interrupt latched **Clear:** 1 = Clear latch

Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Power Meter Core.

5.1 General Design Guidelines

The AXI4-Stream Power Meter core provides the required logic to generate moving average of the power calculated for the input samples. It also generates the magnitude of the averaged data when the generic parameter **calc_magnitude** is set to True. This IP core supports both AXI4-Lite and AXI4-Stream user interfaces. The user can customize the core by setting the generic parameters based on the application requirement as described in Section 2.5.

5.2 Clocking

AXI4-Stream Clock: **axis_aclk**

This clock is used to clock all ports of the core.

CSR Clock: **s_axi_csr_aclk**

This clock is the input AXI4-Lite interface clock to the core which is converted using the AXI Clock converter core to operate the other modules within the AXI4-Stream Power Meter Core in the AXI4-Stream Clock domain.

5.3 Resets

Main reset: **axis_aresetn**

This is an active low reset synchronous with **axis_aclk**.

CSR Reset: **s_axi_csr_aresetn**

This is an active low reset synchronous with **s_axi_csr_clk**. The CSR interface of the core runs on the CSR reset in the AXI4-Stream Clock domain.

5.4 Interrupts

This core has an edge-type (rising edge-triggered) interrupt output. It is synchronous with the **s_axis_aclk**. On the rising edge of any interrupt signal, a one clock cycle wide pulse is output from the core on it's **irq** output. Each interrupt event is stored in two registers, accessible on the **s_axi_csr** bus.

The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Register latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared. The Interrupt flags can be cleared by writing '1' to the associated bit's location. All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR ed" onto the **irq** output.

NOTE: All interrupt sources are latched in the interrupt flag register, even when an interrupt source is not enabled to create an interrupt.

NOTE: Because this core uses edge-triggered interrupts, the fact that an interrupt condition may remain active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

5.5 Interface Operation

CSR Interface: This is the Control/Status Register Interface snd is associated with **axis_aclk**. It is a standard AXI4-Lite Slave Interface. See Chapter 4 for the control register memory map, which provides more details on the registers that can be accessed through this interface.

Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interfaces: This is an AXI4-Stream Slave interface to receive AXI4-Streams in the PDTI format and is associated with **axis_aclk**. For more details about this interface, refer to Section 3.2.1.

Power Output (PWR) Interface: This is an AXI4-Stream Master Interface across the output to transfer the average power output data stream generated by the Power Meter core. It is associated with **axis_aclk**. For more details about this interface, refer to Section 3.2.2.

Magnitude Output (PWR) Interface: This is an AXI4-Stream Master Interface across the output to transfer the magnitude of the averaged data generated by the Power Meter core. It is associated with **axis_aclk**. For more details about this interface, refer to Section 3.2.3.

5.6 Programming Sequence

This section briefly describes the programming sequence of registers in the AXI4-Stream Power Meter Core.

1) Set the Average Control Register with the required value of time constant.

2) Ensure that the Interrupt Flag Register is cleared.

3) Enable the interrupt enable bits based on the user design requirement.

4) Assign desired values to the generic parameters

5) Set Control Register 0 with the reset and reset mode values.

6) Observe the outputs across the outputs ports and the status registers.

7) When done check the Interrupt Flag Register and clear the interrupts.

5.7 Timing Diagrams

The timing diagrams for the AXI4-Stream Power Meter Core are shown in Figure 6-3. This timing diagram is obtained by running the simulation of the test bench of the core in Vivado VSim environment. For more details about the testbench please refer to Section 6.5.

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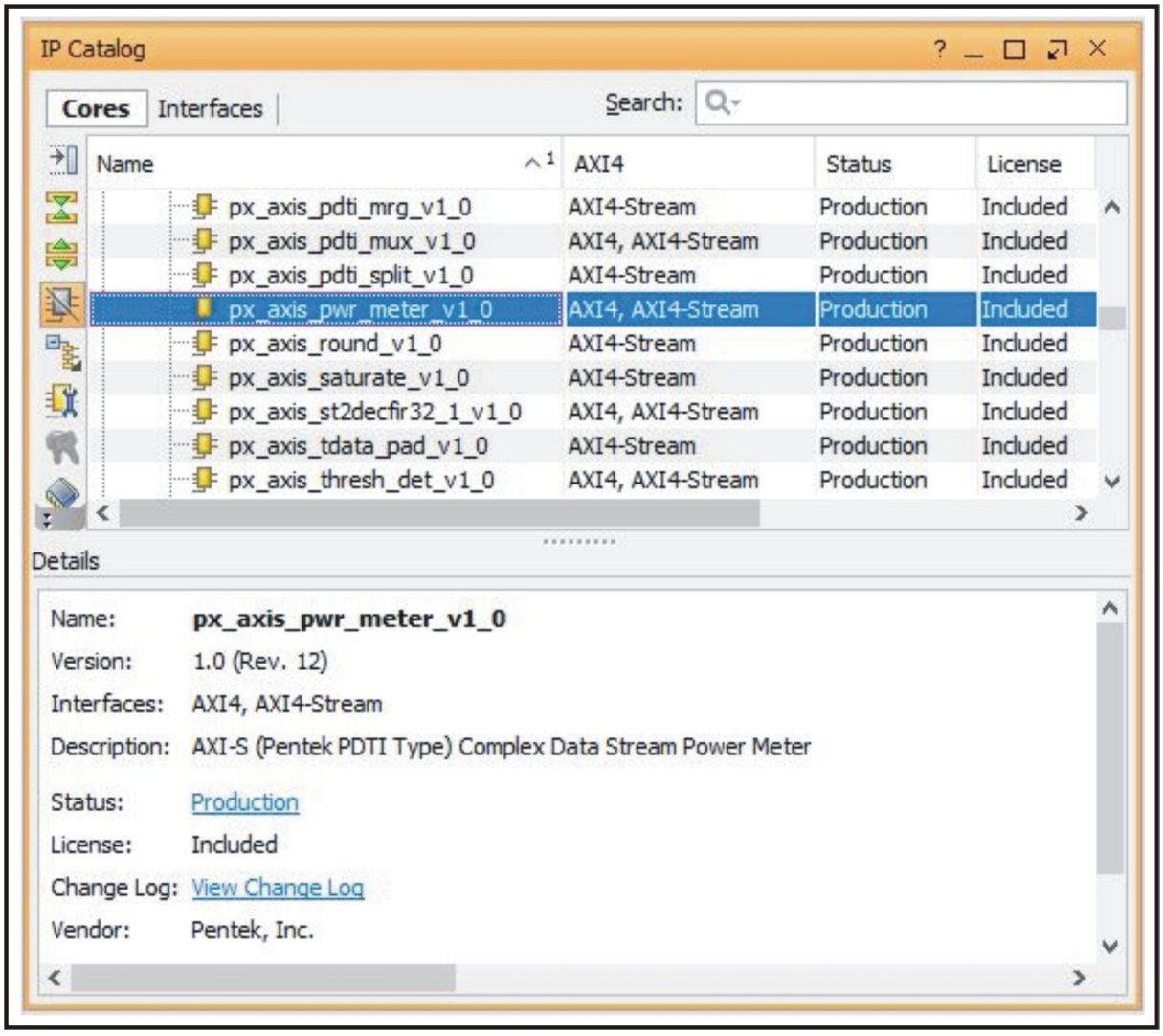
Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Power Meter Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_pwr_meter_v1_0** as shown in Figure 6-1.

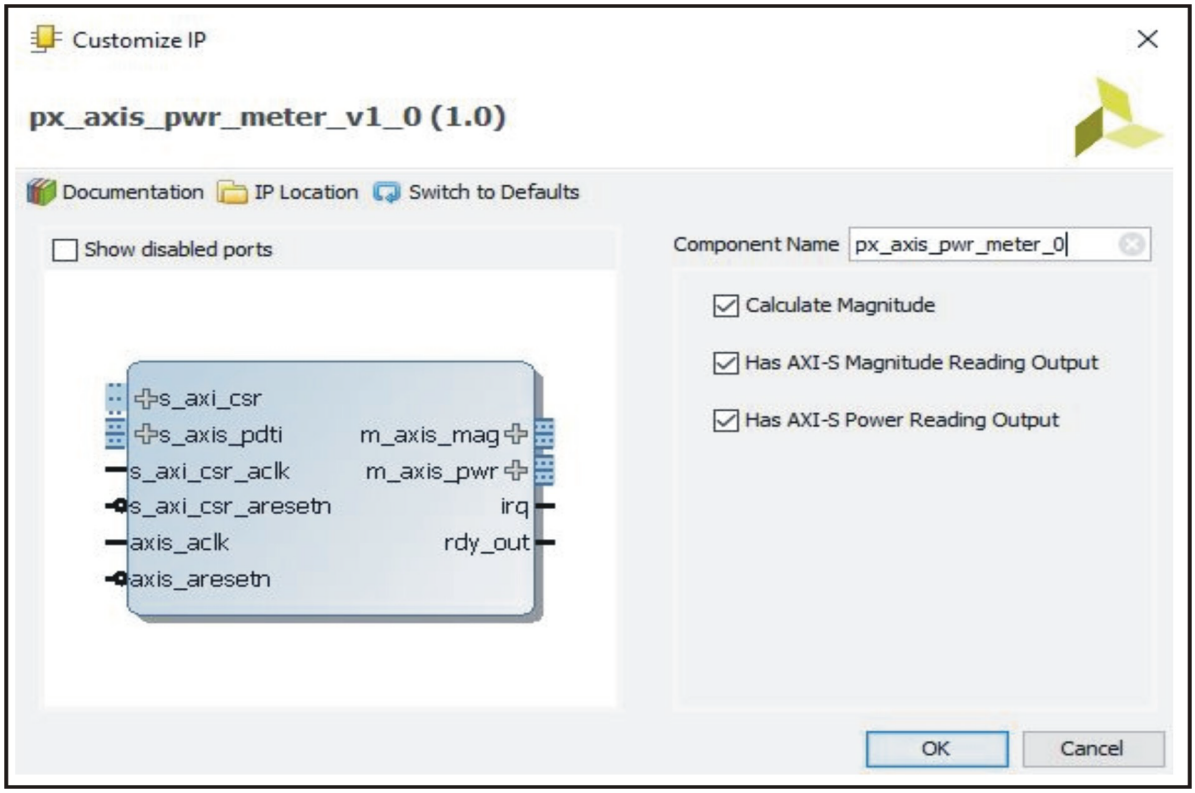
Figure 6-1: AXI4-Stream Power Meter Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the **px_axis_pwr_meter_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6-2). The core's symbol is the box on the left side.

Figure 6-2: AXI4-Stream Power Meter Core IP Symbol



6.2 User Parameters

The user parameter of this IP core are described in Section 2.5 of this user manual.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

6.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Power Meter Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Power Meter Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale and Virtex-7 FPGAs.

Clock Frequencies

The CSR clock (**s_axi_csr_aclk**) and the AXI4-Stream clock (**s_axis_aclk**) have maximum frequencies of 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

The AXI4-Stream Power Meter core has a test bench which generates the output waveforms using the Vivado VSim environment. The test bench is designed to run at 250MHz CSR clock frequency and 250 MHz of AXI4-Stream clock frequency. The test bench calculates the magnitude and has both power, and magnitude output AXI4-Streams. It has a time constant of 0.1 and a manual reset. The time constant defined is converted into a 17-bit vector by the test bench. The input data to the core is 0x00008000. The programming procedure is the same as described in Section 5.6. When run, the simulation produces the results shown in Figure 6-3.

6.5 **Simulation** (continued)

Figure 6-3: AXI4-Stream Power Meter Core Test Bench Simulation Output

6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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