IP CORE MANUAL

AXI4-Stream Merge IP

px_axis_pdti_mrg

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Stream Merge Core enables concatenation of raw I/O data, timestamp, and data information AXI4-Streams into a combined Data/ Timestamp/ Information AXI4-Stream output.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Stream Merge Core.

Features

- Supports AXI4-Stream user interfaces
- Software programmable width of input data streams
- Supports up to 32 bytes wide input data stream
- Delays of up to 31 clock cycles can be introduced into the input data streams
- AXI4-Stream output is the I/O raw data combined with its time-aligned timestamp and data information

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided[b]
Simulation Model	N/A
Supported S/W Driver	N/A
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

The AXI4-Streams of the Pentek Jade series boards follow the following formats:

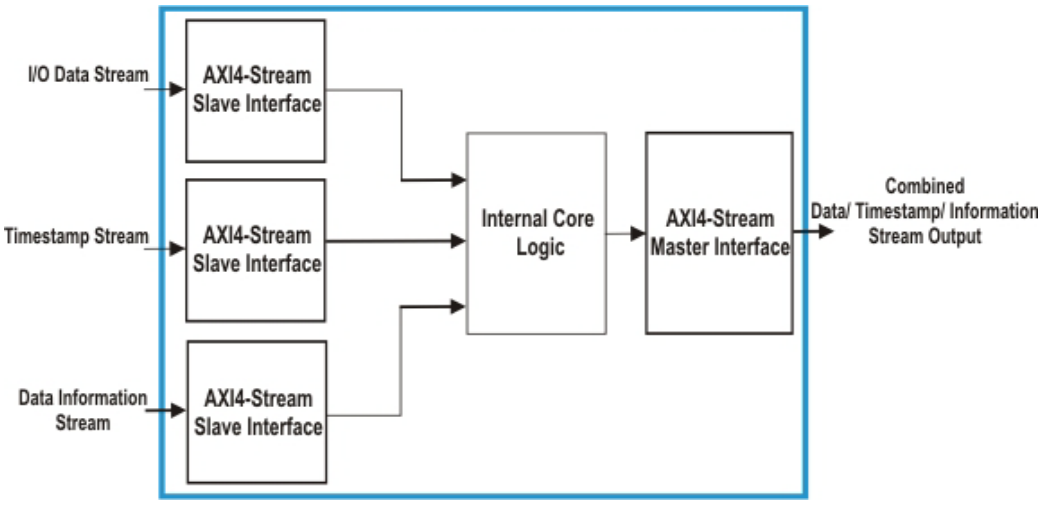
- **Input/Output Raw Data (PD) Streams:** These are AXI4-Streams that which contain only I/O data.
- **Timestamp (PTS) Streams:** These are AXI4-Streams which contain only timestamps and a time-aligned copy of the timing events that created them.
- **Data Information (PI) Streams:** These are AXI4-Streams that indicate the data type and packing information of the I/O data streams.
- **Combined Data/ Timestamp/ Information Streams:** These are AXI4-Streams that combine the data with its time-aligned timestamp, and data information streams.

For more details about these AXI4-Stream formats refer to Section 3.1. The AXI4-Stream Merge Core accepts I/O Raw Data Streams, Timestamp Streams, Data Information Streams and generates a combined Data/ Timestamp/ Information AXI4-Stream output.

The width of the I/O data stream can be defined by the user using the generic parameter **data_byte_width** (see Section 2.5). The incoming AXI4-Streams can be delayed based on the user requirement by defining their respective generic parameters.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream Merge Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Stream Merge Core Block Diagram



1.1 Functional Description (continued)

- **AXI4-Stream Interface:** The AXI4-Stream Merge Core has four AXI4-Stream Interfaces. At the input, AXI4-Stream Slave Interfaces are used to receive AXI4-Streams and at the output AXI4-Stream Master Interfaces are used to transfer data streams through the output ports. For more details about the AXI4-Stream Interfaces refer to Section 3.1 AXI4-Stream Core Interfaces.

1.2 Applications

The AXI4-Stream Merge core can be incorporated into any Kintex Ultrascale FPGA, where concatenation of Data, Timestamp and Information Streams into a combined output AXI4-Stream is required.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream Merge Core has a bus interface that complies with the *ARM AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Stream Merge Core is limited only by the clock frequency of the AXI4-Streams in the user design.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream Merge Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	17
Flip-Flops	66
Memory LUTs	17

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream Merge Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream Merge Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core. The input delay generic parameters are used to align the incoming AXI4-Streams to generate the output AXI4-Stream.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
data_byte_width	Integer	**Data Byte Width:** This parameter indicates the width of the input data stream across the AXI4-Stream Slave Interface in bytes. It can range from 1 to 32 bytes.
data_stream_delay		**I/O Data Stream Delay:** This parameter defines the delay to be introduced to the I/O Data Stream input. It can range from 0 to 31.
time_stream_delay		**Timestamp Stream Delay:** This parameter defines the delay to be introduced to the Timestamp Stream input. It can range from 0 to 31.
info_stream_delay		**Data Information Stream Delay:** This parameter defines the delay to be introduced to the Data Information Stream input. It can range from 0 to 31.

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- AXI4-Stream Core Interfaces

3.1 AXI4-Stream Core Interfaces

The AXI4-Stream Merge Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- I/O Data (PD) Interface: This core has an I/O Data AXI4-Stream Slave Interface at the input of the core to receive I/O data streams.
- Timestamp (PTS) Interface: The AXI4-Stream Merge Core has a Timestamp Interface to receive timestamp data streams.
- Data Information (PI) Stream Interface: This core has a Data Information Interface to receive the data type and packing information of the AXI data streams.
- Combined Data/ Timestamp/ Information (PDTI) Interface: This core implements a Combined Data/ Timestamp/ Information AXI4-Stream across the output to transfer the concatenated streams.

3.1.1 I/O Data (PD) Interface

The AXI4-Stream Merge core implements an I/O Data Interface across the input to receive I/O data streams. This is an AXI4-Stream Slave interface.

Table 3-1 defines the ports in the AXI4-Stream Slave I/O Data Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-1: I/O Data Interface Port Descriptions

Port	Direction	Width	Description
s_axis_aclk	Input	1	**AXI4-Stream Clock**
s_axis_aresetn			**Reset:** Active Low.

Table 3-1: I/O Data Interface Port Descriptions (Continued)			
Port	**Direction**	**Width**	**Description**
s_axis_pd_tdata	Input	depends on the generic parameter **data_byte_width**	**Input Data:** This is the input data stream to the core.
s_axis_pd_tvalid	Input	1	**Input Data Valid:** Asserted when data is valid on **s_axis_pd_tdata**. This signal is mapped to the output **m_axis_pdti_tvalid**.

3.1.2 Timestamp (PTS) Interface

The Timestamp Interface is used to accept timestamp streams which contains only timestamp and a time-aligned copy of the timing events that created the timestamp. This is an AXI4-Stream Slave Interface.

Table 3-2 defines the ports in the Timestamp Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-2: Timestamp Interface Port Descriptions			
Port	**Direction**	**Width**	**Description**
s_axis_aclk	Input	1	**AXI4-Stream Clock**
s_axis_aresetn			**Reset:** Active Low.
s_axis_pts_tdata	Input	64	**Timestamp Data:** This is the timestamp of the data on the I/O Data Bus across the I/O Data Interface.
s_axis_pts_tvalid		1	**Data Valid:** Asserted when data is valid on **s_axis_pts_tdata**.
s_axis_pts_tuser		24	**Sideband Data:** These bits indicate the gate/sync/ PPS positions of the timing events that created the timestamps. **tuser[7:0] - Gate positions** **tuser[15:8] - Sync positions** **tuser[23:16] - PPS positions**

3.1.3 Data Information (PI) Interface

The AXI4-Stream Merge Core has a Data Information Interface across the input to receive data streams which allow the identification of the data type and packing of incoming data on the I/O Data bus. This is an AXI4-Stream Slave interface.

Table 3-3 defines the ports in the Data Information Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-3: Data Information Interface Port Descriptions

Port	Direction	Width	Description
s_axis_aclk	Input	1	**AXI4-Stream Clock**
s_axis_aresetn			**Reset:** Active Low.
s_axis_pi_tdata	Input	16	**Data Information Bus:** The data from the Data Information bus provides the following information: **tdata[3:0] - Samples/ Cycle** **tdata[4] - I/Q data of the sample=> 0 = I; 1 = Q** **tdata[6:5] - Data Format => 0 = 8-bit samples;** **1 = 16-bit;** **2 = 24-bit;** **3 = 32-bit** **tdata[7] - Data Type => 0 = Real; 1 = I/Q** **tdata[15:8] - channel [7:0]** Note: The bits [15:8] define the channel number in the user design from where the data is being received.
s_axis_pi_tvalid		1	**Data Valid:** Asserted when data is valid on **s_axis_pi_tdata**.

3.1.4 Combined Data/ Timestamp/ Information (PDTI) Interface

The Combined Data/ Timestamp/ Information Interface is used to transfer output AXI4-Streams generated by combining the input AXI4-Streams. This is an AXI4-Stream Master Interface.

Table 3-4 defines the ports in the Combined Data/ Timestamp/ Data Information Interface. See the *AMBA AXI4-Stream Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-4: Combined Data/ Timestamp/ Information Interface Port Descriptions

Port	Direction	Width	Description
m_axis_pdti_tdata	Output	depends on the generic parameter **data_byte_width**	**Output Data:** This is the output data of the AXI4-Stream Merge Core obtained from the I/O Data Interface.
m_axis_pdti_tvalid		1	**Output Data Valid:** Asserted when data is valid on **m_axis_pdti_tdata**.
m_axis_pdti_tuser		128	**Output Sideband Information:** This is the sideband information transmitted alongside the data stream. **tuser [63:0] - Timestamp[63:0]** **tuser [71:64] - Gate Positions** **tuser [79:72] - Sync Positions** **tuser [87:80] - PPS Positions** **tuser [91:88] - Samples per clock cycle** **tuser[92] - I/Q data of the sample => 0 = I; 1 = Q** **tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit; 2 = 24-bit; 3 = 32-bit** **tuser [95] - Data Type => 0 = Real; 1 = I/Q** **tuser [103:96] - channel [7:0]** **tuser [127:104] - Reserved** Note: The bits [103:96] define the channel number in the user design from where the data is being received.

Chapter 4: Designing with the Core

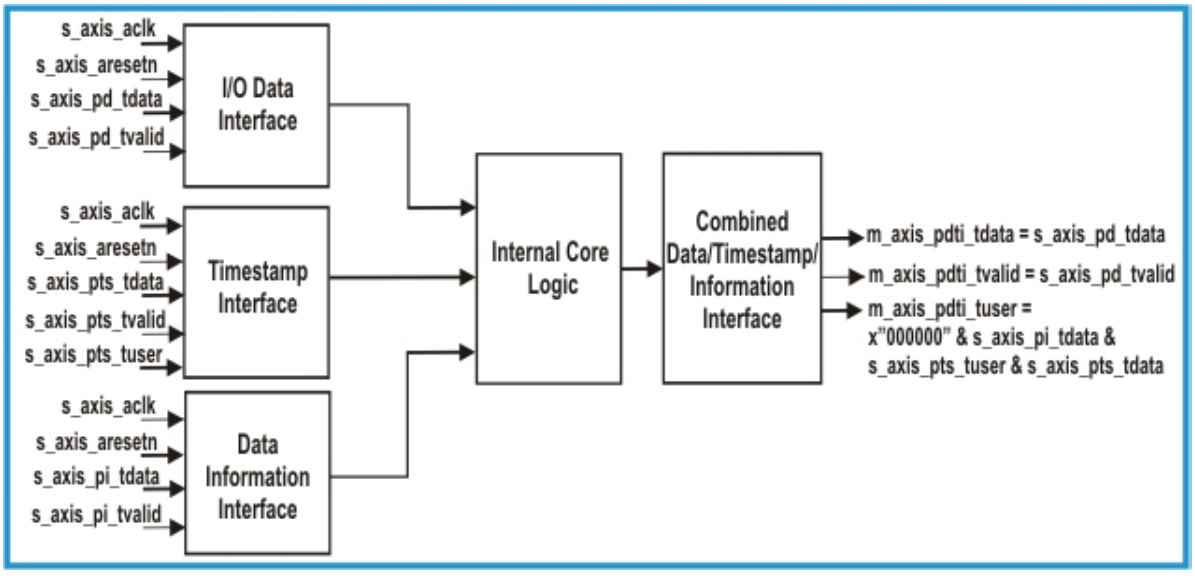
This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream Merge Core.

4.1 General Design Guidelines

The AXI4-Stream Merge Core provides the required logic to generate an AXI4-Stream output by concatenating the incoming AXI4-Streams. This IP core has AXI4-Stream user interfaces. The user can customize the core by setting the generic parameters based on the application requirement as described in Section 2.5.

Figure 4-1 is the block diagram of the AXI4-Stream Merge Core with the input and output signals shown. This diagram illustrates the output signals generated by the AXI4-Stream Merge core, by concatenating the input signals. For more details about the input and output signals, refer to Section 3.1.

Figure 4-1: AXI4-Stream Merge Core Block Diagram with I/O Signals



4.2 Clocking

AXI4-Stream Clock: **s_axis_aclk**

This clock is used to clock all the ports in the AXI4-Stream Merge Core.

4.3 Resets

Main reset: **s_axis_aresetn**

This is an active low reset synchronous with **s_axis_aclk**.

4.4 Interrupts

This section is not applicable to this IP core.

4.5 Interface Operation

I/O Data (PD) Interface: This is an AXI4-Stream Slave Interface used to receive data streams and is associated with **s_axis_aclk**. For more details about this interface, refer to Section 3.1.1.

Timestamp (PTS) Interface: This is an AXI4-Stream Slave Interface used to receive time-stamp and timing event data and is associated with **s_axis_aclk**. For more details about this inter-face, refer to Section 3.1.2.

Data Information (PI) Interface: This is an AXI4-Stream Slave Interface used to receive information about the incoming data across the I/O data interface and is associated with **s_axis_aclk**. For more details about this interface, refer to Section 3.1.3.

Combined Sample Data/ Timestamp/ Information (PDTI) Interface: AXI4-Stream Merge Core implements this AXI4-Stream Master interface across the output to transfer data streams and is associated with **s_axis_aclk**. For more details about this interface, refer to Section 3.1.4.

4.6 Programming Sequence

This section is not applicable to this IP core.

4.7 Timing Diagrams

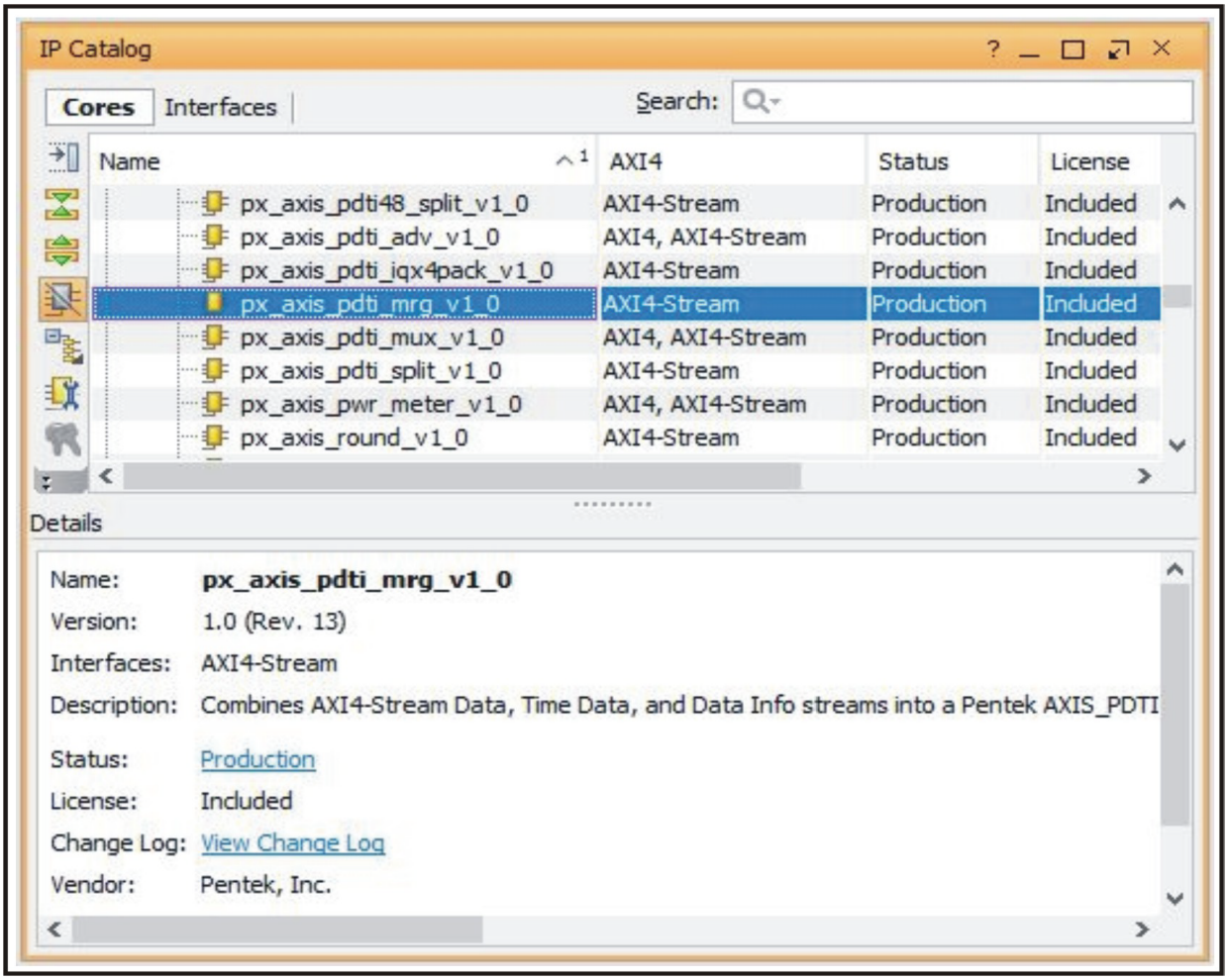
This section is not applicable to this IP core.

Chapter 5: Design Flow Steps

5.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream Merge Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_pdti_mrg_v1_0** as shown in Figure 5-1.

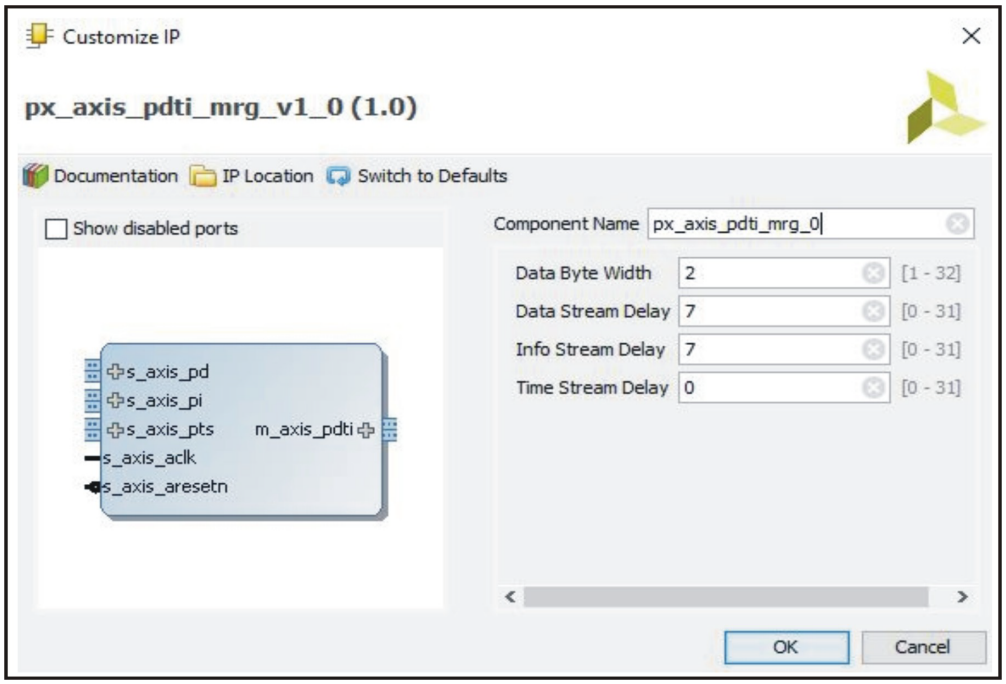
Figure 5-1: AXI4-Stream Merge Core in Pentek IP Catalog



5.1 Pentek IP Catalog (continued)

When you select the **px_axis_pdti_mrg_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 5-2). The core's symbol is the box on the left side.

Figure 5-2: AXI4-Stream Merge Core IP Symbol



5.2 User Parameters

The user parameters of this IP core are described in Section 2.5 of this user manual.

5.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP*.

5.4 Constraining the Core

This section contains information about constraining the AXI4-Stream Merge Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream Merge Core. Clock constraints can be applied in the top-level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The AXI4-Stream clock (**s_axis_aclk**) is based on the clock frequency of the input data streams from the user logic.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

5.5 Simulation

This section is not applicable to this IP core.

5.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.

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