

IP CORE MANUAL



AXI4-Stream IQ Data Format IP

px_axis_iq_fmtr_1

PENTEK

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IP Facts

Description

Pentek's Navigator AXI4-Stream IQ Data Format Core is designed to generate inverted spectrum/ off-set spectrum output data from 24-bit input data streams based on the user requirement.

This core complies with the ARM® AMBA® AXI4 Specification. This product specification defines the hardware interface, software interface, and parameterization options for the AXI4-Stream IQ Data Format Core.

Features

- Software programmable output data format
- Register access through AXI4-Lite Interface
- Supports 24-bit input data streams with single-sample-per-clock-cycle
- Supports generation of packed/ unpacked output data streams
- Performs symmetric rounding operation on the input data stream depending upon the user requirement

Table 1-1: IP Facts Table	
Core Specifics	
Supported Design Family ^a	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite and AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	N/A
Constraints File	Not Provided ^b
Simulation Model	N/A
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the [Vivado Design Suite Release Notes](#).

b.Clock constraints can be applied at the top level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

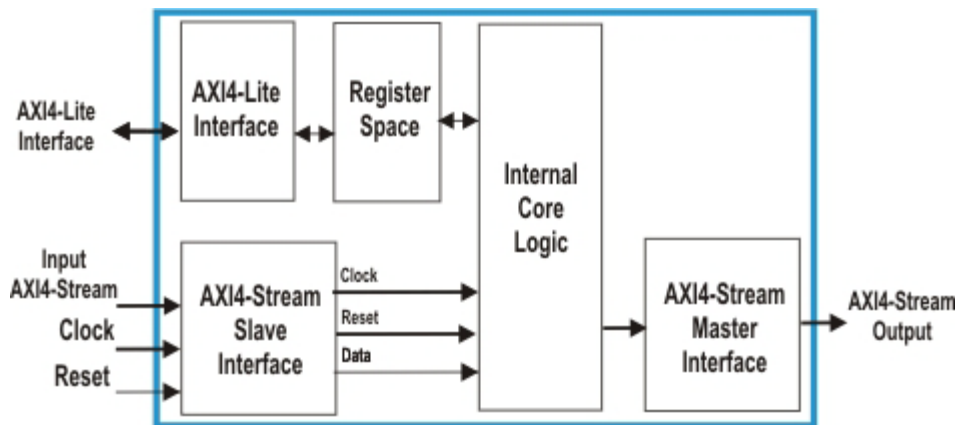
The AXI4-Stream IQ Data Format Core generates output data which is the inverted spectrum or offset spectrum of the input data stream in the data format defined by the user through the generic parameter `out_type` (See Section 2.5). This core supports two output data formats which are Output Type-0 and Output Type-1.

- **Type-0:** 32-bit output data bus which delivers either 16-bit packed I/Q data or unpacked 24-bit consecutive I/Q data streams.
- **Type-1:** 48-bit output data bus which delivers 24-bit packed I/Q data streams.

The user can define the output data to be packed/unpacked, and the desired output spectrum, through the control register within the Register Space of this core. This core performs rounding of the inverted or offset spectrum when the output type is set to Type 0 format. In Output Type 0 format, the 24-bit values must be rounded to 16-bits for packed data output.

Figure 1-1 is a top-level block diagram of the Pentek AXI4-Stream IQ Data Format Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: AXI4-Stream IQ Data Format Core Block Diagram



1.1 Functional Description (continued)

- ❑ **AXI4-Stream Interface:** The AXI4-Stream IQ Data Format Core has three AXI4-Stream Interfaces. At the input, two AXI4-Stream Slave Interfaces are used to receive AXI4-Streams and at the output an AXI4-Stream Master Interface is used to transfer AXI4-Streams through the output ports. For more details about the AXI4-Stream Interfaces refer to [Section 3.2 AXI4-Stream Core Interfaces](#).
- ❑ **AXI4-Lite Interface:** This core implements a 32-bit AXI4-Lite Slave Interface to access the Register Space. For more details about the AXI4-Lite Interface, refer to [Section 3.1 AXI4-Lite Core Interfaces](#).
- ❑ **Register Space:** This module contains the control register of the core. This register is accessed through the AXI4-Lite Interface.

1.2 Applications

The AXI4-Stream IQ Data Format Core can be incorporated into any Kintex Ultrascale FPGA to generate inverted or offset spectrum of the input data stream in the required format.

1.3 System Requirements

For a list of system requirements, see the [Vivado Design Suite Release Notes](#).

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

- 1) *Vivado Design Suite User Guide: Designing with IP*
- 2) *Vivado Design Suite User Guide: Programming and Debugging*
- 3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
<http://www.arm.com/products/system-ip/amba-specifications.php>

Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Stream IQ Data Format Core has bus interfaces that comply with the [ARM AMBA AXI4-Lite Protocol Specification](#) and the [AMBA AXI4-Stream Protocol Specification](#).

2.2 Performance

The performance of the AXI4-Stream IQ Data Format Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The AXI4-Stream IQ Data Format Core has two incoming clock signals. The AXI4-Stream clock and the AXI4-Lite interface CSR clock both have maximum frequencies of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express (PCIe®) AXI bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Stream IQ Data Format Core is shown in [Table 2-1](#). Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Resource	# Used
LUTs	607
Flip-Flops	2090
Memory LUTs	42

NOTE: Actual utilization may vary based on the user design in which the AXI4-Stream IQ Data Format Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Stream IQ Data Format Core are described in [Table 2-2](#). These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters		
Port/Signal Name	Type	Description
out_type	Integer	Output Data Type: This parameter indicates the output data type of the core. 0 => Output Type 0 - 32-bit bus with 16-bit packed I/Q data or 24-bit unpacked I/Q data in consecutive 32-bit words 1 => Output Type 1 - 48-bit bus with 24-bit packed I/Q data

Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- [AXI4-Lite Core Interfaces](#)
- [AXI4-Stream Core Interfaces](#)

3.1 AXI4-Lite Core Interfaces

The AXI4-Stream IQ Data Format Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4-Lite Slave Interface that can be used to access the control and status registers in the AXI4-Stream IQ Data Format Core. [Table 3-1](#) defines the ports in the CSR interface. See [Chapter 4](#) for a Control/Status Register memory map and bit definitions. See the [AMBA AXI4-Lite Specification](#) for more details on operation of the AXI4-Lite interfaces.

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	Clock
s_axi_csr_aresetn	Input	1	Reset: Active low. This signal will reset the control register to it's initial state.
s_axi_csr_awaddr	Input	7	Write Address: Address used for write operations. It must be valid when s_axi_csr_awvalid is asserted and must be held until s_axi_csr_awready is asserted by the AXI4-Stream IQ Data Format Core.
s_axi_csr_awprot	Input	3	Protection: The AXI4-Stream IQ Data Format Core ignores these bits.
s_axi_csr_awvalid	Input	1	Write Address Valid: This input must be asserted to indicate that a valid write address is available on s_axi_csr_awaddr . The AXI4-Stream IQ Data Format Core asserts s_axi_csr_awready when it is ready to accept the address. The s_axi_csr_awvalid must remain asserted until the rising clock edge after the assertion of s_axi_csr_awready .

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	Direction	Width	Description
s_axi_csr_awready	Output	1	Write Address Ready: This output is asserted by the AXI4-Stream IQ Data Format Core when it is ready to accept the write address. The address is latched when s_axi_csr_awvalid and s_axi_csr_awready are high on the same cycle.
s_axi_csr_wdata	Input	32	Write Data: This data will be written to the address specified by s_axi_csr_awaddr when s_axi_csr_wvalid and s_axi_csr_wready are both asserted. The value must be valid when s_axi_csr_wvalid is asserted and held until s_axi_csr_wready is also asserted.
s_axi_csr_wstrb	Input	4	Write Strobes: This signal, when asserted, indicates the number of bytes of valid data on the s_axi_csr_wdata signal. Each of these bits, when asserted, indicate that the corresponding byte of s_axi_csr_wdata contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	Write Valid: This signal must be asserted to indicate that the write data is valid for a write operation. The value on s_axi_csr_wdata is written into the register at address s_axi_csr_awaddr when s_axi_csr_wready and s_axi_csr_wvalid are high on the same cycle.
s_axi_csr_wready	Output	1	Write Ready: This signal is asserted by the AXI4-Stream IQ Data Format Core when it is ready to accept data. The value on s_axi_csr_wdata is written into the register at address s_axi_csr_awaddr when s_axi_csr_wready and s_axi_csr_wvalid are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	Write Response: The AXI4-Stream IQ Data Format Core indicates success or failure of a write transaction through this signal, which is valid when s_axi_csr_bvalid is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the AMBA AXI Specification .
s_axi_csr_bready	Input	1	Write Response Ready: This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	Write Response Valid: This signal is asserted by the AXI4-Stream IQ Data Format Core when the write operation is complete and the Write Response is valid. It is held until s_axi_csr_bready is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	Read Address: Address used for read operations. It must be valid when s_axi_csr_arvalid is asserted and must be held until s_axi_csr_arready is asserted by the AXI4-Stream IQ Data Format Core.
s_axi_csr_arprot	Input	3	Protection: These bits are ignored by the AXI4-Stream IQ Data Format Core.
s_axi_csr_arvalid	Input	1	Read Address Valid: This input must be asserted to indicate that a valid read address is available on s_axi_csr_araddr . The core asserts s_axi_csr_arready when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of s_axi_csr_arready .
s_axi_csr_arready	Output	1	Read Address Ready: This output is asserted by the AXI4-Stream IQ Data Format Core when it is ready to accept the read address. The address is latched when s_axi_csr_arvalid and s_axi_csr_arready are high on the same cycle.
s_axi_csr_rdata	Output	32	Read Data: This value is the data read from the address specified by the s_axi_csr_araddr when s_axi_csr_arvalid and s_axi_csr_arready are high on the same cycle.
s_axi_csr_rresp	Output	2	Read Response: The AXI4-Stream IQ Data Format Core indicates success or failure of a read transaction through this signal, which is valid when s_axi_csr_rvalid is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the AMBA AXI Specification .
s_axi_csr_rvalid	Output	1	Read Data Valid: This signal is asserted by the AXI4-Stream IQ Data Format Core when the read is complete and the read data is available on s_axi_csr_rdata . It is held until s_axi_csr_rready is asserted by the user logic.
s_axi_csr_rready	Input	1	Read Data Ready: This signal is asserted by the user logic when it is ready to accept the Read Data.

3.2 AXI4-Stream Core Interfaces

The AXI4-Stream IQ Data Format Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams.

- Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interface

3.2.1 Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interface

The AXI4-Stream IQ Data Format Core implements two of these AXI4-Stream interfaces across the input and output to receive and transfer AXI4-Streams. Pentek's Jade series board products have AXI4-Streams that follow a combined Sample data/ Timestamp/ Information Stream format. This type of data stream combines sample data with its time aligned timestamp and data information. The input data streams are required to be 24-bit data streams with single-sample-per -clock-cycle. The output data streams of the core are transferred through the output AXI4-Stream Master Interface.

[Table 3-2](#), defines the ports in the AXI4-Stream Slave and Master Sample Data/ Timestamp/ Information Stream Interfaces. See the [AMBA AXI4-Stream Specification](#) for more details on the operation of the AXI4-Stream Interface.

Table 3-2: Combined Sample Data/ Timestamp/ Information Streams Interface Port Descriptions			
Port	Direction	Width	Description
AXI4-Stream Slave Interface			
aclk	Input	1	AXI4-Stream Clock
aresetn	Input	1	Reset: Active Low.
s_axis_pdti_tdata	Input	48	Input Data: This is the input data stream.
s_axis_pdti_tvalid	Input	1	Input Data Valid: Asserted when data is valid on s_axis_pdti_tdata .

Table 3-2: Combined Sample Data/ Timestamp/ Information Streams Interface Port Descriptions (Continued)			
Port	Direction	Width	Description
AXI4-Stream Slave Interface (continued)			
s_axis_pdti_tuser	Input	128	<p>Sideband Information: This is the user defined sideband information received alongside the data stream.</p> <p>tuser [63:0] - Timestamp[63:0] tuser [71:64] - Gate Positions tuser [79:72] - Sync Positions tuser [87:80] - PPS Positions tuser [91:88] - Samples per clock cycle tuser [92] - I/Q data of the sample 0 = I; 1 = Q tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit 2 = 24-bit; 3 = 32-bit tuser [95] - Data Type => 0 = Real; 1 = I/Q tuser [103:96] - channel [7:0] tuser [127:104] - Reserved Note: The bits [103:96] define the channel number in the user design from where the data is being received.</p>
AXI4-Stream Master Interface			
m_axis_pdti_tdata	Output	[31 + (out_type *16)] +1	Output Data: This is the output data stream.
m_axis_pdti_tvalid	Output	1	Output Data Valid: Asserted when data is valid on m_axis_pdti_tdata .
m_axis_pdti_tuser	Output	128	<p>Sideband Information: This is the user defined sideband information received alongside the data stream.</p> <p>tuser [63:0] - Timestamp[63:0] tuser [71:64] - Gate Positions tuser [79:72] - Sync Positions tuser [87:80] - PPS Positions tuser [91:88] - Samples per clock cycle tuser [92] - I/Q data of the sample 0 = I; 1 = Q tuser [94:93] - Data Format => 0 = 8-bit; 1 = 16-bit 2 = 24-bit; 3 = 32-bit tuser [95] - Data Type => 0 = Real; 1 = I/Q tuser [103:96] - channel [7:0] tuser [127:104] - Reserved Note: The bits [103:96] define the channel number in the user design from where the data is being received.</p>

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Chapter 4: Register Space

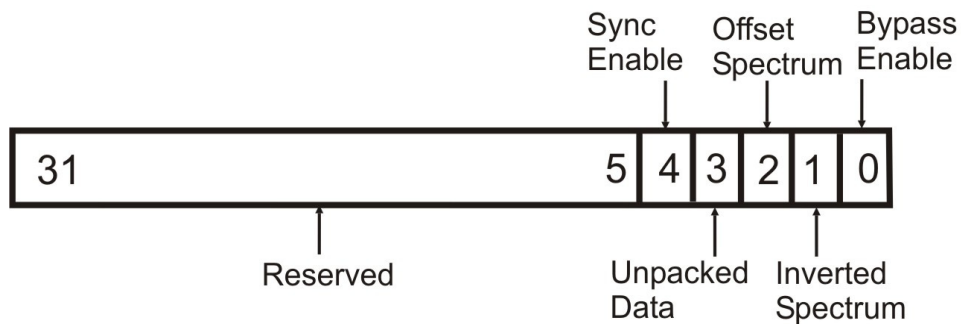
This chapter provides the memory map and register descriptions for the register space of the AXI4-Stream IQ Data Format Core. The memory map is provided in [Table 4-1](#).

Table 4-1: Register Space Memory Map			
Register Name	Address (Base Address +)	Access	Description
Control Register	0x00	R/W	Controls the type of output spectrum, sync enable, unpacked data enable, and bypass enable operations of the core.

4.1 Control Register

This register controls the type of output spectrum of the core, which can be an inverted spectrum or an offset spectrum. It also controls the bypass enable, which can enable bypass of the data from the input to the output without undergoing any change. It can also enable/ disable the generation of unpacked output data stream. This register also controls the sync enable signal, which is used to reset the core based on the sync signal in the input sideband user data, when the core is set to generate an offset spectrum output. The Control Register is illustrated in [Figure 4-1](#) and described in [Table 4-2](#).

Figure 4-1: Control Register



4.1 Control Register (continued)

Table 4-2: Control Register (Base Address + 0x00)				
Bits	Field Name	Default Value	Access Type	Description
31:5	Reserved	N/A	N/A	Reserved
4	sync_en	0	R/W	Sync Enable: This bit enables/ disables the sync signal in the sideband user data to reset the core, when the output of the core is set to offset spectrum. 0 = Disable 1 = Enable
3	unpacked			Unpacked Data: This bit enables/ disables the generation of unpacked output data. 0 = Disable 1 = Enable Note: This bit is valid only when the Output data format is set to Type 0.
2	offset			Offset Spectrum: This bit enables/ disables the generation of offset spectrum output from the input data stream. 0 = Disable 1 = Enable
1	invert			Inverted Spectrum: This bit enables/ disables the generation of inverted spectrum from the input data stream. 0 = Disable 1 = Enable
0	bypass_n			Bypass Enable: This bit enables/ disables the bypass of the input data stream to the output ports without any change. 0 = Enable bypass 1 = Disable bypass

Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Stream IQ Data Format Core.

5.1 General Design Guidelines

The AXI4-Stream IQ Data Format Core provides the required logic to generate the desired output data format based on the user-defined parameters.

5.2 Clocking

AXI4-Stream Clock: **aclk**

This clock is used to clock all ports in the AXI4-Stream IQ Data Format Core.

CSR Clock: **s_axi_csr_aclk**

This clock is used to clock the AXI4-Lite interface of the core.

5.3 Resets

Main reset: **aresetn**

This is an active low reset synchronous with **aclk**.

CSR Reset: **s_axi_csr_aresetn**

This is an active low reset synchronous with **s_axi_csr_clk**.

5.4 Interrupts

This section is not applicable to this IP core.

5.5 Interface Operation

CSR Interface: This is the Control/Status Register Interface. It is associated with `s_axi_csr_aclk`. It is a standard AXI4-Lite Slave interface.

Combined Sample Data/ Timestamp/ Information Streams (PDTI) Interfaces: This core implements two AXI4-Stream interfaces at the input and output to receive/ transfer data streams, and are associated with `aclk`. For more details about these interfaces refer to [Section 3.2.1](#).

5.6 Programming Sequence

This section briefly describes the programming sequence for the AXI4-Stream IQ Data Format Core.

- 1) Assign desired values to the generic parameter.
- 2) Set the control register with the required values based on the desired mode of operation of the core.
- 3) Observe the outputs across the outputs ports when valid data is available at the input ports.

5.7 Timing Diagrams

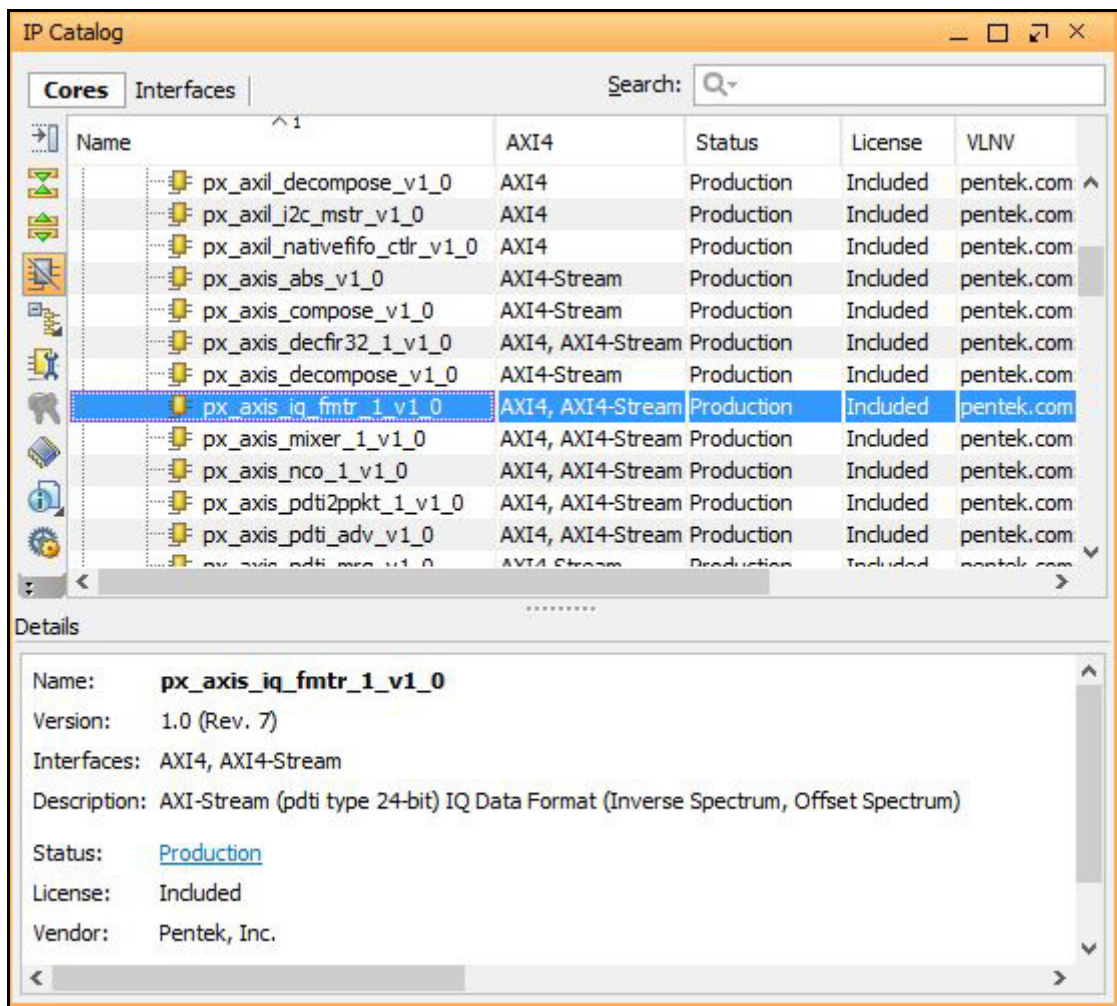
This section is not applicable to this IP core.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Stream IQ Data Format Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axis_iq_fmtr_1_v1_0** as shown in [Figure 6-1](#).

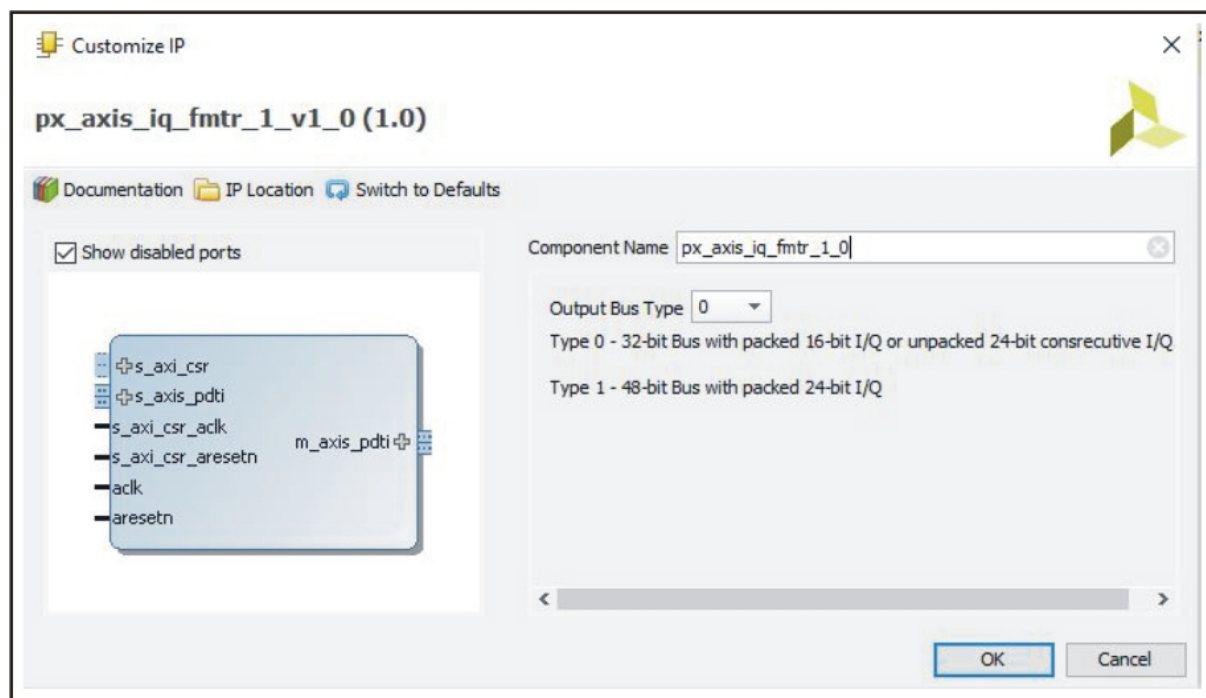
Figure 6-1: AXI4-Stream IQ Data Format Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the `px_axis_iq_fmtr_1_v1_0` core, a screen appears that shows the core's symbol and the core's parameters (see [Figure 6-2](#)). The core's symbol is the box on the left side.

Figure 6-2: AXI4-Stream IQ Data Format Core IP Symbol



6.2 User Parameters

The user parameter of this core is described in [Section 2.5](#) of this Product Guide.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the [Vivado Design Suite User Guide - Designing with IP](#).

6.4 Constraining the Core

This section contains information about constraining the AXI4-Stream IQ Data Format Core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with the AXI4-Stream IQ Data Format Core. Clock constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The CSR clock (`s_axi_csr_aclk`) and the AXI4-Stream clock (`aclk`) have the same maximum operating frequency of 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

This section is not applicable to this IP core.

6.6 Synthesis and Implementation

For details about synthesis and implementation see the [Vivado Design Suite User Guide - Designing with IP](#).

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