IP CORE MANUAL

AXI4-Lite to DDR4 SDRAM Bridge IP

px_axil2ddr_rq

PENTEK

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IP Facts

Description

Pentek's Navigator™ AXI4-Lite to DDR4 SDRAM Bridge Core acts as a bridge between an AXI4-Lite Interface in the user design and the Xilinx® DDR4 Memory Controller IP Core, when connected through a Pentek AXI4-Stream to DDR4 Memory Controller Interface Core. This core converts DDR4 SDRAM read/ write requests received across the AXI4-lite Interface into AXI request data streams.

This core complies with the ARM® AMBA® AXI4 Specification. This user manual defines the hardware interface, software interface, and parameterization options for the AXI4-Lite to DDR4 SDRAM Bridge Core.

Features

- Software programmable Requester ID
- Auto increments the DDR4 SDRAM address for contiguous read/ write requests
- Supports generation of interrupt output

Table 1-1: IP Facts Table

Core Specifics	
Supported Design Family[a]	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite and AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided[b]
Simulation Model	VHDL
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a.For a complete list of supported devices, see the *Vivado Design Suite Release Notes*.
b.Clock constraints can be applied at the top-level module of the user design.

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Chapter 1: Overview

1.1 Functional Description

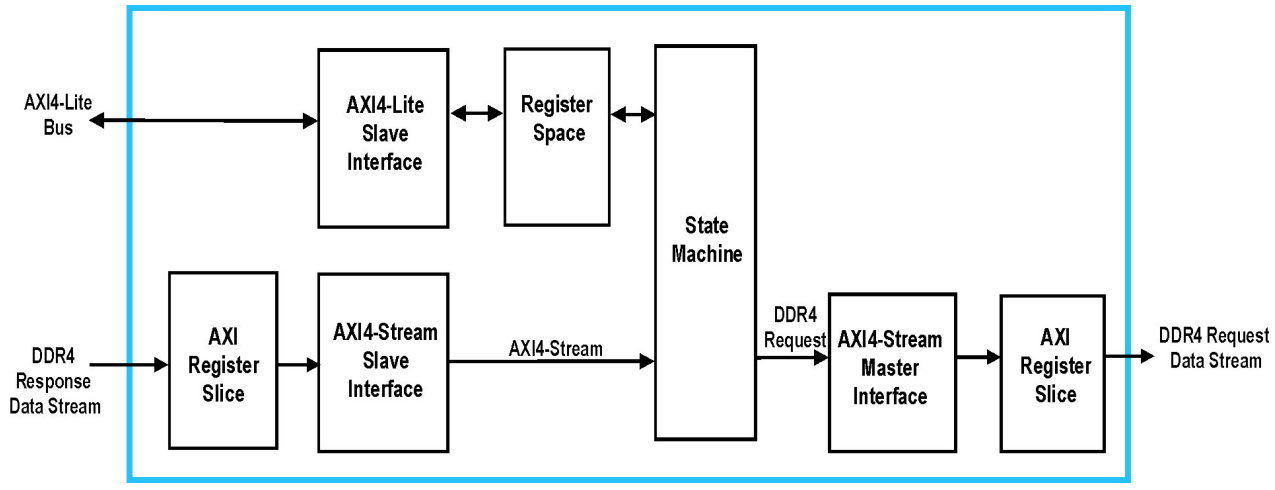
The AXI4-Lite to DDR4 SDRAM Bridge Core provides a transaction interface to the DDR4 Memory Controller. This core accepts DDR4 memory read/ write requests from an AXI4-Lite Interface and converts them into read/ write request data streams compatible with the Xilinx DDR4 Memory Controller IP Core when connected to it through a Pentek AXI4-Stream to DDR4 Memory Controller Interface Core.

A unique requester ID identifying the data streams can be defined by the user through the generic parameter **id** (see Section 2.5). The generic parameters also allow the user to enable or disable the generation an interrupt output. This core includes a **State Machine** to control the generation of memory request data streams from the requests received across the AXI4-Lite Interface.

The AXI4-Lite to DDR4 SDRAM Bridge Core also includes two Xilinx **AXI Register Slices** at the **DDR4 Request** and **DDR4 Response** AXI4-Stream Interfaces to break critical timing paths and achieve higher clock frequency. This core also supports auto increment of the DDR4 memory address, after being set once, for contiguous read/ write requests.

Figure 1-1 is a top-level block diagram of the AXI4-Lite to DDR4 SDRAM Bridge Core. The modules within the block diagram are explained in other sections of this manual.

Figure 1-1: AXI4-Lite to DDR4 SDRAM Bridge Core Block Diagram



1.1 Functional Description (continued)

- **AXI4-Lite Interface:** This module implements a 32-bit AXI4-Lite Slave Interface to receive the memory read/write requests and also access the register space. For more details about the AXI4-Lite Interface, refer to Section 3.1 AXI4-Lite Core Interfaces.

- **AXI4-Stream Interfaces:** The AXI4-Lite to DDR4 SDRAM Bridge Core has AXI4-Stream Interfaces to transfer requests and receive responses to/from the DDR4 SDRAM Memory Controller IP Core. For more details about the AXI4-Stream Interfaces, refer to **Section 3.2 AXI4-Stream Core Interfaces**.

- **Register Space:** This module contains registers to store DDR4 SDRAM request address and other information. Registers are accessed through the AXI4-Lite interface.

- **Register Slices:** The AXI Register Slice Core is included in the Xilinx AXI Interconnect Core and is used to connect one AXI memory-mapped master to one AXI memory-mapped slave through a set of pipeline registers, typically to break a critical timing path. The AXI4-Lite to DDR4 SDRAM Bridge Core includes two Register Slices at the AXI4-Stream Slave and Master Interfaces.

- **State Machine:** This state machine is used to control the generation of the Memory read/write request data streams.

1.2 Applications

This core can be incorporated into any Kintex Ultrascale FPGAto serve as a bridge between an AXI4-Lite Interface in the user design and the Xilinx DDR4 Memory Controller IP Core.

1.3 System Requirements

For a list of system requirements, see the Vivado Design Suite Release Notes.

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

1) *Vivado Design Suite User Guide: Designing with IP*

2) *Vivado Design Suite User Guide: Programming and Debugging*

3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
http://www.arm.com/products/system-ip/amba-specifications.php

4) DDR4 SDRAM Memory Controller Documentation

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Chapter 2: General Product Specifications

2.1 Standards

The AXI4-Lite to DDR4 SDRAM Bridge Core has bus interfaces that comply with the *AMBA AXI4-Lite Protocol Specification* and the *AMBA AXI4-Stream Protocol Specification*.

2.2 Performance

The performance of the AXI4-Lite to DDR4 SDRAM Bridge Core is limited only by the FPGA logic speed. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

This core is designed to meet a target frequency of 250 MHz on a Kintex Ultrascale -2 speed grade FPGA. 250 MHz is typically the PCI Express® (PCIe®) AXI Bus clock frequency.

2.3 Resource Utilization

The resource utilization of the AXI4-Lite to DDR4 SDRAM Bridge Core is shown in Table 2-1. Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Table 2-1: Resource Usage and Availability

Resource	# Used
LUTs	264
Flip-Flops	362

NOTE: Actual utilization may vary based on the user design in which the AXI4-Lite to DDR4 SDRAM Bridge Core is incorporated.

2.4 Limitations and Unsupported Features

This section is not applicable to this IP core.

2.5 Generic Parameters

The generic parameters of the AXI4-Lite to DDR4 SDRAM Bridge Core are described in Table 2-2. These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters

Port/Signal Name	Type	Description
id	Integer	**Requester ID:** The user can define a unique ID to identify the data streams through this generic parameter. It can range from 0 - 255.
has_irq	Boolean	**Has Interrupt Output:** This parameter is used to enable/ disable the generation of an interrupt output after the generation of a read/ write request data stream.

Chapter 3: Port Descriptions

This chapter provides port descriptions for the following interface types:

- AXI4-Lite Core Interfaces
- AXI4-Stream Core Interfaces

3.1 AXI4-Lite Core Interfaces

The AXI4-Lite to DDR4 SDRAM Bridge Core has the following AXI4-Lite interface which is used to receive memory read/ write requests from the user design. .

3.1.1 AXI4-Lite Slave Interface

Table 3-1 defines the ports in the AXI4-Lite Slave Interface. See the *AMBA AXI4-Lite Specification* for more details on the AXI4-Lite interface.

Table 3-1: AXI4-Lite Slave Interface Port Descriptions

Port	Direction	Width	Description
s_axi_aclk	Input	1	**Clock**
s_axi_aresetn	Input	1	**Reset:** Active low. This will reset the state machine within the core.
s_axi_awaddr	Input	4	**Write Address:** Address used for write operations. It must be valid when **s_axi_awvalid** is asserted and must be held until **s_axi_awready** is asserted by the Bridge Core.
s_axi_awprot	Input	3	**Protection:** The Bridge Core ignores these bits.
s_axi_awvalid	Input	1	**Write Address Valid:** This input must be asserted to indicate that a valid write address is available on **s_axi_awaddr**. The Bridge Core asserts **s_axi_awready** when it is ready to accept the address. The **s_axi_awvalid** must remain asserted until the rising clock edge after the assertion of **s_axi_awready**.
s_axi_awready	Output	1	**Write Address Ready:** This output is asserted by the Bridge Core when it is ready to accept the write address.The address is latched when **s_axi_awvalid** and **s_axi _awready** are high on the same cycle.
s_axi_wdata	Input	32	**Write Data:** This data will be written to the address specified by **s_axi_awaddr** when **s_axi_wvalid** and **s_axi_wready** are both asserted. The value must be valid when **s_axi_wvalid** is asserted and held until **s_axi_wready** is also asserted.

Table 3-1: AXI4-Lite Slave Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_wstrb	Input	4	**Write Strobes:** This signal when asserted indicates the number of bytes of valid data on **s_axi_wdata** signal. Each of these bits, when asserted, indicate that the corresponding byte of **s_axi_wdata** contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_wvalid	Input	1	**Write Valid:** This signal must be asserted to indicate that the write data is valid for a write operation. The value on **s_axi_ wdata** is written into the register at address **s_axi_awaddr** when **s_axi_wready** and **s_axi_wvalid** are High on the same cycle.
s_axi_wready	Output	1	**Write Ready:** This signal is asserted by the Bridge Core when it is ready to accept data. The value on **s_axi_ wdata** is written into the register at address **s_axi_awaddr** when **s_axi_wready** and **s_axi_wvalid** are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_bresp	Output	2	**Write Response:** The Bridge Core indicates success or failure of a write transaction through this signal, which is valid when **s_axi_csr_bvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave error 11 = Decode error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_bvalid	Output	1	**Write Response Valid:** This signal is asserted by the core when the write operation is complete and the Write Response is valid. It is held until **s_axi_bready** is asserted by the user logic.
s_axi_bready	Input	1	**Write Response Ready:** This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_araddr	Input	4	**Read Address:** Address used for read operations. It must be valid when **s_axi_arvalid** is asserted and must be held until **s_axi_arready** is asserted by the Bridge Core.
s_axi_arprot	Input	3	**Protection:** These bits are ignored by the Bridge Core.
s_axi_arvalid	Input	1	**Read Address Valid:** This input must be asserted to indicate that a valid read address is available on the **s_axi_araddr**. The Bridge Core asserts **s_axi_arready** when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of **s_axi_arready**.
s_axi_arready	Output	1	**Read Address Ready:** This output is asserted by the AXI4-Lite to DDR4 SDRAM Bridge Core when it is ready to accept the read address. The address is latched when **s_axi_arvalid** and **s_axi_arready** are high on the same cycle.
s_axi_rdata	Output	32	**Read Data:** This value is the data read from the address specified by the **s_axi_araddr** when **s_axi_arvalid** and **s_axi_ arready** are high on the same cycle.

Table 3-1: AXI4-Lite Slave Interface Port Descriptions (Continued)

Port	Direction	Width	Description
s_axi_rresp	Output	2	**Read Response:** The AXI4-Lite to DDR4 SDRAM Bridge Core indicates success or failure of a read transaction through this signal, which is valid when **s_axi_rvalid** is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave error 11 = Decode error Note: For more details about this signal refer to the *AMBA AXI Specification*.
s_axi_rvalid	Output	1	**Read Data Valid:** This signal is asserted by the core when the read is complete and the read data is available on **s_axi_rdata**. It is held until **s_axi_rready** is asserted by the user logic.
s_axi_rready	Input	1	**Read Data Ready:** This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output	1	**Interrupt:** This is an active High edge type interrupt output. This output can be enabled by setting the generic parameter **has_irq** to True.

3.2 AXI4-Stream Core Interfaces

The AXI4-Lite to DDR4 SDRAM Bridge Core has the following AXI4-Stream Interfaces, used to receive and transfer data streams:

- DDR4 Request (RQST) Interface**:** This core has an DDR4 Memory Request AXI4-Stream Interface at the output of the core to transfer the generated memory read/ write requests.
- DDR4 Response (RSP) Interface**:** This core has an DDR4 Memory Response AXI4-Stream Interface at the input of the core to receive response data streams from the DDR4 Memory Controller core.

3.2.1 DDR4 Request (RQST) Interface

The AXI4-Lite to DDR4 SDRAM Bridge Core implements an DDR4 Request Interface across the output to transfer Memory read/ write Request data streams. This is an AXI4-Stream Master Interface. Table 3-2 defines the ports in the AXI4-Stream Master Request Interface. See the *AMBA AXI4-Stream Protocol Specification* for more details on the operation of the AXI4-Stream Interface.

Table 3-2: DDR4 Request Interface Port Descriptions

Port/Signal Name	Type	Direction	Description
m_axis_rqst_tdata	Output	512	**Request Data Bus:** This is the DDR4 Memory Request data generated by the core from the requests received across the AXI4-Lite Interface.
m_axis_rqst_tvalid		1	**Request Data Valid:** Asserted when data is valid on **m_axis_rqst_tdata**. The user application can pace the data transfer using the **m_axis_rqst _tready** signal.
m_axis_rqst_tuser		256	**Request User Data:** This is the sideband user information data which contains the DDR4 memory request packet header. **Table 3-5** includes the bit definitions of the bits **tuser[256:0].**
m_axis_rqst_tlast		1	**Request Data Last:** Since all request frames are single cycle in length, this **tlast** signal is asserted on every valid data cycle. It is provided mainly to allow arbitration in AXI Stream switches to use it to arbitrate on **tlast**.
m_axis_rqst_tid		8	**Request Data Stream Identifier:** This is the unique data stream identifier specified by the user using the generic parameter **`id`**.
m_axis_rqst_tready	Input	1	**Request Data Ready:** Activation of this signal by the user logic indicates that the user logic is ready to accept data. Data is transferred across the interface when both **m_axis_rqst _tvalid** and **m_axis_rqst_tready** are asserted in the same cycle. If the user application deasserts the ready signal when **m_axis_rqst_tvalid** is asserted, the core maintains the data on the bus and keeps the valid signal asserted until the user application has asserted the ready signal.

3.2 AXI4-Stream Core Interfaces (continued)

3.2.1 DDR4 Request (RQST) Interface (continued)

Table 3-3 shows the bit definitions of the DDR4 Request User Data (**m_axis_rqst_tuser**).

Table 3-3: DDR4 Request User Data Bit Definitions

Bit Index	Name	Width	Description
255:128	**DATA**	128	**RAM Data:** These bits carry the upper 128 bits of RAM data to be written to the address location in the DDR4 SDRAM.
127:118	**RES**	9	**Reserved**
119:40	**MSK**	80	**Byte Mask:** These bits indicate the byte masks of the data which indicate the data on the data bus to be masked.
39:36	**RES**	4	**Reserved**
35	**OP**	1	**Type of Request:** This bit indicates the type of Memory request. 0 = Write; 1 = Read
34:32	**ADDRE**	3	**Future Address Expansion:** These bits indicate the address expansion of the DDR4 SDRAM memory location.
31:0	**ADDR**	32	**DDR4 Memory Address:** This is the address location in the DDR4 SDRAM where the read/ write operation is to be performed. The address must be aligned to request size boundaries.

3.2 AXI4-Stream Core Interfaces (continued)

3.2.2 DDR4 Response (RSP) Interface

The AXI4-Lite to DDR4 SDRAM Bridge Core implements an DDR4 Response Interface across the input to receive response data streams. This is an AXI4-Stream Slave Interface. Table 3-4 defines the ports in the AXI4-Stream Slave DDR4 Response Interface. See the *AMBA AXI4-Stream Protocol Specification* for more details on the operation of the AXI4-Stream Interface. .

Table 3-4: DDR4 Response Interface Port Descriptions

Port	Direction	Width	Description
s_axis_rsp_tdata	Input	512	**Response Data Bus:** This is the Response data received from the user design for a DDR4 memory read Request.
s_axis_rsp_tvalid	Input	1	**Response Data Valid:** Asserted when data is valid on **s_axis_rsp_tdata**. This bus cannot be throttled and there is no **tready** output from the core. The core must be ready to accept data if it requested it.
s_axis_rsp_tuser	Input	256	**Request User Data:** This is the sideband user information data which contains the DDR4 response packet header and error indicators. **Table 3-5** defines the bit definitions of the bits **tuser[255:0].**
s_axis_rsp_tlast	Input	1	**Request Data Last:** Since all request frames are single cycle in length, this **tlast** signal is asserted on every valid data cycle. It is provided mainly to allow arbitration in AXI Stream switches to use it to arbitrate on **tlast**.
s_axis_rsp_tid	Input	8	**Response Data Stream Identifier:** This is the unique data stream identifier specified by the user in the request which indicates the request corresponding to the response.

3.2 AXI4-Stream Core Interfaces (continued)

3.2.2 DDR4 Response (RSP) Interface (continued)

Table 3-5 shows the bit definitions of the DDR4 Response User Data (**m_axis_rsp_tuser**).

Table 3-5: DDR4 Request User Data Bit Definitions

Bit Index	Name	Width	Description
255:128	**DATA**	128	**RAM Data:** These bits carry the upper 128 bits of RAM data being received from the address location in the DDR4 SDRAM.
127:118	**RES**	9	**Reserved**
119:40	**MSK**	80	**Byte Masks:** These bits indicate the byte masks of the data on the data bus to be masked.
39:35	**RES**	5	**Reserved**
34:32	**ADDRE**	3	**Future Address Expansion:** These bits indicate the address expansion of the DDR4 SDRAM memory location.
31:0	**ADDR**	32	**DDR4 Memory Address:** This is the address location in the DDR4 SDRAM where the read/ write operation is to be performed. The address must be aligned to request size boundaries.

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Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the AXI4-Lite to DDR4 SDRAM Bridge Core. The memory map is provided in Table 4-1.

Table 4-1: Register Space Memory Map

Register Name	Address (Base Address +)	Access	Description
DDR4 Address Register 1	0x00	R/W	Controls the DDR4 SDRAM request address.
DDR4 Address Register 2	0x04		Controls the DDR4 Address expansion bits, memory area, and byte enables.
DDR4 Data Access	0x08		Indicates DDR4 data access for read/write operations.

4.1 DDR4 Address Register 1

This register controls the least significant 32 bits of the DDR4 SDRAM address where data is to be written to or read from. This control register is illustrated in Figure 4-1 and described in Table 4-2.

Figure 4-1: DDR4 Address Register 1

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Table 4-2: DDR4 Address Register 1 (Base Address + 0x00)

Bits	Field Name	Default Value	Access Type	Description
31:0	ddr4_addr	0x00000000	R/W	**DDR4 Address[31:0]:** These bits hold the value of the DDR4 SDRAM read/ write request address bits [31:0].

4.2 DDR4 Address Register 2

This register controls the most significant 2 bits of the DDR4 address, the memory area, byte mask bits, and interrupt enable. This register is illustrated in Figure 4-2 and described in Table 4-3.

Figure 4-2: DDR4 Address Register 2

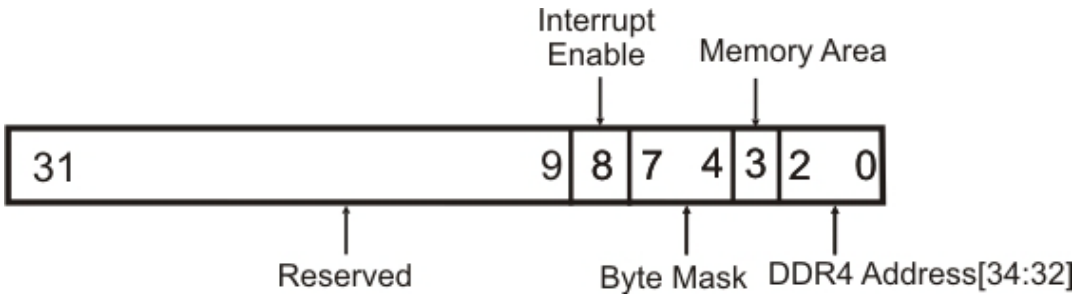

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Table 4-3: DDR4 Address Register 2 (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:9	reserved	N/A	N/A	**Reserved**
8	int_en	0	R/W	**Interrupt Enable:** This when set to '1' generates an interrupt after a read/ write request has been generated. An interrupt output is generated by the Bridge core when this interrupt enable bit is High, and the generic parameter **has_irq** is set to True.
7:4	byte_mask	0000	R/W	**Byte Mask Bits:** These bits are used to mask the bytes of data to be written to or read from the DDR4 SDRAM. Each bit corresponds to a byte in the 32-bit data of the AXI4-Lite bus. **byte_mask[0]** corresponds to least significant byte and **byte_mask[3]** corresponds to the most significant byte. 0 = Byte mask disabled 1 = Byte mask enabled.
3	mem_area	0	R/W	**Memory Area:** Data bus of the DDR4 memory is 640 bits wide. Since the maximum output data bus width of this core is 512 bits, **mem_area** is used to identify the data corresponding to the ranges of 0 to 512 bits and 513 to 639 bits. Based on this bit, the byte mask is defined within the user sideband data of the core. 0 - data in bits 0 to 512 1 - data in bits 513 to 639
2:0	ddr4_addr	000	R/W	**DDR4 Address[34:32]:** These bits hold the value of the DDR4 request address bits [34:32].

4.3 DDR4 Data Access Register

This register indicates the data read from the DDR4 SDRAM during a read operation at the address specified by the DDR4 Address Register 1. During a write oepration, this register controls the data to be written to the DDR4 SDRAM. The DDR4 address auto increments for contiguous read/ write requests. This register is illustrated in Figure 4-3 and described in Table 4-4.

Figure 4-3: DDR4 Data Access Register

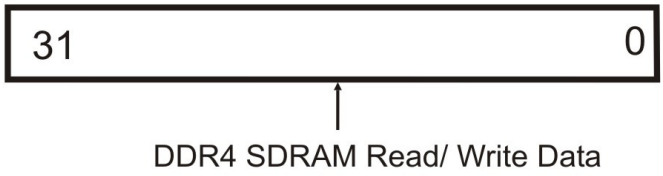

Table 4-4: DDR4 Data Access Register (Base Address + 0x08)

Bits	Field Name	Default Value	Access Type	Description
31:0	data	0x00000000	R/W	**DDR4 SDRAM Read/ Write Data**

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Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the AXI4-Lite to DDR4 SDRAM Bridge Core.

5.1 General Design Guidelines

The AXI4-Lite to DDR4 SDRAM Bridge Core is used to convert DDR4 requests from the user design across an AXI4-Lite interface into request data streams compatible with the Xilinx DDR4 SDRAM Memory Controller Core. This core must be connected to the DDR4 SDRAM Memory Controller Core through a Pentek AXI4-Stream to DDR4 SDRAM Memory Controller Interface Core. The core also provides an auto increment feature to increment the DDR4 address for contiguous requests.

5.2 Clocking

Main Clock: **s_axi_aclk**

This clock is used to clock all the ports on the core.

5.3 Resets

Reset: **s_axi_aresetn**

This is active low synchronous reset associated with the **s_axi_aclk**.

5.4 Interrupts

This section is not applicable to this IP core.

5.5 Interface Operation

AXI4-Lite Interface: This is an AXI4-Lite Slave Interface and is associated with **s_axi_aclk**. This interface receives the DDR4 read/ write requests from the user design.

DDR4 Request (RQST) Interface: This is an AXI4-Stream Master Interface used to transfer DDR4 request data streams and is associated with **s_axi_aclk**. For more details about this interface, refer to Section 3.2.1.

DDR4 Response (RSP) Interface: This is an AXI4-Stream Slave Interface used to receive DDR4 response data streams for the requests transferred by the core and is associated with **s_axi_aclk**. For more details about this interface, refer to Section 3.2.2.

5.6 Programming Sequence

This section briefly describes the programming sequence for the AXI4-Lite to DDR4 SDRAM Bridge Core.

1) Set the desired DDR4 address [31:0].

2) Set the desired DDR4 address [34:32], memory area, byte mask, and interrupt enable.

3) Write/ read data to/ from the DDR4 SDRAM.

5.7 Timing Diagrams

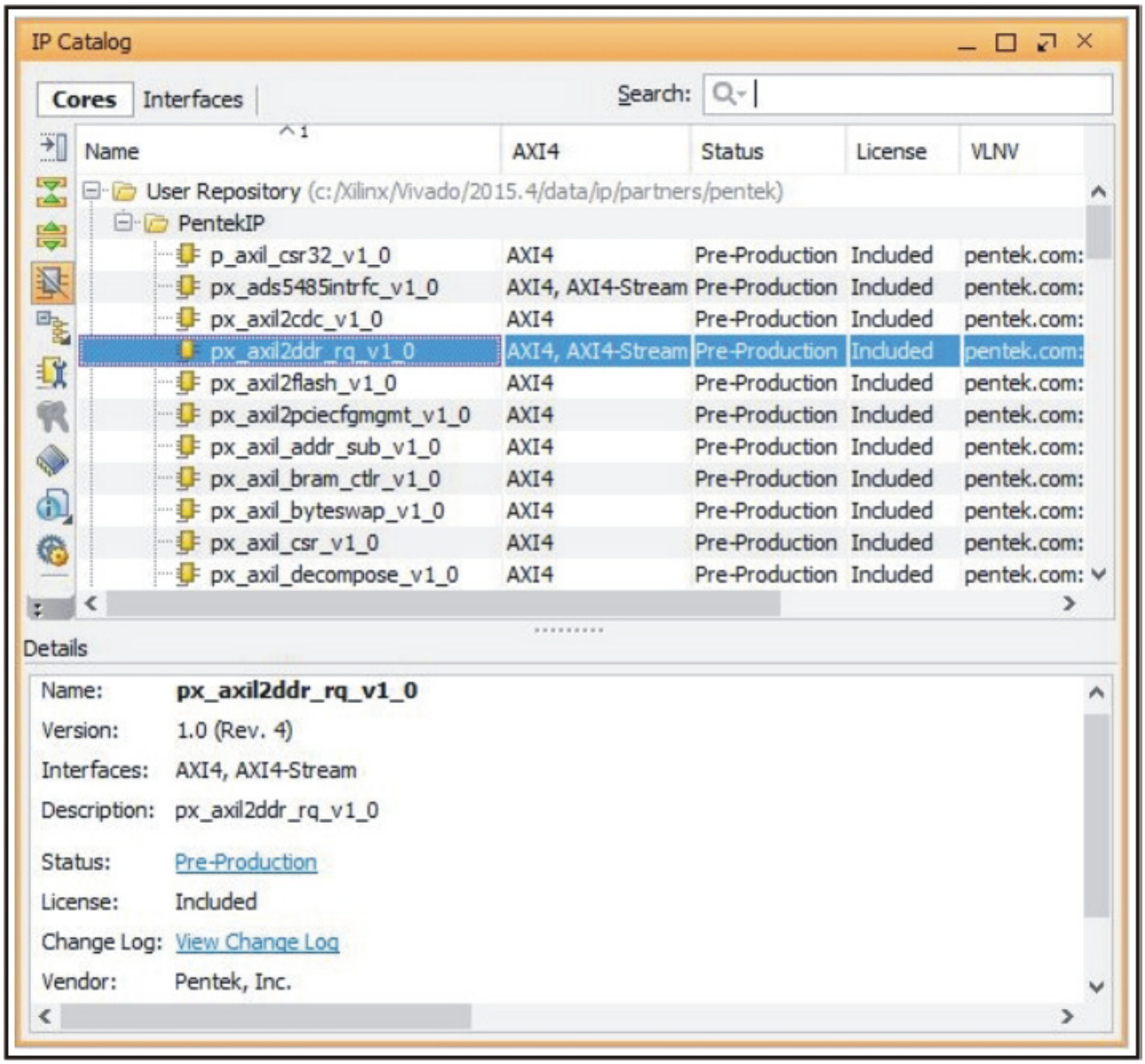
The timing diagram for the AXI4-Lite to DDR4 SDRAM Bridge Core, shown in Figure 6-3, is obtained by running the simulation of the test bench of the core in Vivado VSim environment. For more details about the test bench, refer to Section 6.5.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek AXI4-Lite to DDR4 SDRAM Bridge Core. It also includes simulation, synthesis, and implementation steps that are specific to this IP core. This core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_axil2ddr_rq_v1_0** as shown in Figure 6-1.

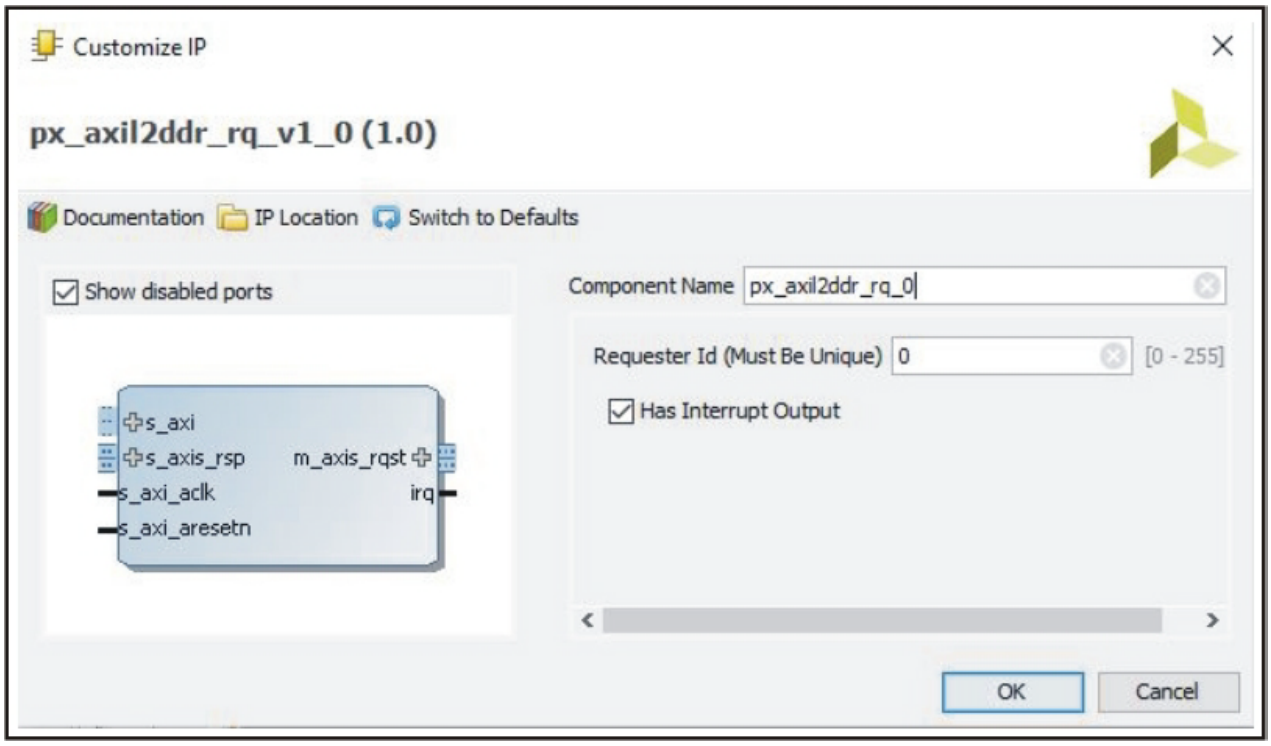
Figure 6-1: AXI4-Lite to DDR4 SDRAM Bridge Core in Pentek IP



6.1 Pentek IP Catalog (continued)

When you select the **px_axil2ddr_rq_v1_0** core, a screen appears that shows the core's symbol and the core's parameters (see Figure 6-2). The core's symbol is the box on the left side.

Figure 6-2: AXI4-Lite to DDR4 SDRAM Bridge Core IP Symbol



6.2 User Parameters

For a detailed explanation of the user parameters, refer to Section 2.5.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the *Vivado Design Suite User Guide - Designing with IP.*

6.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite environment.

Required Constraints

The XDC constraints for this core are not included in the Package IP. Clock constraints can be applied at the top level of the user design which includes this IP core.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale and Virtex-7 FPGAs.

Clock Frequencies

The clock frequency (**s_axi_aclk**) for this IP core is 250 MHz.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

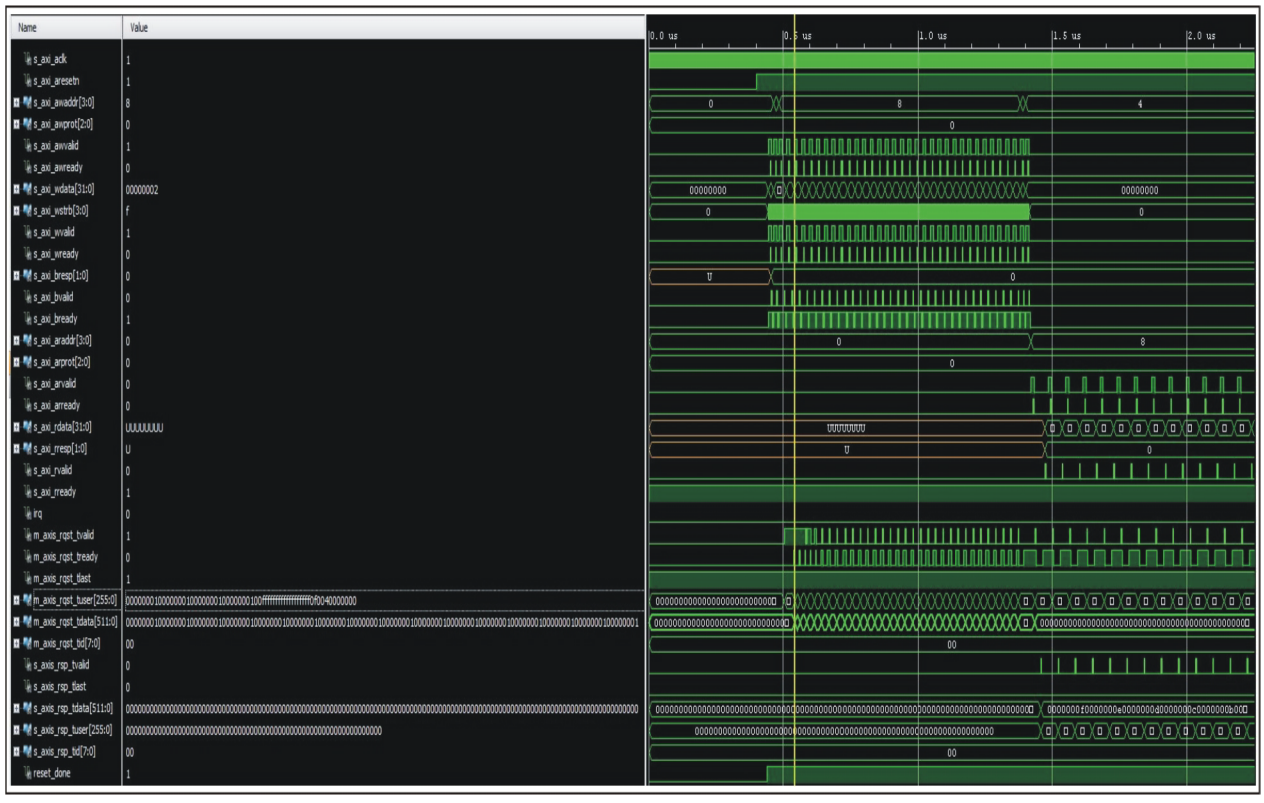
6.5 Simulation

The AXI4-Lite to DDR4 SDRAM Bridge Core has a test bench which generates the output waveforms using the Vivado VSim environment. The test bench is designed to run at 250 MHz clock frequency.

The test bench sets the requester ID to 0. It writes 32 DWords to the DDR4 SDRAM and reads the same from it. Since the AXI4-Lite to DDR4 SDRAM Bridge Core has auto increment mode, the DDR4 address is set once and incrementing data (0 to 31) is written into 32 contiguous address locations. The data written is stored in a test memory array and fed as data for DDR4 read responses.

The programming procedure is the same as described in Section 5.6. When run, the simulation produces the results shown in Figure 6-3.

Figure 6-3: AXI4-Lite to DDR4 SDRAM Bridge Core Test Bench Simulation Output



6.6 Synthesis and Implementation

For details about synthesis and implementation see the *Vivado Design Suite User Guide - Designing with IP*.