

IP CORE MANUAL



ADS5485 ADC Interface Core

px_ads5485intrfc

PENTEK

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IP Facts

Description

Pentek's Navigator™ ADS5485 ADC Interface Core serves as an interface to the Texas Instruments™ ADS5485 Analog to Digital converter.

This core complies with the ARM® AMBA® AXI4 specification. This manual defines the hardware interface, software interface, and parameterization options for the ADS5485 ADC Interface Core.

Features

- Provides offset and gain adjustment to the ADC Data
- Register access through AXI4-Lite interface
- Output data through AXI4-Stream Interface
- Differential Termination can be applied to inputs based on the user application requirement
- Performs data rounding and saturation operation after the offset and gain stage
- Detects data overload based on user defined overload settings
- Allows user to implement input buffers in low power or high performance mode
- Software programmable input tap delay at reset
- ADS5485 ADC dither mode and power down at reset can be enabled by the user
- Input delay control with adjustable reference clock frequency

Table 1-1: IP Facts Table	
Core Specifics	
Supported Design Family ^a	Kintex® Ultrascale
Supported User Interfaces	AXI4-Lite and AXI4-Stream
Resources	See Table 2-1
Provided with the Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided ^b
Constraints File	Not Provided ^c
Simulation Model	N/A
Supported S/W Driver	HAL Software Support
Tested Design Flows	
Design Entry	Vivado® Design Suite 2016.3 or later
Simulation	Vivado VSim
Synthesis	Vivado Synthesis
Support	
Provided by Pentek fpgasupport@pentek.com	

a. For a complete list of supported devices, see the [Vivado Design Suite Release Notes](#).

b. The test bench will be available in the next revision of this core.

c. Clock constraints can be applied at the top level module of the user design.

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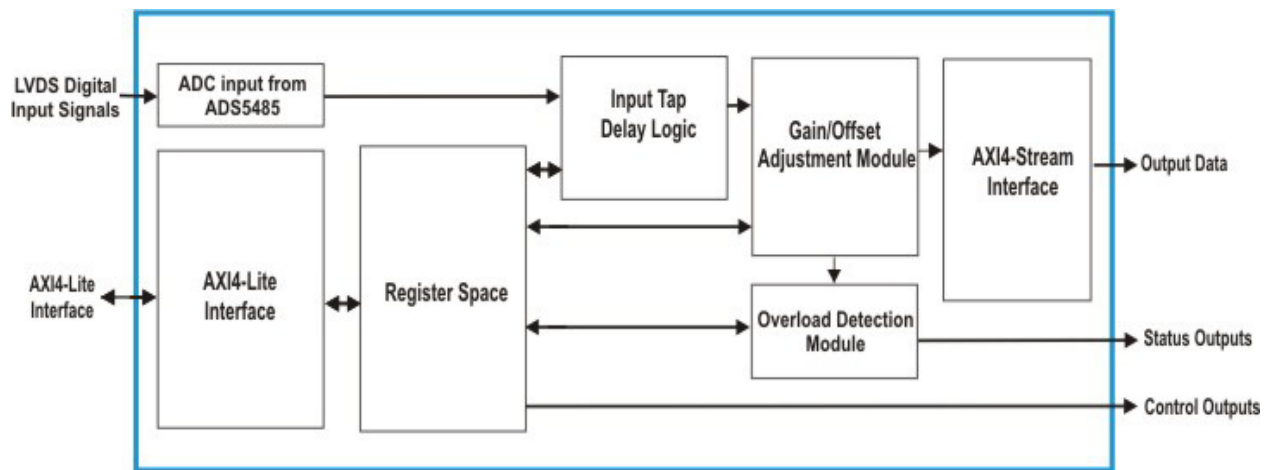
Chapter 1: Overview

1.1 Functional Description

The ADS5485 ADC Interface Core provides a transaction interface to the AXI4-Lite Interface. The AXI4-Lite interface acts as a slave and is connected to the Register Space as shown in [Figure 1-1](#), below. The ADC Core (ADS5485 ADC Interface Core) also has LVDS digital inputs from the ADS5485 ADC. The input data is passed through input tap delay, gain and offset adjustment and overload detection modules before obtaining the desired output through the AXI4-Stream Interface of the core. Control outputs (power down and dither) from the core are directed to the ADS5485 ADC.

[Figure 1-1](#) is the top level block diagram of the ADS5485 ADC Interface Core. The modules within the block diagram are explained in the later sections of this manual.

Figure 1-1: ADS5485 ADC Interface Core Block Diagram



- ❑ **AXI4-Lite Interface:** This module implements a 32-bit AXI4-Lite Slave interface to access the Register Space. For additional details about the AXI4-Lite Interface, refer to the [Section 3.1 AXI4-Lite Core Interfaces](#).
- ❑ **Register Space:** This module contains the control and status registers including Interrupt Enable, Interrupt Flag, and Interrupt Status registers. Registers are accessed through the AXI4-Lite interface.
- ❑ **Input Tap Delay Logic:** This module introduces delay to the incoming data. The delay to be introduced is determined from the generic parameter `initial_tap_delay`, defined by the user. Tap delay is used to achieve proper setup time on the input data lines.

1.1 Functional Description (continued)

- ❑ **Gain and Offset Adjustment:** This module serves to allow for gain and offset adjustment of the ADC data and also performs rounding, saturation operations on the data. This module returns a 16-bit signed value.
- ❑ **Overload Detection:** This module detects an overload in the ADC data and the gain/offset data. It indicates an overload through the overload LED.
- ❑ **AXI4-Stream Interface:** This module implements a 16-bit AXI4-Stream Master interface for the output data stream from the ADC Core. For additional details about the AXI4-Stream Interface, refer to the [Section 3.2 AXI4-Stream Core Interfaces](#).

1.2 Applications

This core can be used as an interface to the Texas Instruments ADS5485 Analog to Digital converter.

1.3 System Requirements

For a list of system requirements, see the [Vivado Design Suite Release Notes](#).

1.4 Licensing and Ordering Information

This core is included with all Pentek Navigator FPGA Design Kits for Pentek Jade series board products. Contact Pentek for Licensing and Ordering Information (www.pentek.com).

1.5 Contacting Technical Support

Technical Support for Pentek's Navigator FPGA Design Kits is available via e-mail (fpgasupport@pentek.com) or by phone (201-818-5900 ext. 238, 9 am to 5 pm EST).

1.6 Documentation

This user manual is the main document for this IP core. The following documents provide supplemental material:

- 1) *Vivado Design Suite User Guide: Designing with IP*
- 2) *Vivado Design Suite User Guide: Programming and Debugging*
- 3) *ARM AMBA AXI4 Protocol Version 2.0 Specification*
<http://www.arm.com/products/system-ip/amba-specifications.php>
- 4) *Texas Instruments ADS5485 Analog to Digital Converter Datasheet*

Chapter 2: General Product Specifications

2.1 Standards

The ADS5485 ADC Interface Core has bus interfaces that comply with the [ARM AMBA AXI4-Lite Protocol Specification](#) and the [AMBA AXI4-Stream Protocol Specification](#).

2.2 Performance

The performance of the ADC Core is limited by the maximum operating frequency of the ADS5485 Analog to Digital Converter. The values presented in this section should be used as an estimation guideline. Actual performance can vary.

2.2.1 Maximum Frequencies

The ADS5485 ADC has a maximum operating frequency of 200 MHz. The ADC Core is therefore designed to run at a maximum clock frequency of 200 MHz.

2.3 Resource Utilization

The resource utilization of the ADS5485 ADC Interface Core is shown in [Table 2-1](#). Resources have been estimated for the Kintex Ultrascale XCKU060 -2 speed grade device. These values were generated using the Vivado Design Suite.

Resource	# Used
LUTs	110
Flip-Flops	235

NOTE: Actual utilization may vary based on the user design in which the ADS5485 ADC Interface Core is incorporated.

2.4 Limitations and Unsupported Features

Does not support DMA transfer length less than a dword (4 bytes).

2.5 Generic Parameters

The generic parameters of the ADS5485 ADC Interface Core are described in [Table 2-2](#). These parameters can be set as required by the user application while customizing the core.

Table 2-2: Generic Parameters		
Port/Signal Name	Type	Description
iodelay_grp_01	String	IO Delay Group: This is a string label that is used to group the IODELAY tap delay components for all ADC channels within the user design with the corresponding IDELAY control component.
iodelay_grp_23		
iodelay_grp_45		
iodelay_grp_67		
iodelay_grp_89		
iodelay_grp_1011		
iodelay_grp_1213		
iodelay_grp_1415		
initial_tap_delay	Integer	Initial Tap Delay Value: This parameter defines the initial tap delay (in number of taps) to be introduced to the incoming data. It can range from 0 to 511.
initial_gain_percent		Initial Gain Percentage: This is the gain percentage for the ADC and is used to trim the gain of the input ADC signal of the core.
initial_offset_counts		Initial Offset Count: This is the initial DC offset trim for the ADC. This value is used to minimize ADC DC offset errors. It ranges from -32767 to 32767.
initial_2comp	Boolean	Initial Two's Complement: Defines the data format at reset. When set to True, the input data is converted to the 2's complement format by the core before processing.
initial_pdwnf		ADC is powered down at Reset: Defines the power saving mode for the ADS5485 ADC at reset. When set to True, the ADC is powered down to sleep mode at reset.
initial_dither		Initial ADC Dither: This signal is used to enable/disable the Dither mode of the ADS5485 ADC at reset. Active High.

Table 2-2: Generic Parameters (Continued)		
Port/Signal Name	Type	Description
initial_led_select	Integer	Initial LED Source Select at Reset: Selects the source of the LED at reset. 0 = ADC Input Overload 1 = Gain/Offset Trim Overload 2 = External Signal 3 = Disabled
differential_term	String	Differential Termination: Differential termination for the input. TERM_NONE = No differential termination for the inputs TERM_100 = 100 Ω differential termination
ibuf_low_pwr	Boolean	Input Buffer Low Power: Sets the input buffer performance. True = Input buffer implemented in low power mode; False = Input buffer implemented in high performance mode
has_ext_led_src		Has External LED Source: Indicates whether the core has an external LED source. This can be any signal from the user logic.
idelaycntrl_refclk_freq	Integer	IDelay Control Reference Clock: It is the reference clock frequency in MHz for the Input Tap Delay Logic block of this core. Typically this is 200 MHz.
initial_ovld_thresh		Initial Overload threshold: Sets the initial overload threshold value for overload detection. It can range from 0 to 32767.
led_pulse_stretch		LED Pulse Stretcher: The LED pulse is stretched based on this value to make short overload events more visible on the LED. It can range from 0 to 65535.

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Chapter 3: Port Descriptions

This chapter provides details about the port descriptions for the following interface types:

- [AXI4-Lite Core Interfaces](#)
- [AXI4-Stream Core Interfaces](#)
- [I/O Signals](#)

3.1 AXI4-Lite Core Interfaces

The ADS5485 ADC Interface Core uses the Control/Status Register (CSR) interface to control, and receive status from, the user design.

3.1.1 Control/Status Register (CSR) Interface

The CSR interface is an AXI4-Lite Slave Interface that can be used to access the control and status registers in the ADC Core. [Table 3-1](#) defines the ports in the CSR Interface. See [Chapter 4](#) for a Control/Status Register memory map and bit definitions. See the [AMBA AXI4-Lite Specification](#) for more details on operation of the AXI4-Lite interfaces.

Port	Direction	Width	Description
s_axi_csr_aclk	Input	1	Clock
s_axi_csr_aresetn	Input	1	Reset: Active low. This value will reset all control registers to their initial states.
s_axi_csr_awaddr	Input	7	Write Address: Address used for write operations. It must be valid when s_axi_csr_awvalid is asserted and must be held until s_axi_csr_awready is asserted by the ADC Core.
s_axi_csr_awprot	Input	3	Protection: The ADC interface core ignores these bits.
s_axi_csr_awvalid	Input	1	Write Address Valid: This input must be asserted to indicate that a valid write address is available on s_axi_csr_awaddr . The ADC Core asserts s_axi_csr_awready when it is ready to accept the address. The s_axi_csr_awvalid must remain asserted until the rising clock edge after the assertion of s_axi_csr_awready .

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	Direction	Width	Description
s_axi_csr_awready	Output	1	Write Address Ready: This output is asserted by the ADC Core when it is ready to accept the write address. The address is latched when s_axi_csr_wvalid and s_axi_csr_awready are high on the same cycle.
s_axi_csr_wdata	Input	32	Write Data: This data will be written to the address specified by s_axi_csr_awaddr when s_axi_csr_wvalid and s_axi_csr_wready are both asserted. The value must be valid when s_axi_csr_wvalid is asserted and held until s_axi_csr_wready is also asserted.
s_axi_csr_wstrb	Input	4	Write Strobes: This signal when asserted indicates the number of bytes of valid data on s_axi_csr_wdata signal. Each of these bits, when asserted indicate that the corresponding byte of s_axi_csr_wdata contains valid data. Bit 0 corresponds to the least significant byte, and bit 3 to the most significant.
s_axi_csr_wvalid	Input	1	Write Valid: This signal must be asserted to indicate that the write data is valid for a write operation. The value on s_axi_csr_wdata is written into the register at address s_axi_csr_awaddr when s_axi_csr_wready and s_axi_csr_wvalid are high on the same cycle.
s_axi_csr_wready	Output		Write Ready: This signal is asserted by the ADC Core when it is ready to accept data. The value on s_axi_csr_wdata is written into the register at address s_axi_csr_awaddr when s_axi_csr_wready and s_axi_csr_wvalid are high on the same cycle, assuming that the address has already or simultaneously been submitted.
s_axi_csr_bresp	Output	2	Write Response: The core indicates success or failure of a write transaction through this signal, which is valid when s_axi_csr_bvalid is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the AMBA AXI Specification .
s_axi_csr_bready	Input	1	Write Response Ready: This signal must be asserted by the user logic when it is ready to accept the Write Response.
s_axi_csr_bvalid	Output	1	Write Response Valid: This signal is asserted by the ADC Core when the write operation is complete and the Write Response is valid. It is held until s_axi_csr_bready is asserted by the user logic.

Table 3-1: Control/Status Register (CSR) Interface Port Descriptions (Continued)			
Port	Direction	Width	Description
s_axi_csr_araddr	Input	7	Read Address: Address used for read operations. It must be valid when s_axi_csr_arvalid is asserted and must be held until s_axi_csr_arready is asserted by the ADC Core.
s_axi_csr_arprot	Input	3	Protection: These bits are ignored by the ADC Core.
s_axi_csr_arvalid	Input	1	Read Address Valid: This input must be asserted to indicate that a valid read address is available on the s_axi_csr_araddr . The ADC Core asserts s_axi_csr_arready when it ready to accept the Read Address. This input must remain asserted until the rising clock edge after the assertion of s_axi_csr_arready .
s_axi_csr_arready	Output	1	Read Address Ready: This output is asserted by the ADC Core when it is ready to accept the read address. The address is latched when s_axi_csr_arvalid and s_axi_csr_arready are high on the same cycle.
s_axi_csr_rdata	Output	32	Read Data: This value is the data read from the address specified by the s_axi_csr_araddr when s_axi_csr_arvalid and s_axi_csr_arready are High on the same cycle.
s_axi_csr_rresp	Output	2	Read Response: The ADC Core indicates success or failure of a read transaction through this signal, which is valid when s_axi_csr_rvalid is asserted; 00 = Success of normal access 01 = Success of exclusive access 10 = Slave Error 11 = Decode Error Note: For more details about this signal refer to the AMBA AXI Specification .
s_axi_csr_rvalid	Output	1	Read Data Valid: This signal is asserted by the ADC Core when the read is complete and the read data is available on the s_axi_csr_rdata . It is held until s_axi_csr_rready is asserted by the user logic.
s_axi_csr_rready	Input		Read Data Ready: This signal is asserted by the user logic when it is ready to accept the Read Data.
irq	Output		Interrupt: This is an active High, edge type interrupt request output.

3.2 AXI4-Stream Core Interfaces

The ADS5485 ADC Interface Core has the following AXI4-Stream Interface, which is used to transfer data streams.

3.2.1 Stream Data (DATAIO_PD) Interface

This interface is used to transfer ADC data stream through the output ports of the ADC Core. [Table 3-2](#) defines the ports in the Stream Data Interface. This interface is an AXI4-Stream Master Interface that is used to output the ADC data. This AXI4-Stream bus is synchronous with the Sample Clock (**sample_clk**) input of the core. See the [AMBA AXI4-Stream Specification](#) for more details on the operation of the AXI4-Stream Interface.

Port	Direction	Width	Description
m_axis_dataio_pd_tdata	Output	16	Output Data
m_axis_dataio_pd_tvalid		1	Output Data Valid: Asserted when data is valid on the m_axis_dataio_pd_tdata . Since ADC data is available every clock cycle, m_axis_dataio_pd_tvalid remains High always.

3.3 I/O Signals

The I/O port/signal descriptions of the top level module of the ADS5485 ADC Interface Core are provided in [Table 3-3](#).

Port/Signal Name	Type	Direction	Description
ADS5485 ADC Input			
d0_1_p	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d0_1_n	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d2_3_p	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d2_3_n	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d4_5_p	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d4_5_n	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d6_7_p	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC

Table 3-3: I/O Signals (Continued)			
Port/Signal Name	Type	Direction	Description
d6_7_n	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d8_9_p	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d8_9_n	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d10_11_p	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d10_11_n	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d12_13_p	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d12_13_n	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d14_15_p	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
d14_15_n	std_logic	Input	LVDS Digital Data Input from the ADS5485 ADC
sample_clk	std_logic	Input	Sample Clock Input: This is the sample clock input from the ADS5485 ADC.
Control Outputs			
pdwnf	std_logic	Output	Power Down: Controls the power down mode of the ADS5485 ADC. Active High. This signal is to be connected externally to the ADS5485 ADC.
dither	std_logic	Output	Dither: Controls the dither mode of the ADS5485. Active High. This signal is to be connected externally to the ADS5485 ADC.
ovld_led_n	std_logic	Output	Overload LED Drive: This indicates an overload of the source of the LED selected by the user at reset. Active Low. The LED source is defined by the generic parameter <code>initial_led_select</code> .
ext_led_src	std_logic	Input	External LED Source: This is the external source, from the user design, to the Overload LED Drive.
Status Outputs			
adc_ovld	std_logic	Output	ADC Data Overload: Active High. This status bit indicates an overload of the incoming ADC data.
go_trim_ovld			Gain/Offset Trim Overload: Active High. This bit indicates an overload of the data from the gain/offset adjustment module.

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Chapter 4: Register Space

This chapter provides the memory map and register descriptions for the register space of the ADS5485 ADC Interface Core. The memory map is provided in [Table 4-1](#).

Register Name	Address (Base Address +)	Access	Description
Control Register 1	0x00	R/W	Controls the input tap delay.
Control Register 2	0x04		Controls the integer clock delay, two's complement, dither, power down, LED source select, and overload threshold count.
Gain/Offset Trim Control Register	0x08		This register holds the gain and offset trim values.
Reserved	0x0C	N/A	Reserved
Reserved	0x10		Reserved
Interrupt Enable Register	0x14	R/W	Interrupt enable bits
Interrupt Status Register	0x18	RO	Interrupt source status bits
Interrupt Flag Register	0x1C	R/Clr	Interrupt flag bits

4.1 Control Register 1

This register is used to control the input tap delay of the input data. This register is illustrated in Figure 4-1 and described in Table 4-2.

NOTE: The bits [8:0] are set based on the generic parameter `initial_tap_delay` defined by the user, which is used as the default value. The tap size may vary over temperature.

Figure 4-1: Control Register 1

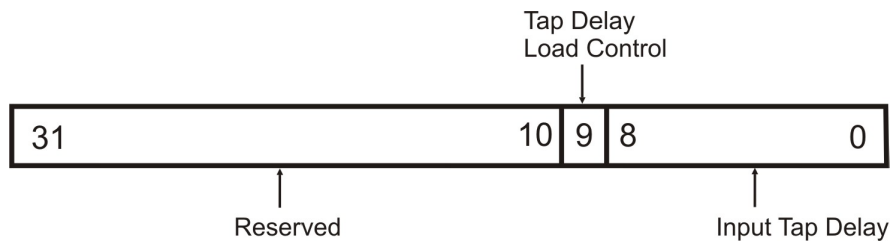


Table 4-2: Control Register 1 (Base Address + 0x00)				
Bits	Field Name	Default Value	Access Type	Description
31:10	Reserved	N/A	N/A	Reserved
9	dly_ld_ctl	0	R/W	Tap Delay Load Control: This bit controls loading of the tap delay value (bits [8:0]) into the Xilinx IDELAY component of the core. The IDELAY component is used to introduce tap delay to the incoming data. Toggling this bit '1' then '0' will enable the tap delay value to be loaded into the IDELAY component.
8:0	tap_delay	-		Input Tap Delay: These bits are used to control the number of taps required to introduce the desired delay to the input data of the core. The Kintex Ultrascale FPGA has a 512 tap delay line with a maximum delay value of 7600 ps and minimum delay value of 1250 ps.

4.2 Control Register 2

This register controls the integer clock delay, two's complement, dither, power down, LED source select, and overload threshold count of this core. This register is illustrated in Figure 4-2 and described in Table 4-3.

NOTE: The bits [31:16] and [6:2] are set based on the generic parameters defined by the user, which are used as default values.

Figure 4-2: Control Register 2

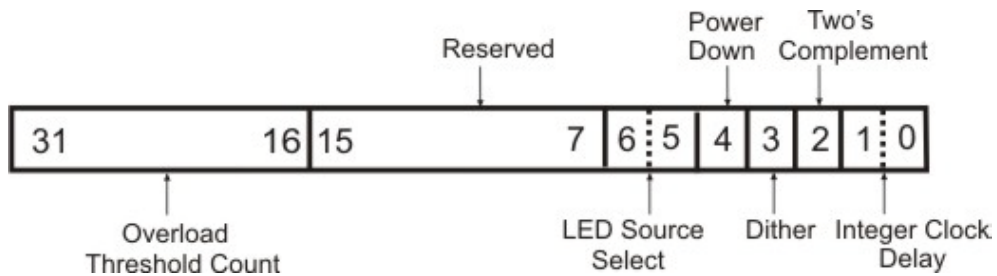


Table 4-3: Control Register 2 (Base Address + 0x04)

Bits	Field Name	Default Value	Access Type	Description
31:16	ovld_thresh_cnt	-	R/W	Overload Threshold Count: These bits set the overload threshold value for overload detection.
15:7	Reserved	N/A	N/A	Reserved
6:5	led_sel	-	R/W	LED Source Select: These bits select the source of the overload LED drive. 00 = ADC Input Overload 01 = Gain/Offset Trim Overload 10 = External Signal 11 = Disabled
4	pwdnf	-	R/W	Power Down: Controls the power down mode of ADS5485 ADC. For addition details about the power down modes of the ADS5485, refer to the Texas Instruments ADS5485 Analog to Digital Converter Datasheet . 0 = ADC is set to deep sleep mode 1 = ADC is set to light sleep mode

Table 4-3: Control Register 2 (Base Address + 0x04) (Continued)				
Bits	Field Name	Default Value	Access Type	Description
3	dither	-	R/W	Dither: Controls the dither mode of the ADS5485 ADC. For addition details about the dither mode of the ADS5485, refer to the Texas Instruments ADS5485 Analog to Digital Converter Datasheet . 0 = Dither mode disabled 1 = Dither mode enabled
2	twoscomp	-	R/W	Two's Complement: When set to '1', the input data is converted to the 2's complement format by the ADC Core before processing the data. 0 = No change in input data 1 = Two's complement of input data
1:0	int_delay	00	R/W	Integer Clock Delay: These bits are used to introduce an additional variable delay to the input data with respect to the sample clock frequency.

4.3 Gain/Offset Trim Control Register

This register holds the values of the gain and offset trim. This register is illustrated in [Figure 4-3](#) and described in [Table 4-4](#).

NOTE: The bits [31:0] are set based on the generic parameters defined by the user, which are used as default values.

Figure 4-3: Gain/Offset Trim Control Register

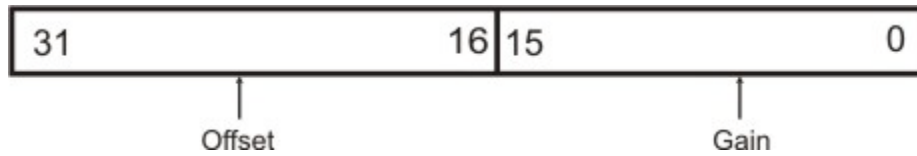


Table 4-4: Gain/Offset Trim Control Register (Base Address + 0x08)				
Bits	Field Name	Default Value	Access Type	Description
31:16	Offset	-	R/W	Offset: DC offset trim for the ADC. It is a 16-bit two's complement value.
15:0	Gain	-		Gain: Unsigned binary gain trim value for the ADC input. 0x0000 - zero gain 0x8000 - unity gain 0x8FFF - almost gain of 2

4.4 Interrupt Enable Register

The bits in the interrupt enable register are used to enable (or disable) the generation of interrupts based on the condition of certain circuit elements, known as interrupt sources. When a bit in this register associated with a given interrupt source is High, an interrupt will be generated by the rising edge of that source’s Interrupt Status Register bit (see Section 4.5). This register is illustrated in Figure 4-4 and the bits are described in Table 4-5.

Figure 4-4: Interrupt Enable Registers

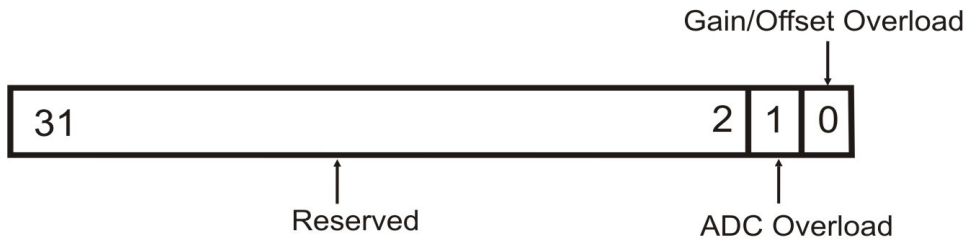


Table 4-5: Interrupt Enable Register (Base Address + 0x14)				
Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	N/A	N/A	Reserved
1	adc_ovld	0	R/W	ADC Overload: This bit enables/ disables the ADC overload interrupt source. 0 = Disable interrupt 1 = Enable interrupt
0	go_ovld			Gain/Offset Overload: This bit enables/ disables the overload interrupt source of ADC data after a gain/ offset adjustment. 0 = Disable interrupt 1 = Enable interrupt

4.5 Interrupt Status Register

The Interrupt Status Register has read-only access associated with each interrupt condition. A status bit changes to ‘1’ when the source interrupt occurs. When a status bit in this register changes to ‘1’ the corresponding flag bit in the Interrupt Flag Register is set to ‘1’. A status bit in this register clears to ‘0’ when that interrupt condition clears, whereas the associated flag bit in the Interrupt Flag Register remains at logic ‘1’ until it is explicitly cleared by the user.

Some of the interrupt sources are transient and so may not appear in the Interrupt Status Register at the time it is read. In such cases use the Interrupt Flag Register to see the interrupt conditions that have occurred. The Interrupt Status Register is illustrated in Figure 4-5 and the bits are described in Table 4-6.

Figure 4-5: Interrupt Status Registers

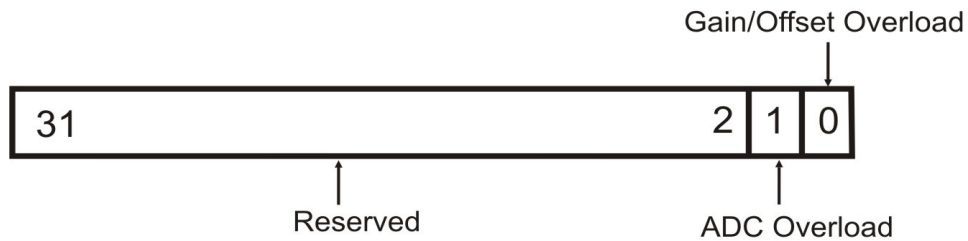


Table 4-6: Interrupt Status Register (Base Address + 0x18)				
Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	N/A	N/A	Reserved
1	adc_ovld	0	R	ADC Overload: This bit indicates the status of the ADC overload interrupt source. 0 = No interrupt 1 = Interrupt condition asserted
0	go_ovld			Gain/Offset Overload: This bit indicates the status of the overload interrupt source of ADC data after a gain/ offset adjustment. 0 = No interrupt 1 = Interrupt condition asserted

4.6 Interrupt Flag Register

The Interrupt Flag Register has read/clear access associated with each interrupt condition. When reset, this register has all bits set to ‘0’ (cleared). Each flag bit in this register latches an interrupt occurrence. A ‘1’ in any flag bit in this register indicates that an interrupt has occurred.

Note that when any status bit in the Interrupt Status Register, changes to ‘1’ the corresponding flag bit in this register will also be set to ‘1’. However, when a status bit in the Interrupt Status Register clears from ‘1’ to ‘0’, the corresponding latched flag bit in this register does not clear, but remains at ‘1’. To clear the flag bits, write ‘1’s to the desired bits. The flags are not affected by the Interrupt Enable Register. The Interrupt Flag Register is illustrated in Figure 4-5 and the bits are described in Table 4-6.

Figure 4-6: Interrupt Flag Registers

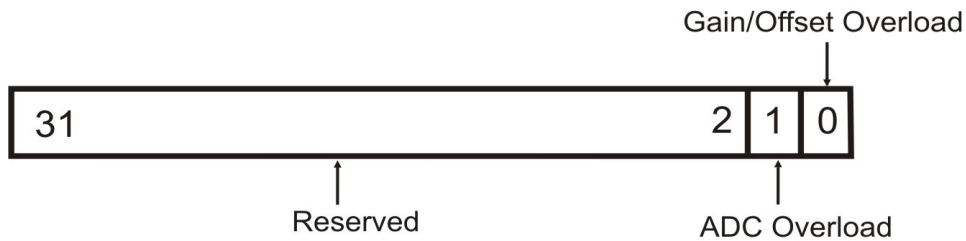


Table 4-7: Interrupt Flag Register (Base Address + 0x1C)

Bits	Field Name	Default Value	Access Type	Description
31:2	Reserved	N/A	N/A	Reserved
1	adc_ovld	0	R/Clr	ADC Overload: This bit indicates the ADC overload interrupt flag. Read: 0 = No interrupt 1 = Interrupt latched Clear: 1 = Clear latch
0	go_ovld			Gain/Offset Overload: This bit indicates the gain/ offset ADC overload interrupt flag. Read: 0 = No interrupt 1 = Interrupt latched Clear: 1 = Clear latch

Chapter 5: Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the ADS5485 ADC Interface Core.

5.1 General Design Guidelines

The ADS5485 ADC Interface Core is used as an interface to the Texas Instruments ADS5485 Analog to Digital Converter. It provides gain/offset adjustment and overload detection of the ADS5485 ADC output data.

5.2 Clocking

AXI4-Lite Clock: **s_axi_csr_aclk**

The **s_axi_csr_aclk** is used to clock the AXI4-Lite Control/Status Register (**s_axi_csr**) interface of the core.

ADC and AXI4-Stream Interface Clock: **sample_clk**

This clock is used to clock the ADS5485 inputs and AXI4-Stream outputs of the core.

5.3 Resets

Main reset: **s_axi_csr_aresetn**

This is an active low synchronous reset associated with the **s_axi_csr_aclk**. When asserted, all state machines in the core are reset, all FIFOs are flushed and all the control registers are cleared back to their initial default states.

5.4 Interrupts

This core has an edge type (rising edge-triggered) interrupt output. It is synchronous with the **s_axi_csr_aclk**. On the rising edge of any interrupt signal, a one clock cycle wide pulse is output from the core on its **irq** output. Each interrupt event is stored in two registers accessible on the **s_axi_csr** bus. The Interrupt Status Register always reflects the current state of the interrupt condition, which may have changed since the generation of the interrupt. The Interrupt Flag Register latches the occurrence of each interrupt, in a bit that retains its state until explicitly cleared.

The Interrupt flags can be cleared by writing '1' to the associated bit's location. All interrupt sources that are enabled (via the Interrupt Enable Register) are "OR ed" onto the **irq** output.

5.4 Interrupts (continued)

Note: All interrupt sources are latched in the interrupt flag register, even when an interrupt source is not enabled to create an interrupt.

Note: Because this core uses edge-triggered interrupts, the fact that an interrupt condition may remain active after servicing will not cause the generation of a new interrupt. A new interrupt will only be generated by another rising edge on an interrupt source.

5.5 Interface Operation

Control/Status Register Interface: This is the control/status register Interface. It is associated with the `s_axi_csr_ahb`. It is a standard AXI4-Lite type interface. See [Chapter 5](#) for the control register memory map, for more details on the registers that can be accessed through this interface.

Stream Data (DATAIO_PD) Interface: This interface is used to transfer output ADC data streams. It is a standard AXI4-Stream Master Interface. For more details about this interface refer to [Section 3.2.1](#).

5.6 Programming Sequence

This section briefly describes the programming sequence of registers to initiate and complete a transaction on the ADS5485 ADC Interface Core. The programming sequence for this core is as follows:

- 1) Ensure that the Interrupt Flag Register is cleared.
- 2) The input data passes through the tap delay logic and the gain/offset adjustment modules for the input delay, gain/offset adjustment defined by the control register bits.
- 3) The data passes through the overload detection block and indicates any overload through the Overload LED Drive.
- 4) The data is transferred across the output ports.

5.7 Timing Diagrams

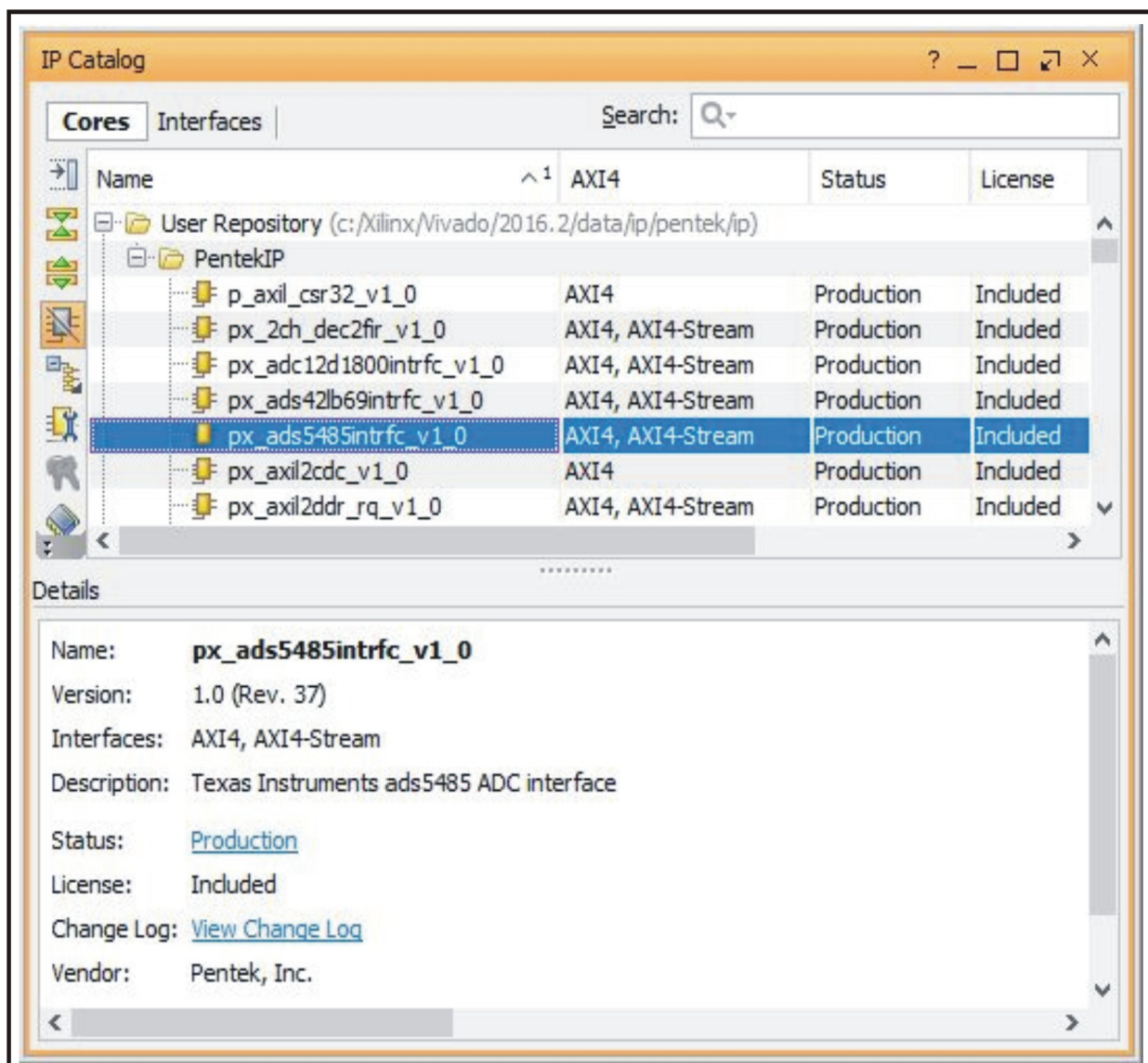
This section is not applicable to this IP core.

Chapter 6: Design Flow Steps

6.1 Pentek IP Catalog

This chapter describes customization and generation of the Pentek ADS5485 ADC Interface Core. It also includes simulation, synthesis and implementation steps that are specific to this core. This IP core can be generated from the Vivado IP Catalog when the Pentek IP Repository has been installed. It will appear in the IP Catalog list as **px_ads5485intrfc_v1_0** as shown in Figure 6-1.

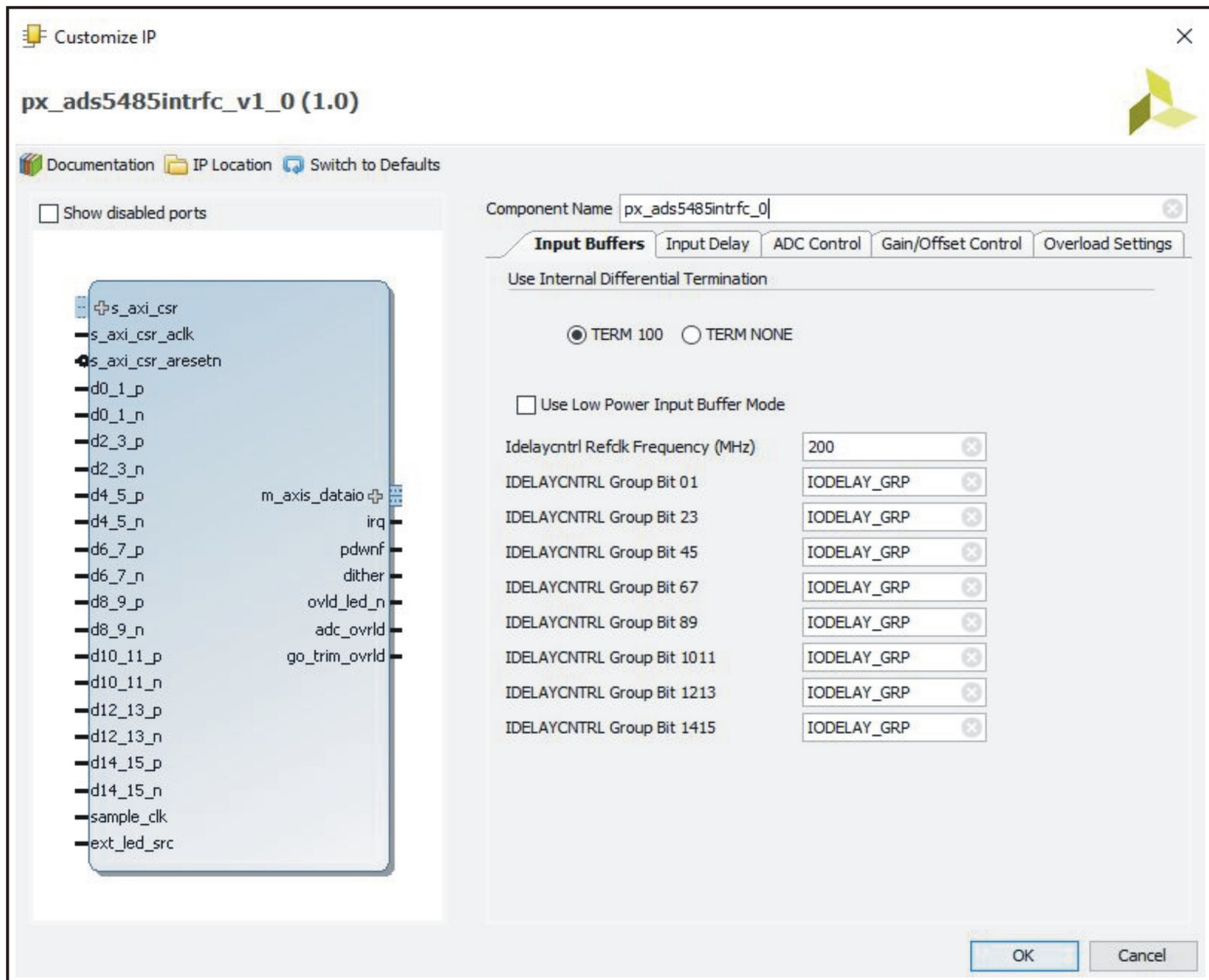
Figure 6-1: ADS5485 ADC Interface Core in Pentek IP Catalog



6.1 Pentek IP Catalog (continued)

When you select the `px_ads5485intrfc_v1_0` core, a screen appears that shows the core's symbol and the core's parameters (see [Figure 6-2](#)). The core's symbol is the box on the left side.

Figure 6-2: ADS5485 ADC Interface Core IP Symbol



6.2 User Parameters

6.2.1 Input Buffers

- **Internal Differential Termination:** Differential termination for the differential input signals. This can be used to turn the built-in, 100 Ω , differential termination on or off.
- **Use Low Power Input Buffer Mode:** This is used to enable low power mode operation of the input buffers.
- **Idelay Control Reference Clock Frequency:** This is the reference clock frequency for the idelaycntl module of the Xilinx Kintex Ultrascale FPGA. The typical reference clock frequency is 200 MHz.
- **IDELAYCNTRL Group Bits [01 - 1415]:** These are string labels used to group the IODELAY tap delay components for all ADC channels within the user design with the corresponding IDELAY control components.

6.2.2 Input Delay

- **Input Tap Delay at Reset:** This parameter indicates the number of taps required to introduce the desired delay to the inputs of the core at reset. It can range from 0-511.

6.2.3 ADC Control

- **Is 2's Complement format at Initialization:** This parameter sets the data format at reset. It is set to High when the incoming data is to be converted to 2's complement format before being processed.
- **Initial ADC Dither Setting at Reset:** This is used to control Dither mode of the ADS5485 ADC at reset. This signal is to be connected externally to ADS5485 ADC.
- **ADC is Powered Down at Reset:** This is used to control power down mode of the ADS5485 ADC at reset. This signal is to be connected externally to ADS5485 ADC.

6.2.4 Gain/Offset Control

- **Initial Offset counts at Reset:** The initial offset for the ADC can be defined using this parameter. It can range from -32767 to 32767.
- **Initial Gain percentage at Reset:** The initial gain percentage for the ADC is defined using this parameter.

6.2 User Parameters (continued)

6.2.5 Overload Settings

- **Overload LED Source Selection at Reset:** The overload LED drive source at reset can be selected by defining this parameter.

0 = ADC Input Overload;
1 = Gain/Offset Overload
2 = External Signal
3 = Disabled
- **Initial Overload Threshold Band:** This is the overload threshold for the overload detection module. It can range from 0 - 32767
- **LED Pulse Stretch Length:** The LED pulse is stretched for the length defined by this parameter to make short overload events more visible on the LED.
- **Has Auxiliary External LED Input Signal Source:** This is set to True if there is an external source for the LED drive.

6.3 Generating Output

For more details about generating and using IP in the Vivado Design Suite, refer to the [Vivado Design Suite User Guide - Designing with IP](#).

6.4 Constraining the Core

This section contains information about constraining the core in Vivado Design Suite.

Required Constraints

The XDC constraints are not provided with this core. The necessary constraints can be applied in the top level module of the user design.

Device, Package, and Speed Grade Selections

This IP works for the Kintex Ultrascale FPGAs.

Clock Frequencies

The maximum Sample clock (**sample_clk**) frequency for this IP core is 200 MHz while the AXI4-Lite interface clock (**s_axi_csr_aclk**) frequency is 250 MHz.

6.4 Constraining the Core (continued)

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking and Placement

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

6.5 Simulation

The test bench and the simulation results for this IP core will be available in the next revision of this manual.

6.6 Synthesis and Implementation

For details about synthesis and implementation see the [Vivado Design Suite User Guide - Designing with IP](#).

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