ADDENDUM MANUAL

MODEL 7807 – OPTION 110

XMC PCI Express Carrier – Optical Interface Programming

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Date	Revision	Comments
5/1/15	0.1	Initial release.

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Table of Contents

Page

Chapter 1: Model 7807–110 Optical Programming

Appendix A: Phillips Semiconductors Corporation, PCA9535 Data Sheet

Appendix B: Samtec Inc, FireFly™ Optical User Manual

Table of Contents

Page

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Chapter 1: Model 7807–110 Optical Programming

1.1 Overview

This addendum to the Model 7807 Operating Manual (800.78070) and the Onyx® Model 787xx series Installation Manuals (800.787xx) describes operation and programming of the Model 7807 Option 110 optical interface. Refer to the Model 7807 Operating Manual (800.78070) or the Onyx Model 787xx Installation Manual (800.787xx) provided with your shipment for description of the hardware and connections referenced in this addendum.

In addition to the programming instructions provided in this Option 110 Addendum Manual, copies of the manufacturers datasheets for the programmable devices in this optical interface are provided in the Appendices to this addendum manual.

1.2 TWSI (I^2C) Bus Interface

Programmable devices for the Option 110 optical interface are accessed using a TWSI (I^2C) bus interface. This bus is a two–wire, serial data (SDA) and serial clock (SCL), bi–directional bus, derived from the **J15 MSDA** and **MSCL** signals from the XMC mounted on the 7807. Refer to the operating manual for the Pentek XMC module you are using (800.717xx for a Pentek Onyx Model 787xx) for information on accessing this TWSI bus from the XMC.

The TWSI bus provides programming signals to the Samtec FireFly™ active optical receive and transmit modules connected to the 7807 connectors **J26** and **J27** (described in the Model 7807 Operating Manual, 800.78070). The TWSI bus provides access to a Philips Semiconductors PCA9535 I/O port serial to parallel converter for discrete con–trol lines, and to the FireFly Receive and Transmit modules for device programming, as illustrated below.

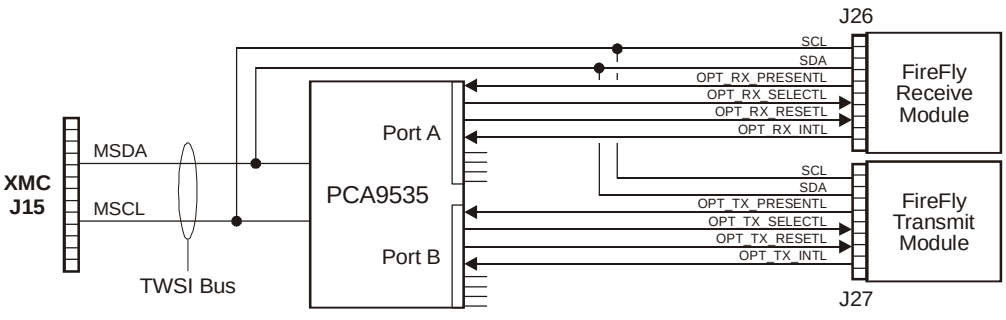

Figure 1–1: TWSI Bus interfaces

1.2 TWSI (I^2C) Bus Interface (continued)

The devices on the TWSI bus are accessed at the following bus addresses.

Device	Binary bus address	Description
FireFly Receive module	1010100h	Section 1.3
FireFly Transmit module	1010000h	Section 1.3
PCA9535	0100000h	Section 1.4

1.3 FireFly Receive and Transmit Modules Programming

The Samtec FireFly optical receive (**RX**) and transmit (**TX**) modules used with the 7807 each have a control interface on the TSWI bus at binary address 1010100h for receive module, and at binary address 1010000h for transmit module. Each module has a dis–crete select line that enables that module to send/receive data from the TWSI bus.

- Bit 1 of the PCA9535 Port A Register 2 (OPT_RX_SELECTL, Section 1.5.2.2) enables the optical receive module to send/receive data on the TWSI bus at binary address 1010100h

- Bit 1 of the PCA9535 Port B Register 3 (OPT_TX_SELECTL, Section 1.6.2.2) enables the optical transmit module to send/receive data on the TWSI bus at binary address 1010000h

Each FireFly module has internal registers that must be set up using the TWSI bus interface. Refer to the Samtec FireFly Optical User Manual, Appendix B, for program–ming information.

1.4 PCA9535 Programming

Model 7807 uses a Philips Semiconductors PCA9535 I^2C I/O port device, which is at binary address 0100000h on the TWSI bus. The PCA9535 has two 8–bit I/O ports; each port I/O pin can be configured as either input or output. The PCA9535 has eight regis–ters for programming the function of each pin, and reading from or writing to the pins.

The use of each I/O port is:

- Port A – Optical Receive Control, Section 1.5 – two input and two output pins

- Port B – Optical Transmit Control, Section 1.6 – two input and two output pins

Refer to the Philips Semiconductors Corporation PCA9535 Data Sheet, Appendix A, for programming information.

1.5 PCA9535 Port A – Optical Receive

PCA9535 Port A is connected to the optical receive module control connector **J26**, and is used to program the active interface and read status from it. Port A is accessed and controlled using PCA9535 internal registers 0, 2, 4, and 6 as follows:

- Register 0 – Data input from Port A
- Register 2 – Data output to Port A
- Register 4 – Invert input data from Port A
- Register 6 – I/O control of Port A

1.5.1 Port A, Register 0 – Input Data (READ ONLY)

Table 1–1: PCA Register 0: Port A Data Input

	7 – 4	3	2 – 1	0
Bit Name	NOT USED	OPT_RX_INTL	NOT USED	OPT_RX_PRESENTL
Function	Mask when reading	0 = Interrupt 1 = No Interrupt	Mask when reading	0 = Present 1 = Not Present

1.5.1.1 OPT_RX_INTL

This bit indicates an interrupt from the optical receive module. A "1" indicates no interrupt; a "0" indicates an interrupt is present. Refer to the Samtec FireFly data sheet for interpretation of this interrupt.

1.5.1.2 OPT_RX_PRESENTL

This bit indicates the presence of the optical receive module on this connector. A "1" indicates that it is not present; a "0" indi–cates the module is present.

1.5 PCA9535 Port A – Optical Receive (continued)

1.5.2 Port A, Register 2 – Output Data (WRITE ONLY)

Table 1–2: PCA Register 2: Port A Data Output				
	7 – 3	2	1	0
Bit Name	NOT USED	OPT_RX_RESETL	OPT_RX_SELECTL	NOT USED
Function	Write zeros	0 = Reset 1 = Run	0 = Select 1 = Do not select	Write zero

1.5.2.1 OPT_RX_RESETL

This bit resets the optical receive module. A "0" holds the device in a reset state, a "1" allows it to run.

1.5.2.2 OPT_RX_SELECTL

This bit selects the serial interface pins of the optical receive module (SDA and SCL). A "0" enables the optical receive serial interface and allows this module to communicate on the TWSI bus; a "1" disables the TWSI interface.

1.5.3 Port A, Register 4 – Polarity Control

Input data inversion on the Model 7807 is not used. Since the power–on default state of all bits is "0", this register does not require programming

1.5.4 Port A, Register 6 – I/O Control

To configure a port pin as an output, set the corresponding register bit to "0". To configure a pin as an input, set the register bit to "1". The following shows the bit settings for Port A, where bits 3 and 0 are the only input pins.

Table 1–3: PCA Register 6: Port A I/O Control								
	7	6	5	4	3	2	1	0
Function	0	0	0	0	1	0	0	1

1.6 PCA9535 Port B – Optical Transmit

PCA9535 Port B is connected to the optical transmit module control connector **J27**, and is used to program the active interface and read status from it. Port B is accessed and controlled using PCA9535 internal registers 1, 3, 5, and 7, as follows:

- Register 1 – Data input from Port B
- Register 3 – Data output to Port B
- Register 5 – Invert input data from Port B
- Register 7 – I/O control of Port B

1.6.1 Port B, Register 1 – Input Data (READ ONLY)

Table 1–4: PCA Register 1: Port B Data Input

	7 – 4	3	2 – 1	0
Bit Name	NOT USED	OPT_TX_INTL	NOT USED	OPT_TX_PRESENTL
Function	Mask when reading	0 = Interrupt 1 = No Interrupt	Mask when reading	0 = Present 1 = Not Present

1.6.1.1 OPT_TX_INTL

This bit indicates an interrupt from the optical transmit module. A "1" indicates no interrupt; a "0" indicates an interrupt is present. Refer to the Samtec FireFly data sheet for interpretation of this interrupt.

1.6.1.2 OPT_TX_PRESENTL

This bit indicates the presence of an optical transmit module on this connector. A "1" indicates that it is not present; a "0" indicates the module is present.

1.6 PCA9535 Port B – Optical Transmit (continued)

1.6.2 Port B, Register 3 – Output Data (WRITE ONLY)

Table 1–5: PCA Register 3: Port B Data Output				
	7 – 3	2	1	0
Bit Name	NOT USED	OPT_TX_RESETL	OPT_TX_SELECTL	NOT USED
Function	Write zeros	0 = Reset 1 = Run	0 = Select 1 = Do not select	Write zero

1.6.2.1 OPT_TX_RESETL

This resets the optical transmit module. A "0" holds the device in a reset state, a "1" allows it to run.

1.6.2.2 OPT_TX_SELECTL

This bit selects the serial interface pins of the optical transmit module (SDA and SCL). A "0" enables the optical transmit serial interface and allows this module to communicate on the TWSI bus; a "1" disables the TWSI interface.

1.6.3 Port B, Register 5 – Polarity Control

Input data inversion on the Model 7807 is not used. Since the power–on default state of all bits is "0", this register does not require programming

1.6.4 Port B, Register 7 – I/O Control

To configure a port pin as an output, set the corresponding register bit to "0". To configure a pin as an input, set the register bit to "1". The following shows the bit settings for Port B, where bits 3 and 0 are the only input pins.

Table 1–6: PCA Register 7: Port B I/O Control								
	7	6	5	4	3	2	1	0
Function	0	0	0	0	1	0	0	1

Appendix A: Phillips Semiconductors Corporation, PCA9535 Data Sheet

A.1 Introduction

The following pages are a reprint of the Phillips Semiconductors Corporation, PCA9535 16–bit I^2C and SMBus I/O port Data Sheet.

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DATA SHEET

PCA9535

16-bit I^2C and SMBus, low power I/O port with interrupt

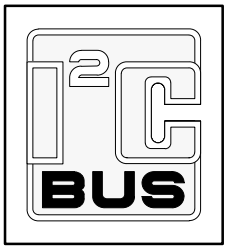
Product data

2003 Jun 27

Philips
Semiconductors

PHILIPS

16-bit I²C and SMBus, low power I/O port with interrupt PCA9535



FEATURES

- Operating power supply voltage range of 2.3 V-5.5 V
- 5 V tolerant I/Os
- Polarity inversion register
- Active LOW interrupt output
- Low stand-by current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 16 I/O pins which default to 16 inputs
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Offered in three different packages: SO24, TSSOP24, and HVQFN24

DESCRIPTION

The PCA9535 is a 24-pin CMOS device that provide 16 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C/SMBus applications and was developed to enhance the Philips family of I²C I/O expanders. The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, LEDs, fans, etc.

The PCA9535 consist of two 8-bit Configuration (Input or Output selection); Input, Output and Polarity inversion (Active HIGH or Active LOW operation) registers. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion Register. All registers can be read by the system master. Although pin-to-pin and I²C address compatible with the PCF8575, software changes are required due to the enhancements and are discussed in Application Note AN469.

The PCA9535 is identical to the PCA9555 except for the removal of the internal I/O pull-up resistor which greatly reduces power consumption when the I/Os are held LOW.

The PCA9535 open-drain interrupt output is activated when any input state differs from its corresponding input port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I²C address and allow up to eight devices to share the same I²C/SMBus. The fixed I²C address of the PCA9535 is the same as the PCA9554 allowing up to eight of these devices in any combination to share the same I²C/SMBus.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
24-Pin Plastic SO	-40 to +85 °C	PCA9535D	PCA9535D	SOT137-1
24-Pin Plastic TSSOP	-40 to +85 °C	PCA9535PW	PCA9535PW	SOT355-1
24-Pin Plastic HVQFN	-40 to +85 °C	PCA9535BS	9535	SOT616-1

Standard packing quantities and other packing data are available at *www.philipslogic.com/packaging*.

PIN CONFIGURATION — SO, TSSOP

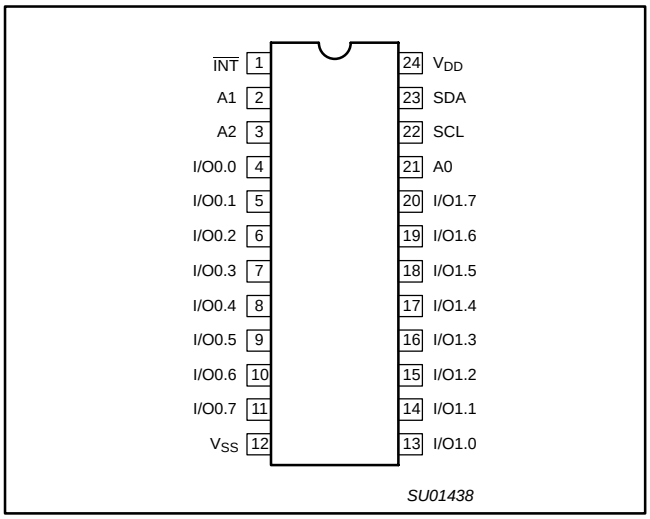


Figure 1. Pin configuration — SO, TSSOP

PIN CONFIGURATION —HVQFN

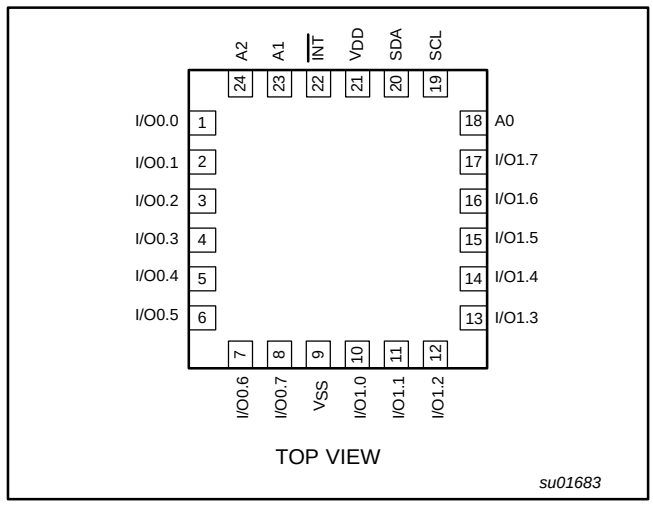


Figure 2. Pin configuration — HVQFN

PIN DESCRIPTION

SO, TSSOP PIN NUMBER	HVQFN PIN NUMBER	SYMBOL	FUNCTION
1	22	$\overline{INT}$	Interrupt output (open drain)
2	23	A1	Address input 1
3	24	A2	Address input 2
4-11	1-8	I/O0.0-I/O0.7	I/O0.0 to I/O0.7
12	9	V_{SS}	Supply ground
13-20	10-17	I/O1.0-I/O1.7	I/O1.0 to I/O1.7
21	18	A0	Address input 0
22	19	SCL	Serial clock line
23	20	SDA	Serial data line
24	21	V_{DD}	Supply voltage

BLOCK DIAGRAM

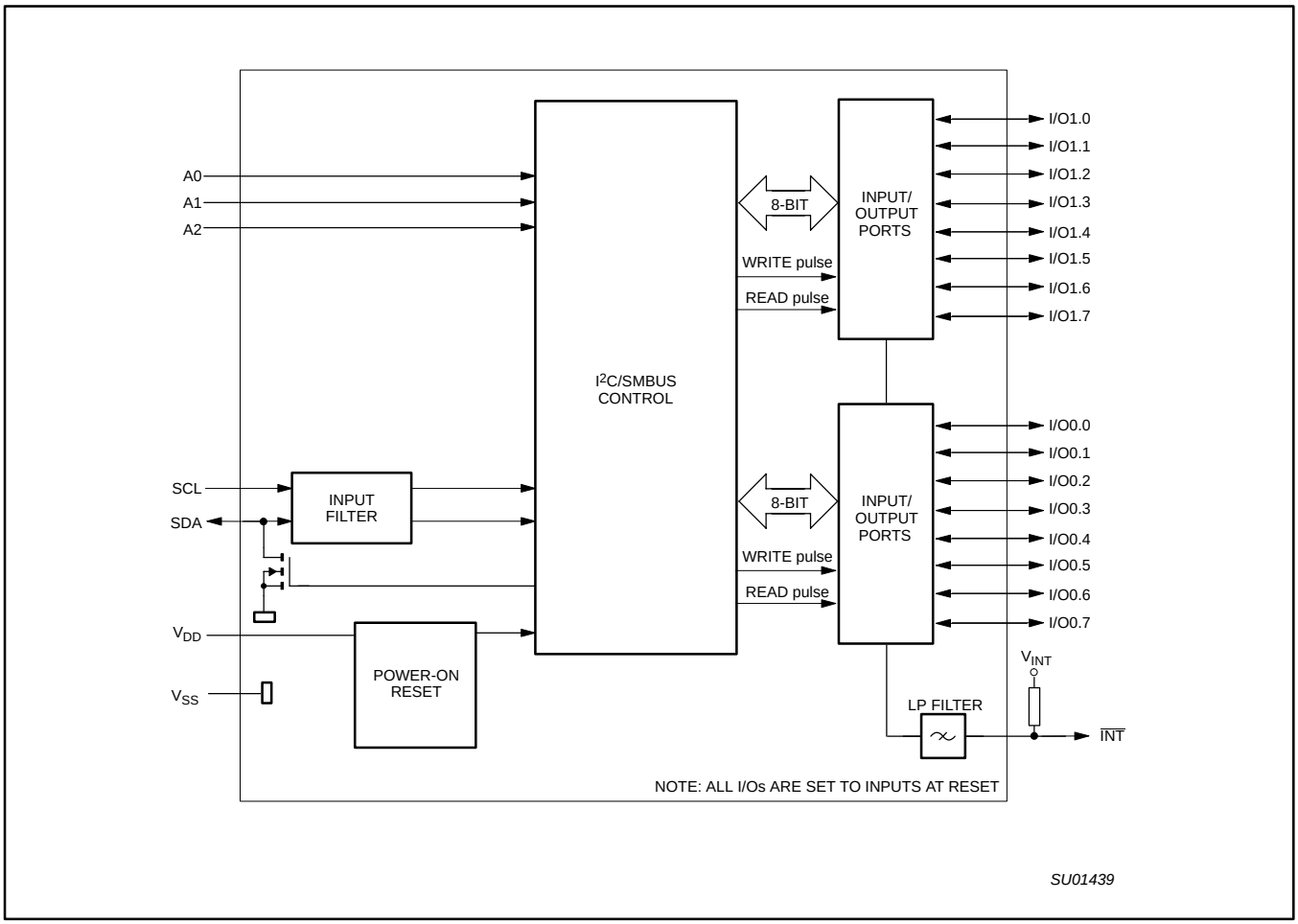
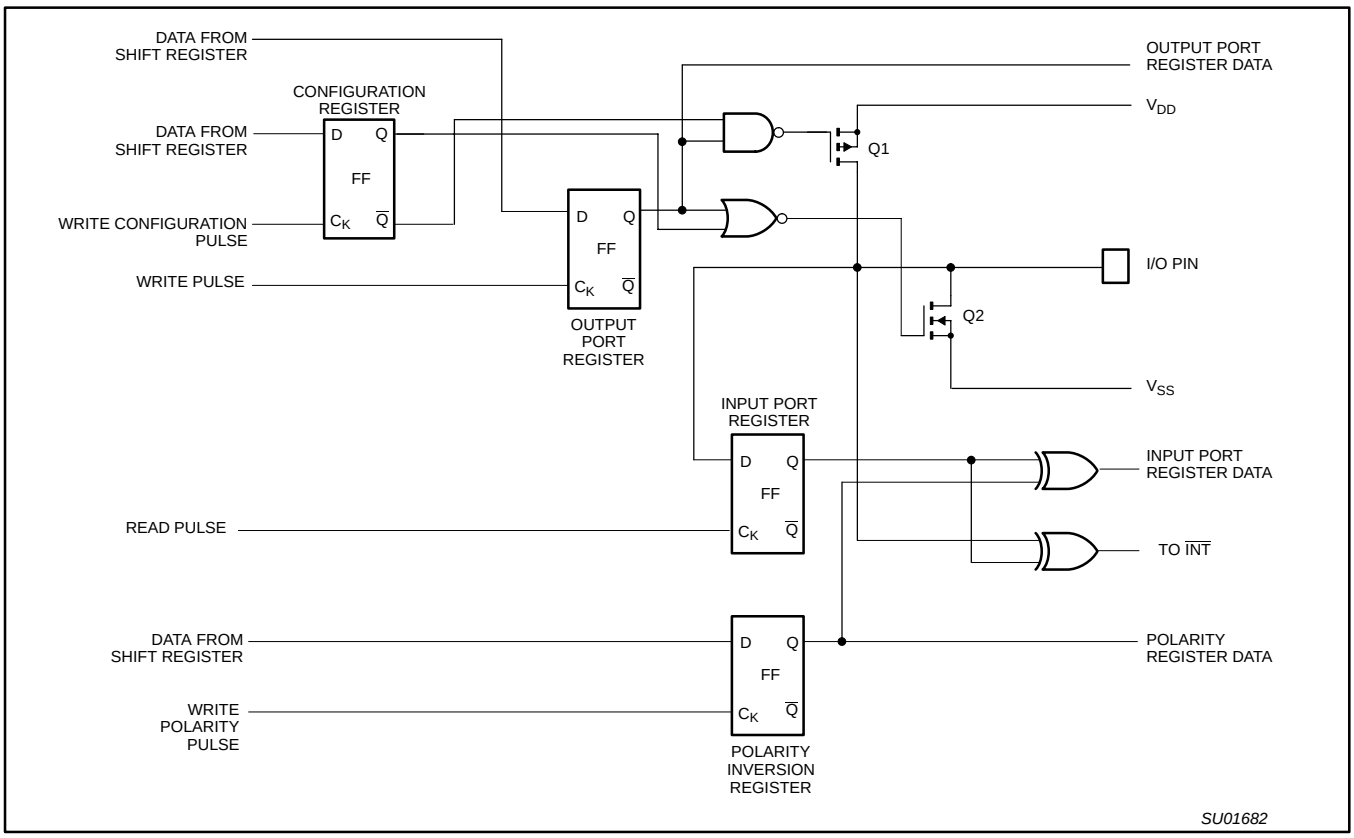


Figure 3. Block diagram

SIMPLIFIED SCHEMATIC OF I/Os



NOTE: At Power-on Reset, all registers return to default values.

Figure 4. Simplified schematic of I/Os

I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low impedance path that exists between the pin and either V_{DD} or V_{SS}.

REGISTERS

Command Byte

Command	Register
0	Input port 0
1	Input port 1
2	Output port 0
3	Output port 1
4	Polarity inversion port 0
5	Polarity inversion port 1
6	Configuration port 0
7	Configuration port 1

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Registers 0 and 1 — Input Port Registers

This register is an input-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

Registers 2 and 3 — Output Port Registers

bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
default	1	1	1	1	1	1	1	1
bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
default	1	1	1	1	1	1	1	1

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Register 6 and 7. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

Registers 4 and 5 — Polarity Inversion Registers

bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
default	0	0	0	0	0	0	0	0
bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
default	0	0	0	0	0	0	0	0

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the Input Port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

Registers 6 and 7 — Configuration Registers

bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
default	1	1	1	1	1	1	1	1
bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. At reset the device's ports are inputs.

POWER-ON RESET

When power is applied to V_{DD}, an internal power-on reset holds the PCA9535 in a reset state until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9535 registers and SMBus state machine will initialize to their default states.

DEVICE ADDRESS

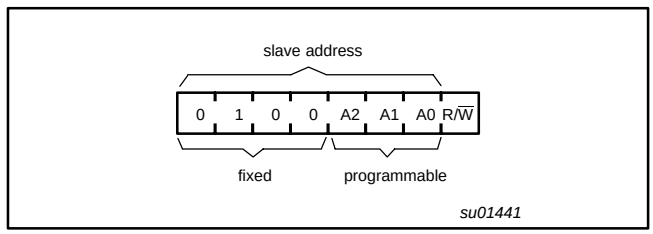


Figure 5. PCA9535 address

BUS TRANSACTIONS

Writing to the port registers

Data is transmitted to the PCA9535 by sending the device address and setting the least significant bit to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register will receive the data following the command byte.

The eight registers within the PCA9535 are configured to operate as four register pairs. The four pairs are Input Ports, Output Ports, Polarity Inversion Ports, and Configuration Ports. After sending data to one register, the next data byte will be sent to the other register in the pair (see Figures 6 and 7). For example, if the first byte is sent to Output Port (register 3), then the next byte will be stored in Output Port 0 (register 2). There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

Reading the port registers

In order to read data from the PCA9535, the bus master must first send the PCA9535 address with the least significant bit set to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again but this time, the least significant bit is set to a logic 1. Data from the register defined by the command byte will then be sent by the PCA9535 (see Figures 8 , 9, and 10). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data will now reflect the information in the other register in the pair. For example, if you read Input Port 1, then the next byte read would be Input Port 0. There is no limitation on the number of data bytes received in one read transmission but the final byte received, the bus master must not acknowledge the data.

Interrupt Output

The open-drain interrupt output is activated when one of the port pins change state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or the input port register is read (see Figure 9). A pin configured as an output cannot cause an interrupt. Since each 8-bit port is read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1 or the other way around.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

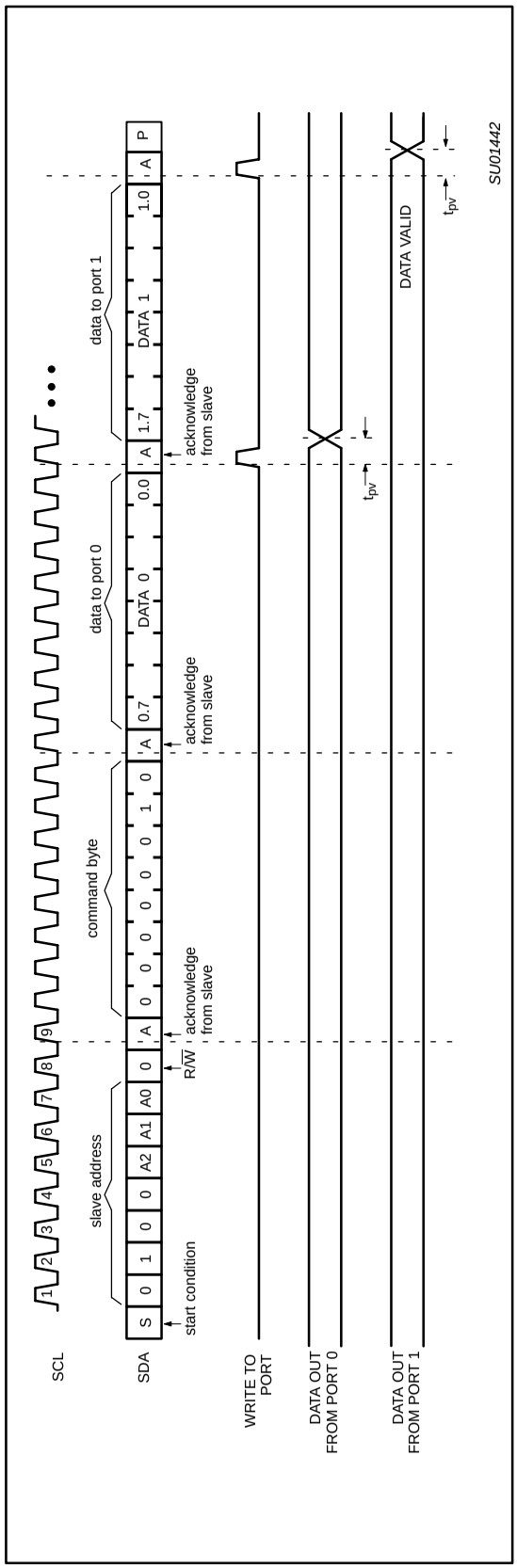


Figure 6. WRITE to output port registers

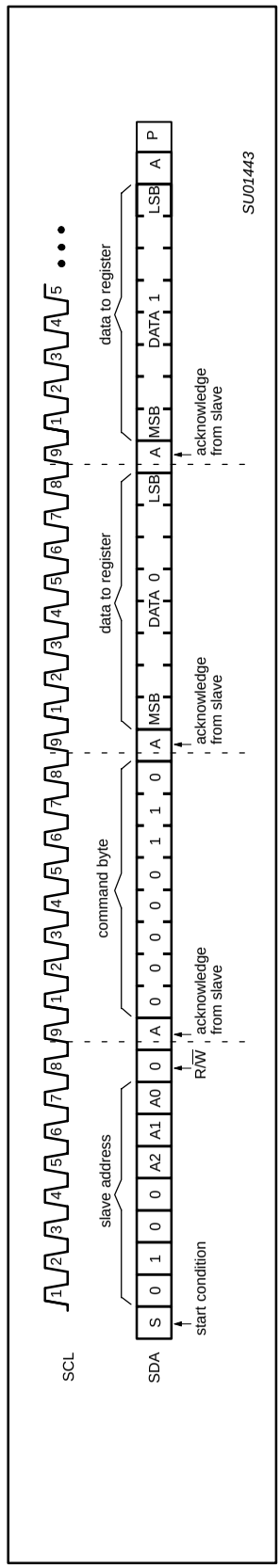
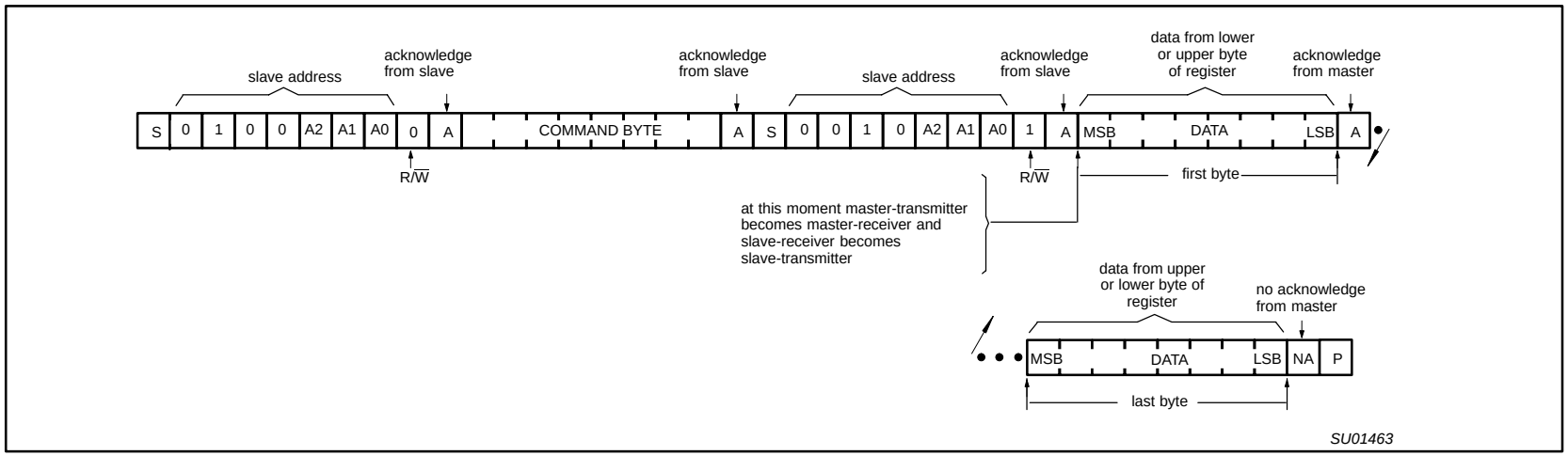
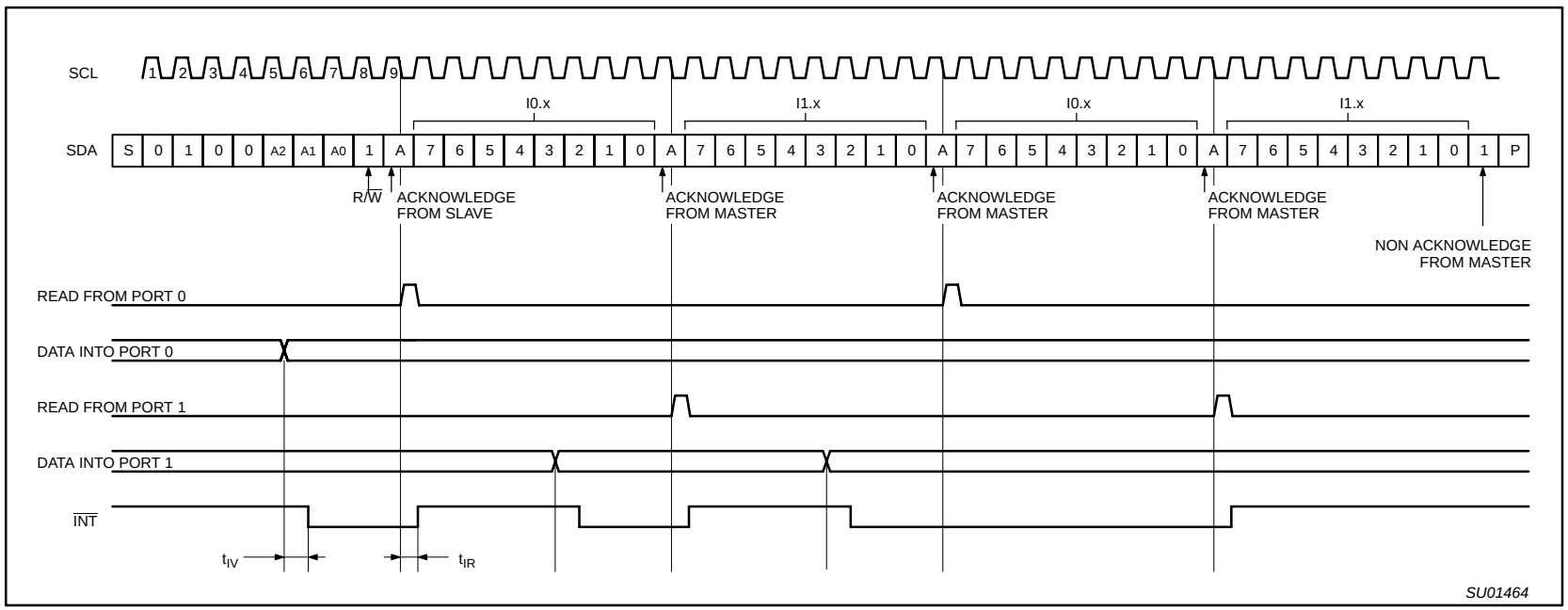


Figure 7. WRITE to configuration registers



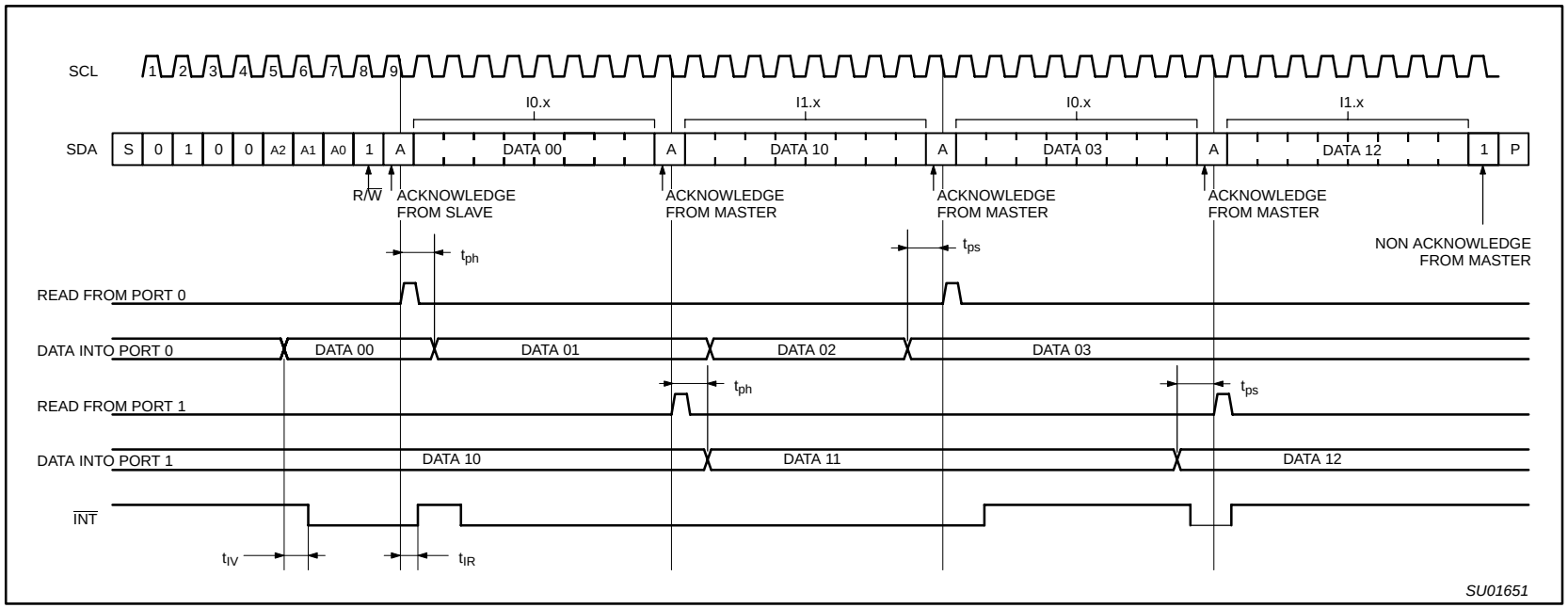
NOTE: Transfer can be stopped at any time by a STOP condition.

Figure 8. READ from register



NOTES: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to 00 (read input port port register).

Figure 9. READ input port register — scenario 1



NOTES: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to 00 (read input port port register).

Figure 10. READ input port register — scenario 2

TYPICAL APPLICATION

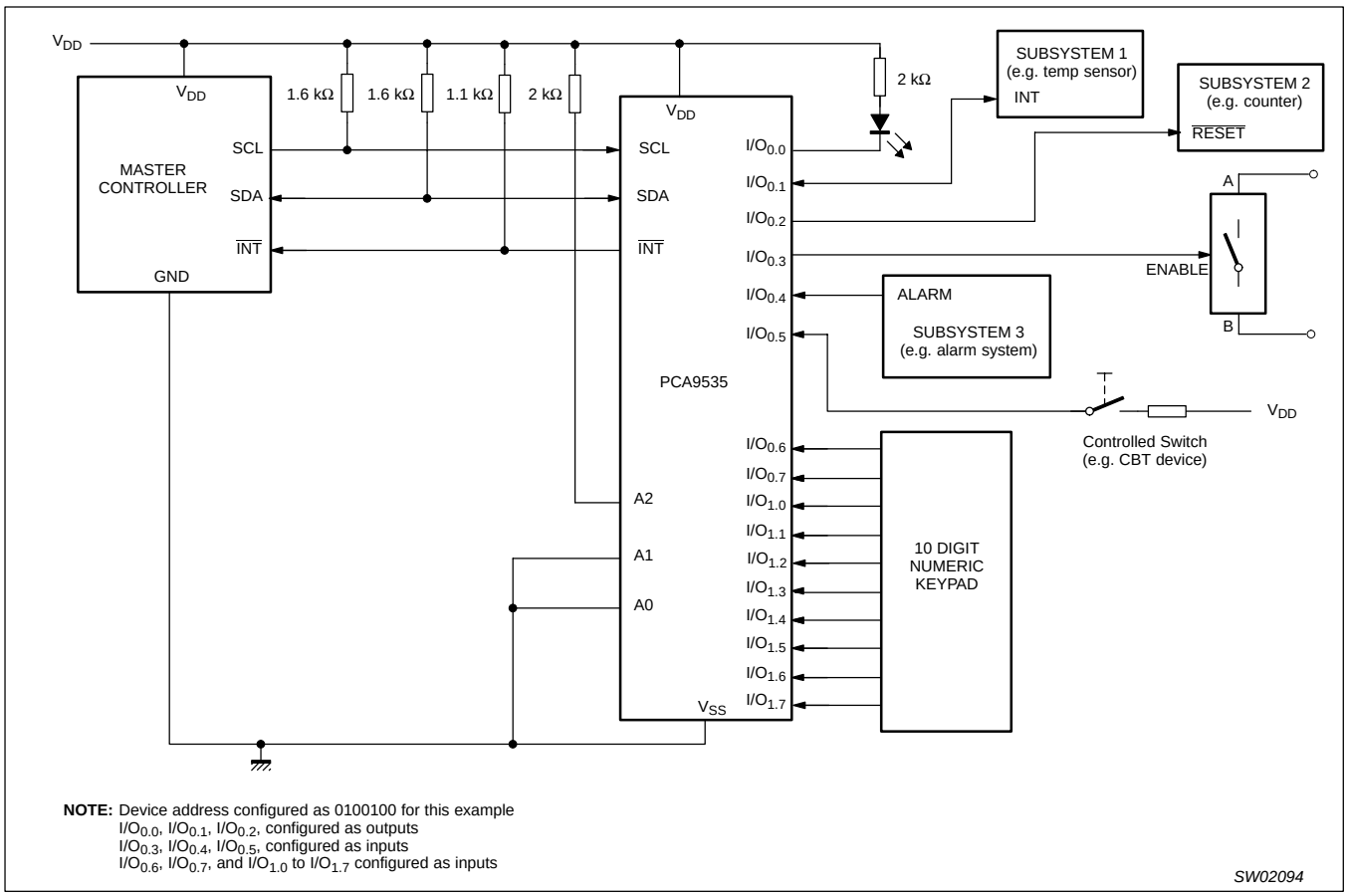


Figure 11. Typical application

Minimizing I_{DD} when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V_{IN} is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_{IN} becomes lower than V_{DD} and is specified as ΔI_{DD} in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 12 shows a high value resistor in parallel with the LED. Figure 13 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{DD} and prevents additional supply current consumption when the LED is off.

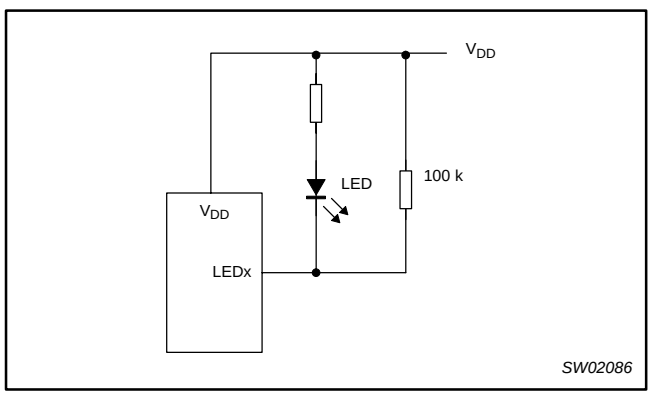


Figure 12. High value resistor in parallel with the LED

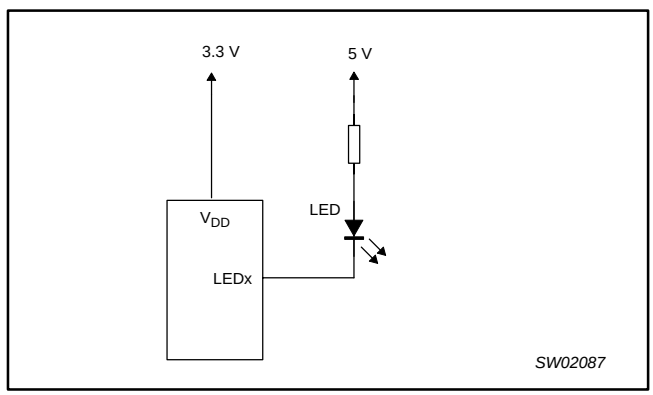


Figure 13. Device supplied by a lower voltage

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		-0.5	6.0	V
$V_{I/O}$	DC input current on an I/O		V_{SS} - 0.5	6	V
$I_{I/O}$	DC output current on an I/O		—	± 50	mA
I_I	DC input current		—	± 20	mA
I_{DD}	Supply current		—	160	mA
I_{SS}	Supply current		—	200	mA
P_{tot}	Total power dissipation		—	200	mW
T_{stg}	Storage temperature range		-65	+150	°C
T_{amb}	Operating ambient temperature		-40	+85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = -40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz; I/O = inputs	—	135	200	µA
I_{stbl}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	µA
I_{stbh}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	µA
V_{POR}	Power-on reset voltage	No load; $V_I = V_{DD}$ or V_{SS}	—	1.5	1.65	V
input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	3	—	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	6	10	pF
I/Os						
V_{IL}	LOW-level input voltage		-0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3-5.5 V; Note 1	8	8-20	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3-5.5 V; Note 1	10	10-24	—	mA
V_{OH}	HIGH-level output voltage	I_{OH} = -8 mA; V_{DD} = 2.3 V; Note 2	1.8	—	—	V
		I_{OH} = -10 mA; V_{DD} = 2.3 V; Note 2	1.7	—	—	V
		I_{OH} = -8 mA; V_{DD} = 3.0 V; Note 2	2.6	—	—	V
		I_{OH} = -10 mA; V_{DD} = 3.0 V; Note 2	2.5	—	—	V
		I_{OH} = -8 mA; V_{DD} = 4.75 V; Note 2	4.1	—	—	V
		I_{OH} = -10 mA; V_{DD} = 4.75 V; Note 2	4.0	—	—	V
I_{IH}	Input leakage current	V_{DD} = 5.5 V; $V_I = V_{DD}$	—	—	1	µA
I_{IL}	Input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$	—	—	-1	µA
C_I	Input capacitance		—	3.7	5	pF
C_O	Output capacitance		—	3.7	5	pF
Interrupt $\overline{INT}$						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	—	—	mA
Select Inputs A0, A1, A2						
V_{IL}	LOW-level input voltage		-0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{LI}	Input leakage current		-1	—	1	µA

NOTES:

1. The total current sunk by all I/Os must be limited to 200 mA.
2. The total current sourced by all I/Os must be limited to 160 mA.

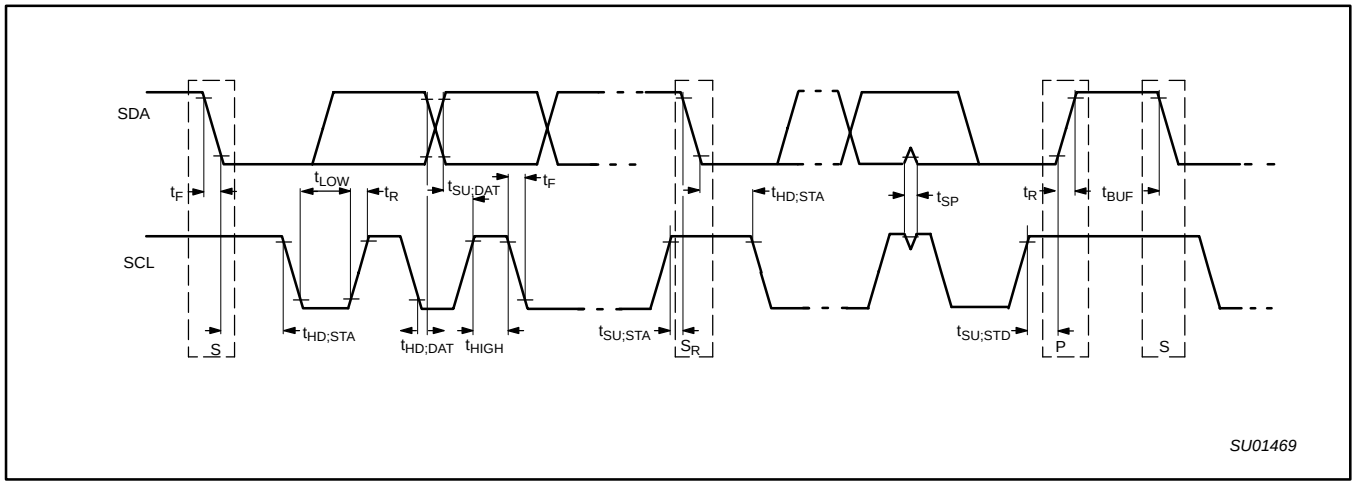
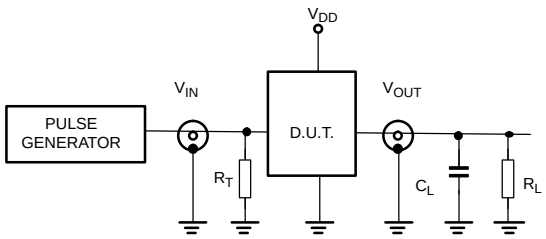


Figure 14. Definition of timing

AC CHARACTERISTICS

SYMBOL	PARAMETER	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	—	0.6	—	µs
$t_{VD;ACK}$	Valid time of ACK condition[2]	0.3	3.45	0.1	0.9	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;DAT}$	Data out valid time[3]	300	—	50	—	ns
$t_{SU;DAT}$	Data set-up time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	$20 + 0.1C_b$ [1]	300	ns
t_R	Clock/Data rise time	—	1000	$20 + 0.1C_b$ [1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data set-up time	150	—	150	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs
Interrupt Timing						
t_{IV}	Interrupt valid	—	4	—	4	µs
t_{IR}	Interrupt reset	—	4	—	4	µs

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
4. t_{PV} measured from $0.7V_{DD}$ on SCL to 50% I/O output.



TEST CIRCUIT FOR OUTPUTS

DEFINITIONS

R_L = 1 kΩ

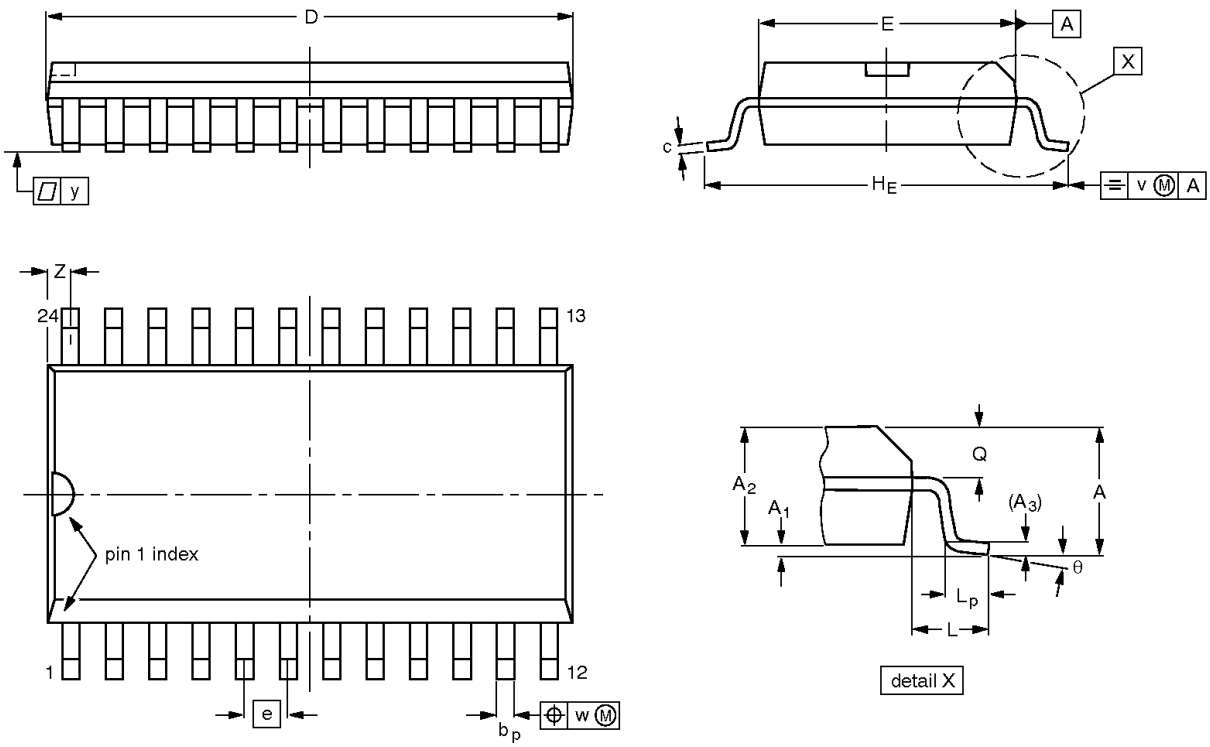
C_L = 50 pF

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

su01760

Figure 15. t_{PV} set-up conditions

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

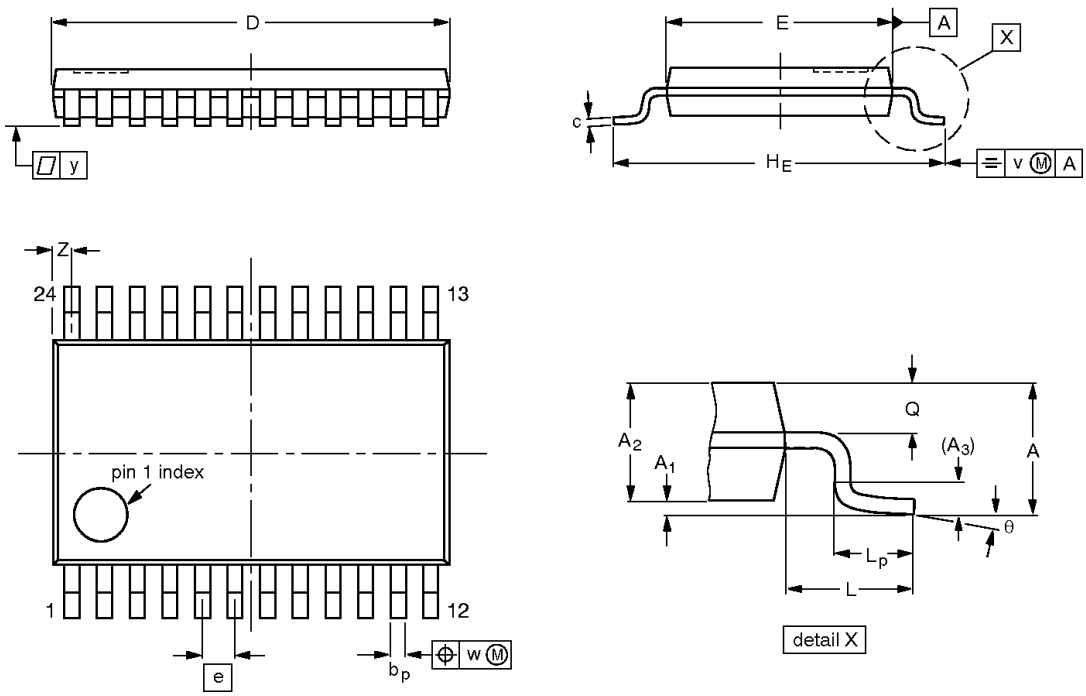
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

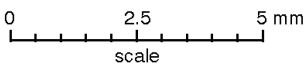
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

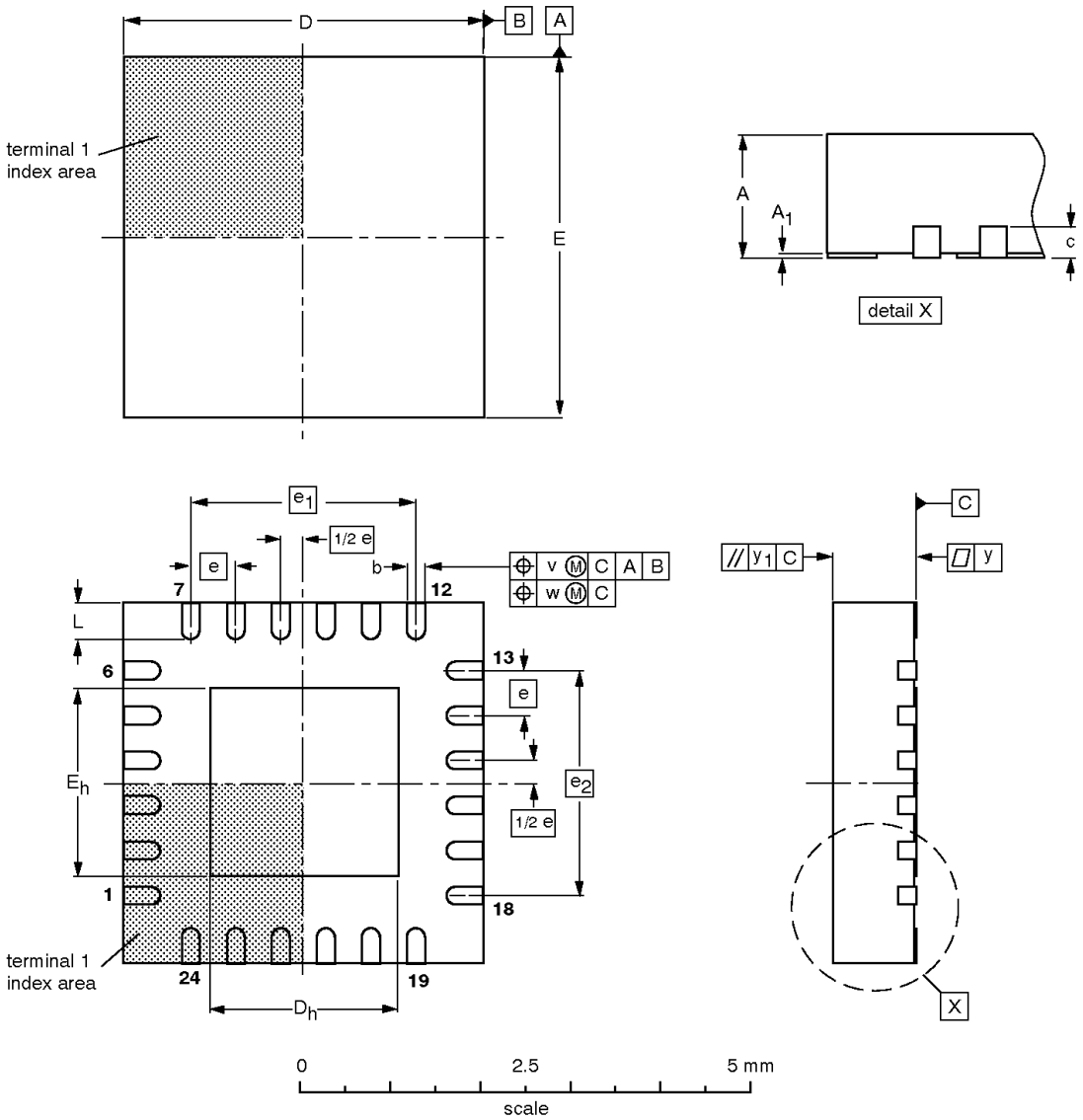
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

REVISION HISTORY

Rev	Date	Description
_1	20030627	**Product data (9397 750 11681); ECN 853-2430 30019 dated 11 June 2003. Initial version**

16-bit I²C and SMBus, low power I/O port with interrupt PCA9535

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status[1]	Product status[2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 06-03

Document order number: 9397 750 11681

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Appendix B: Samtec Inc, FireFly™ Optical User Manual

B.1 Introduction

The following pages are a reprint of the Samtec Inc, FireFly™ Optical User Manual.

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FireFly™ Optical

User Manual

Revision D03 - January, 2014

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Patents

Patents: 8588562 and 858856. Additional Patents pending.

Table of Contents

List of Figures

Change History

Revision #	Reason	Author	Date
Draft 01	Working Draft	Kevin Burt	11/25/2013
Draft 02	Working Draft- Reformat	Kevin Burt	1/13/2014
Draft 03	Preliminary Document	Kevin Burt	02/02/2014

1 Introduction

1.1 *Product Features*

The FireFly™ Micro Flyover System is the first inside the box interconnect system that gives the designer a choice of using either micro footprint optical or copper interconnects to meet today's and future data rate requirements and future proofing the next generation. The FireFly™ system enables chip-to-chip, board-to-board and system-to-system connectivity at data rates up to 28Gb/s. Current cable versions offer 12 channels of 14Gb/s providing 168Gb/s total bandwidth.

By taking the data connections "off-board" with FireFly™ fly over cables, the signal integrity design is made significantly easier, and the electrical performance improved. Allowing data to fly over lossy board materials and other signal degrading components negates the need for the layout complexities that are required to design for high speed signalling/

Unlike existing optical engine-based solutions, thermal operating conditions are acknowledged and designed for by including an integral heat sink. The heat sink is available in several default designs to allow for air cooling or with cold plate liquid cooling. In addition, the flexible design accepts customer specific heat sinks for easy integration into existing thermal solutions.

Due to Samtec's extensive catalogue of connector solutions, the copper FireFly™ assembly is made even more powerful by allowing use of different connector types for the far end. This enables the seamless connection between new boards and existing products without forcing a redesign.

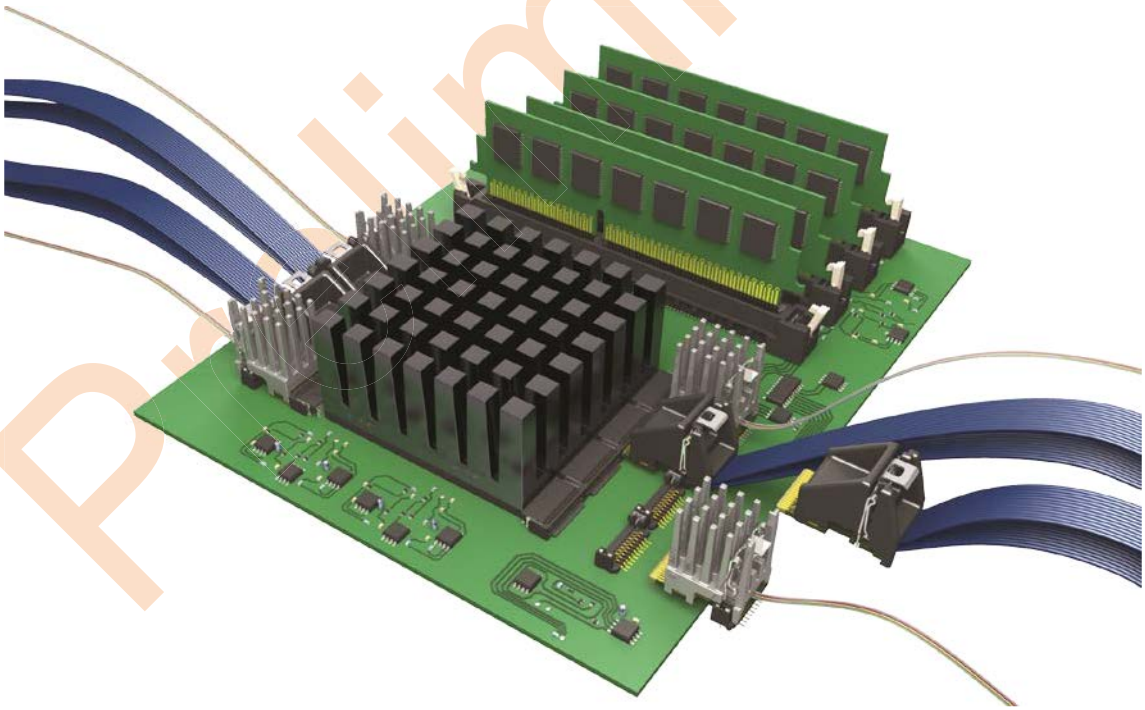


Figure 1: FireFly™ Application using Copper and Optical Assemblies

1.2 System Components

1.2.1 On Board Connector and Transceiver

The FireFly™ Connector system is a two part connector designed for applications up to 28 GB/s. It is based on two connectors, a micro high speed edge connector (UEC5, shown rear left) with two rows of 19 positions providing 12 differential lanes and a 10 position positive latch connector (UCC8, shown front right).

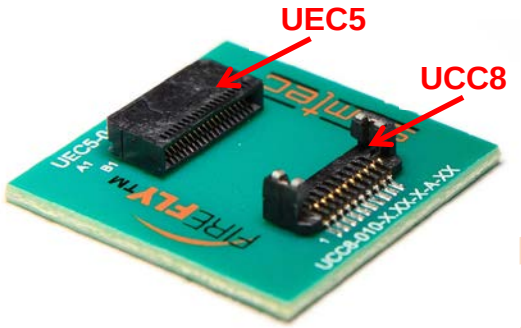


Figure 2: FireFly™ x12 Connector System

The UEC5 connector is used to connect the high speed data signals from the host system to the inputs of the optical or copper FireFly™ assemblies.

The UCC8 connector provides mechanical support in conjunction with a mechanical latch on the FireFly™ assembly. In addition, it provides power and low speed communications for optical assemblies.

The on-board connector system is designed for placement on a host board or directly on an IC package. In addition, it enables on-package applications due to the separation of the high speed signals and the power pins.

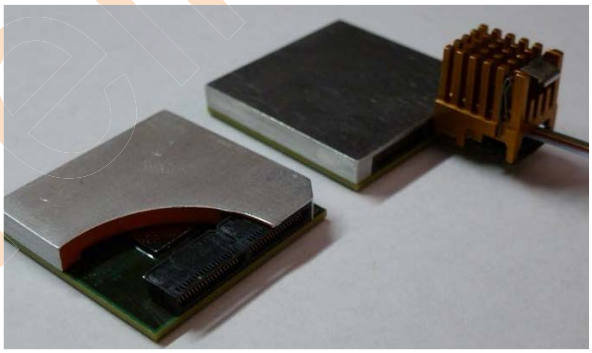


Figure 3: FireFly™ On Chip Example

For on package applications, the UEC5 connector is co-packaged with the IC and the UCC8 is placed on the board. Installing the connector onto the IC package enables the shortest possible trace length to maximize performance a high density interconnects. To accommodate the increased height of combined UEC5 connector and substrate, the UCC8 can be configured in different heights.

Detailed Connector specifications can be found in Section 2.
On-board connector pin outs can be found in Section 6.1

1.2.2 Copper Cables

FireFly™ copper cables are available based on Samtec's 50Ω 38 AWG, Micro coax ribbon cable. This cable provides performance up to 28 Gb/s on twelve 100 Ω differential lanes and comes as standard with a FireFly™ connector on end two.

Figure 4: ECUE 12 Pair Copper Cable

In addition to the standard connector on the second end of the cable, the assembly can be customised with a wide variety of Samtec connectors. Please contact HDR@samtec.com for further information on cables built with any of the following as the second end:

- Edge Card,
- SEARAU™
- Q Rate®
- Q Series®
- Edge Rate™

For applications which require improved Signal Integrity or a lower profile, Samtec also offers FireFly™ cables based on our 100 Ω 30AWG, Accelerate™ Twinax Ribbon Cable.

Figure 5: Accelerate™ Twinax Ribbon FireFly Assembly

This cable will plug into the FireFly™ connector set, however it will result in a slightly larger keep out area due to the different cable construction and the use of a screw down retention system.

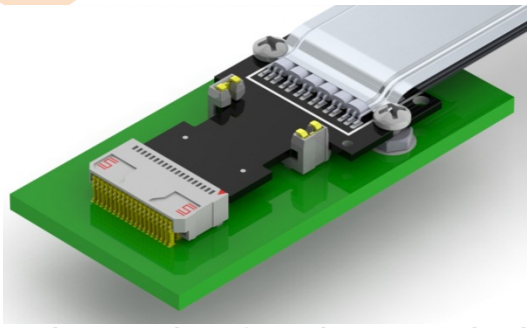


Figure 6: Close Up View of Accelerate Based Cable End

In addition to the lower profile and increased SI performance, the Accelerate™ based cable can be configured so that sideband signals can be carried via the UCC8 connections. Please contact HDR@samtec.com for further information.

1.3 *Optical Assemblies*

Optical Assemblies are available in three different configurations.

- Half Cable
- Active Optical Cable
- Y Cable

The same optical engines are used in each cable. As a result, the differences are with the assembly and not the optical engine form factor or performance. All engines are unidirectional, that is there are separate transmit and receive engines each with 12 channels either transmitting or receiving data. Bidirectional assemblies are supported by combining a transmit and receive engine into a single *Y cable* (see below)

Half Cables

Figure 7: Half Cable

Half cables are available with either a transmit or a receive optical engine joined to an optical connector with a 12-fiber optical cable.

These assemblies are customisable to different lengths and with different fiber types, different heat sinks and different optical connectors.

Active Optical Cables

Figure 8: Active Optical Cable

Active optical cables are available with a transmit optical engine on one end and a receive optical engine on the second end.

These assemblies can also be configured to different lengths and with different fiber types, different heat sinks and different optical connectors.

Y Cables

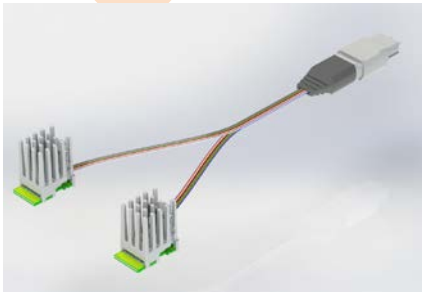


Figure 9: Y Cable

Y cables consist of both a transmit optical engine and a receive optical engine connected to a single 24 Fiber optical connector.

Again, these assemblies are customisable to different lengths (identical for transmit and receive) and with different fiber types, different heat sinks and different optical connectors.

1.3.1 Heat Sink Options

FireFly™ optical assemblies can be configured with a choice of standard heat sinks shown in Figure 10. These heat sink designs support air flow cooling and cold plate cooling. In addition, the FireFly™ design allows the use of custom heat sinks that allow the integration of cooling solutions for multiple components.

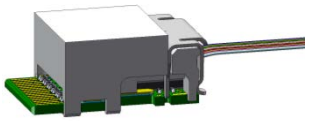
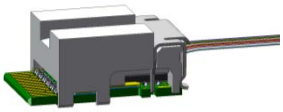
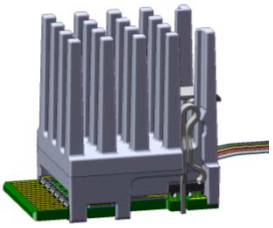
Cold Plate Solutions		Air Cooled Solution
		
Flat	Flat with 3-Ribbon Pass-Through	Pin-Fin

Figure 10: Standard Heatsinks

The *flat with 3-ribbon pass-through* heat sink is intended for ultra-high density applications. The angled recess in the heat sink is designed to accommodate the fibers from up to three other ECUO optical assemblies configured in stacked rows. This is shown in Figure 11 (only shown with 3 stacked rows and 2 fibers being passed through for simplicity).

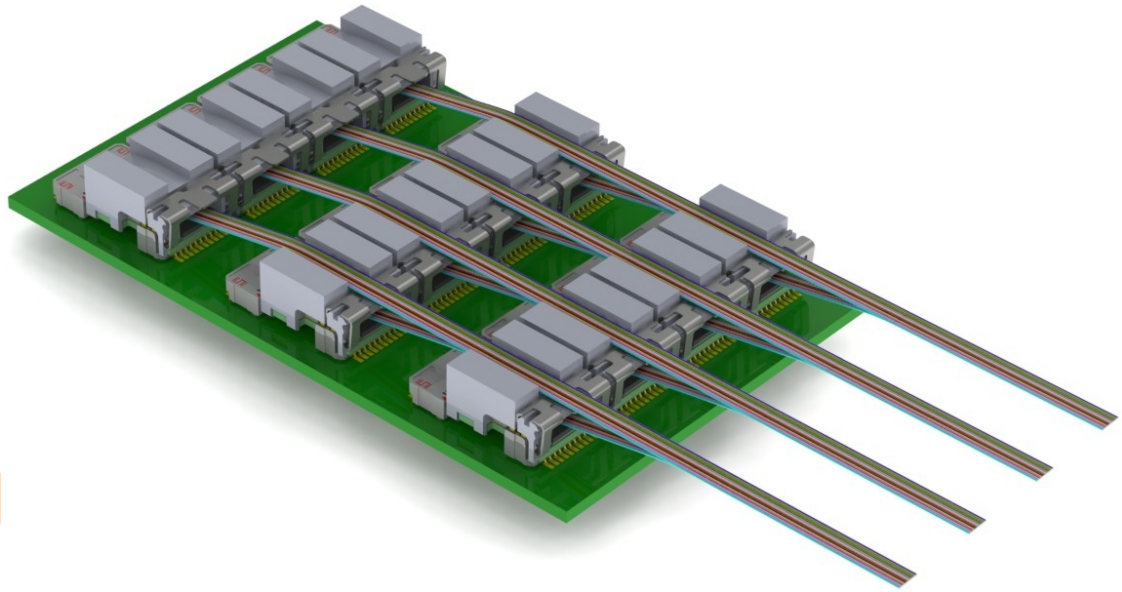


Figure 11: 4 x 3 Multi-Row FireFly™ Arrangement

In addition to the standard heat sinks listed, Samtec will work with customers to create heat sinks optimised for their specific designs[1]. For further information, please contact your local sales representative or firefly@samtec.com.

More information on Heatsinks can be found in Section 3.5.

[1] Minimum order quantity or NRE may be required

1.4 *Evaluation Kit*

To assist with the evaluation of the FireFly™ system, Samtec has created an evaluation kit. The FireFly™ evaluation kit is rated up to 25 Gb/s and is shown in Figure 12.

The FireFly™ evaluation kit consist of a break-out board connecting a FireFly™ socket (UEC5 and UCC8 connectors) to a 2x12 Bull's Eye™ connector landing pads and bringing low speed signals and power rails to various standard connectors.

A mating Samtec Bull's Eye connector with 24 cables terminated with SMA connectors allows for connecting all 12 channels to test equipment. A second Bull's Eye connector landing pad provides standard open and thru circuits to enable de-embedding of the Bull's Eye and PCB affects on the high speed signals.

The kit includes the following items:

- 1 each FireFly™ PCB break-out board
- 1 each Bull's Eye x24 block and 2x nuts
- 2 each Bull's Eye x12 ground insert
- 24 each Bull's Eye to SMA cable
- 1 each Bull's Eye cable removal tool
- 1 each Aardvark USB to I2C dongle and USB cable
- 1 each USB memory stick with Aardvark driver, FireFly™ Optical Engine client interface, FireFly™ Optical Engine user manual

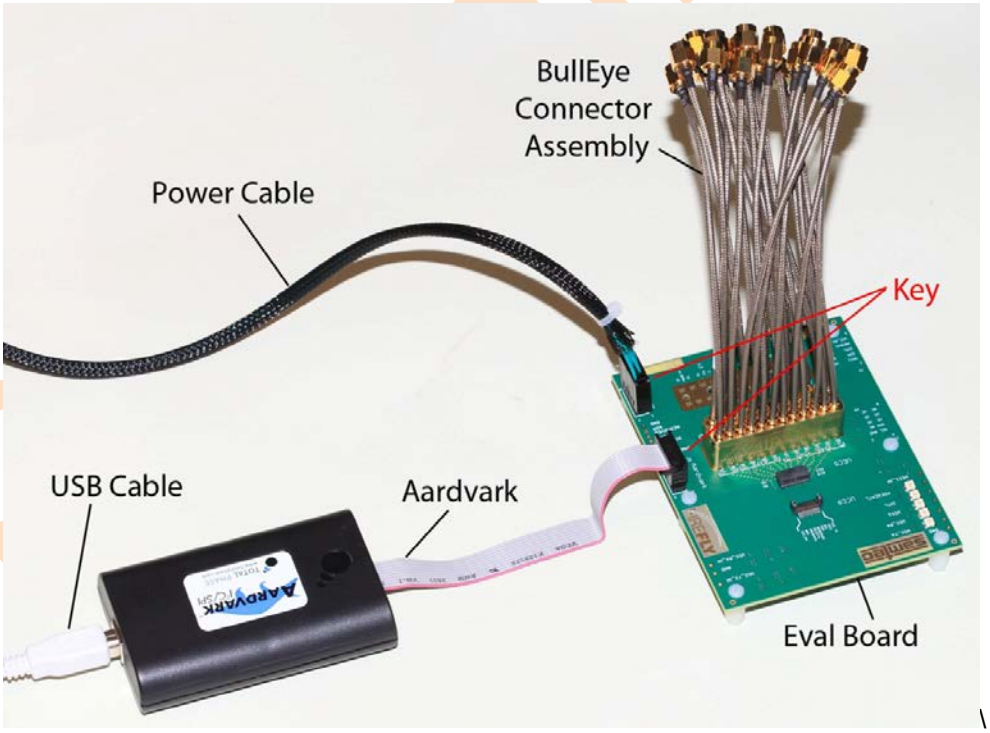


Figure 12: FireFly™ Evaluation Kit

The part number to purchase the evaluation kit is FIK-FIREFLY-01.

1.5 *Functional Description*

1.5.1 ECUO-T12 Transmitter

The ECUE-T12 optical assembly incorporates a 12-channel VCSEL array, a 12-channel laser driver, diagnostic monitors, control and bias blocks. The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 Ω. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board.

An LVTTL compatible Two-Wire Serial (or I_2C) interface is provided for module control and diagnostics. Status, alarm and fault information are available via the TWS interface. To reduce the need for polling, a hardware interrupt signal is provided to inform hosts of an assertion of an alarm, and Transmitter (Tx) fault.

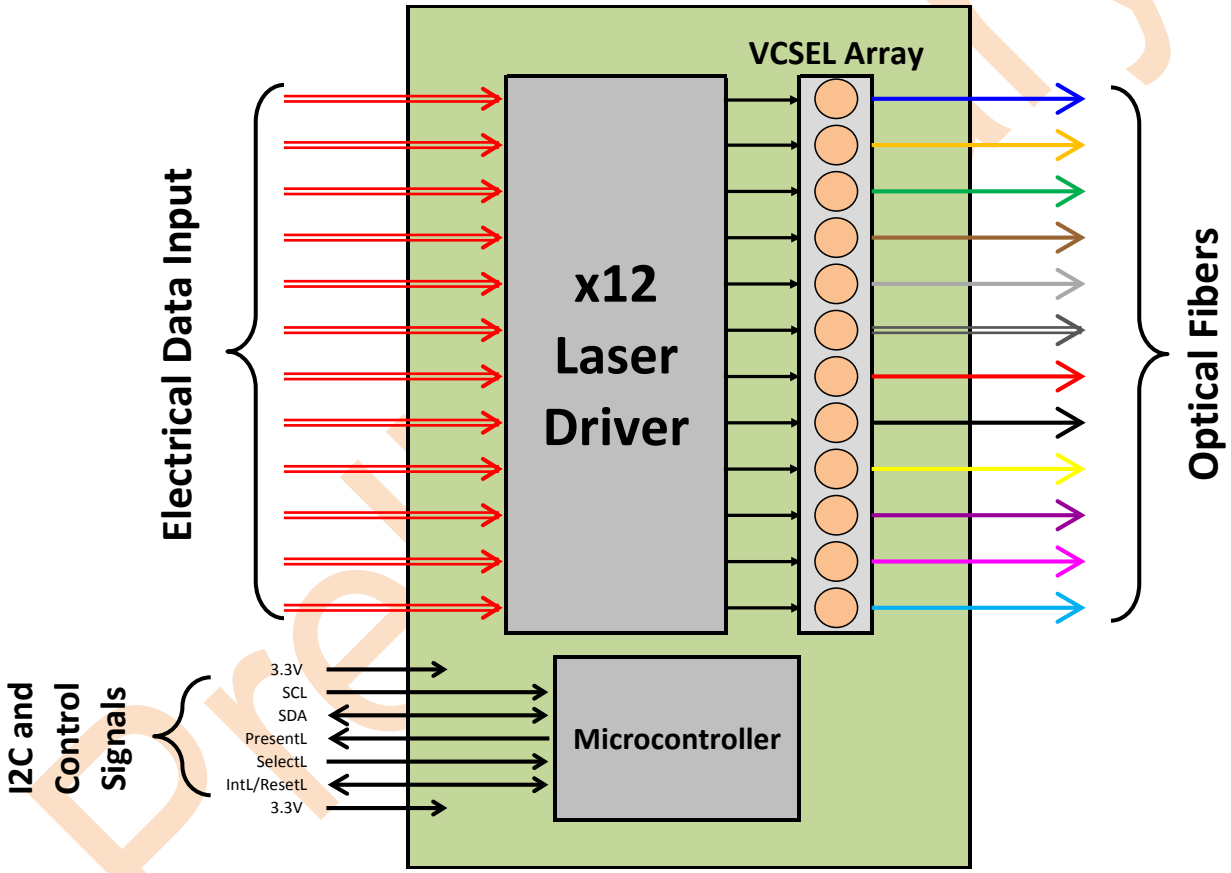


Figure 13: ECUO-T12 Block Diagram

1.5.2 ECUO-R12 Receiver

The ECUE-R12 optical assembly incorporates a 12-channel PIN photodiode array, a 12-channel TIA array, diagnostic monitors, control, and bias blocks. The Receiver Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ω to AC ground and 100 Ω differentially. Again, AC coupling capacitors are located on the optical engine and are therefore not required on the host board.

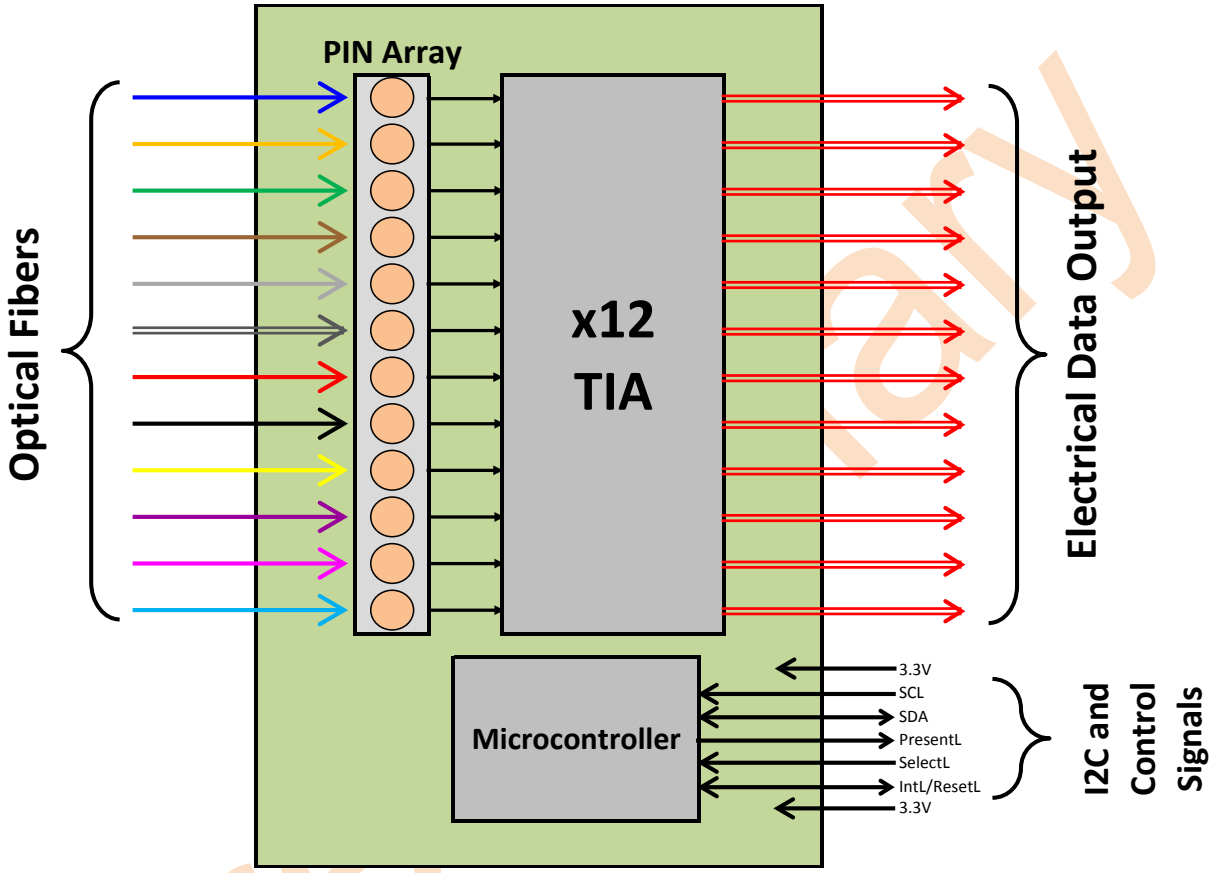


Figure 14: ECUO-R12 Block Diagram

1.6 *Management Interface*

Each optical engine has an I2C based management interface that is based on that defined for the CXP cables in the specification, *Infiniband™ Architecture Specification Volume 2, Release 1.3*. The specified memory map has been:

- Modified to separate Tx and Rx functionality
- Modified to use of Module Select Pin to allow multiple engines on the bus
- Simplified to reflect product features
- Expanded to provide additional features

This management interface provides digital diagnostics and control/monitor functional control to the host system. The on board microcontroller monitors and reports this information via the I2C interface.

The following module and channel digital diagnostic parameters are monitored:

- Temperature
- Supply Voltage

The microcontroller will generate an Interrupt Flag, by pulsing low the IntL signal, when an operational fault occurs. The host can identify the source of the interrupt by reading the appropriate registers through the I2C interface. The following Interrupt Flags are provided:

Transmitter

- **Tx Fault**
  - Provided for each channel, indicating that a fault condition relating to that specific laser modulators has occurred
- **High Temperature**
  - Heat sink temperature has exceeded maximum allowed temperature
- **Low Temperature**
  - Heat sink temperature has dropped below minimum allowed temperature
- **High Vcc**
  - Supply voltage has exceeded maximum allowed voltage
- **Low Vcc**
  - Supply voltage has dropped below allowed voltage

Receiver

- **Rx LOS**
  - Provided for each channel, indicating that the optical power input into the receiver has dropped below a minimum allowed value
- **High Temperature**
  - Heat sink temperature has exceeded maximum allowed temperature
- **Low Temperature**
  - Heat sink temperature has dropped below minimum allowed temperature
- **High Vcc**
  - Supply voltage has exceeded maximum allowed voltage
- **Low Vcc**
  - Supply voltage has dropped below allowed voltage

More Information on the management interface can be found in Section 0

2 On- Board Connector Specifications

2.1 *Drawings and 3D Models*

Three Dimensional models and product prints for the UEC5 and UCC8 connectors showing dimensions, footprint and options will be available at:

http://www.samtec.com/cable-systems/active-optics/on-board-optical/firefly.aspx.

Prior to general release, please contact optics@samtec.com for the most up to date versions.

2.2 *Connector Footprints*

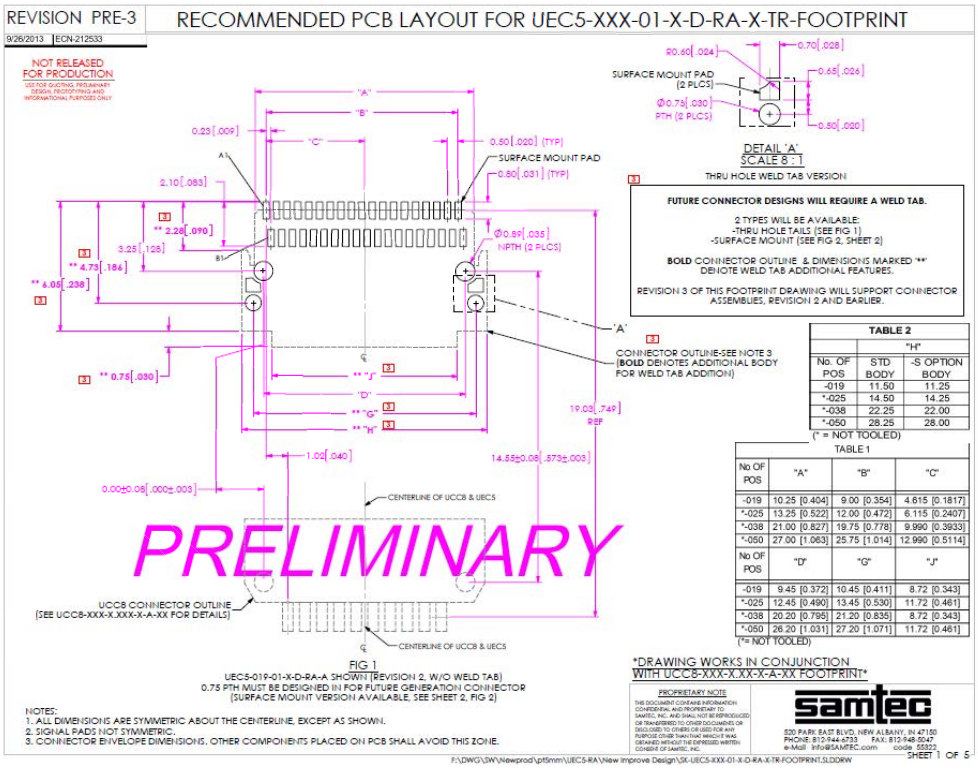
Detailed Connector Footprint information is available for the FireFly™ connectors and will be available at:

http://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=UEC5 for the UEC5 and

http://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=UCC8 for the UCC8

Prior to general release, please contact optics@samtec.com for the most up to date versions of these files.

UEC5



REVISION PRE-3 | RECOMMENDED PCB LAYOUT FOR UEC5-XXX-01-X-D-RA-X-TR-FOOTPRINT

PRELIMINARY

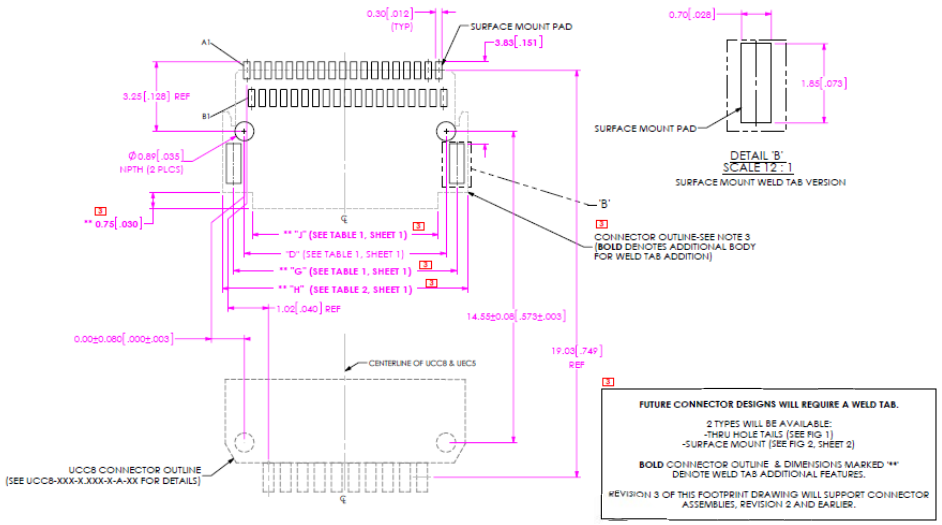


FIG 2
UEC5, 19 POSITION WITH SURFACE MOUNT WELD TAB SHOWN
0.70 x 1.85 SMT PAD MUST BE DESIGNED IN FOR FUTURE GENERATION CONNECTOR
(THRU-HOLE VERSION AVAILABLE, SEE SHEET 1, FIG 1)
(SAME AS FIG 1, EXCEPT AS SHOWN)

FUTURE CONNECTOR DESIGNS WILL REQUIRE A WELD TAB.

2 TYPES WILL BE AVAILABLE:
-THRU HOLE TAILS (SEE FIG 1)
-SURFACE MOUNT (SEE FIG 2, SHEET 2)

BOLD CONNECTOR OUTLINE & DIMENSIONS MARKED '**' DENOTE WELD TAB ADDITIONAL FEATURES.

#REVISION 3 OF THIS FOOTPRINT DRAWING WILL SUPPORT CONNECTOR ASSEMBLIES, REVISION 2 AND EARLIER.

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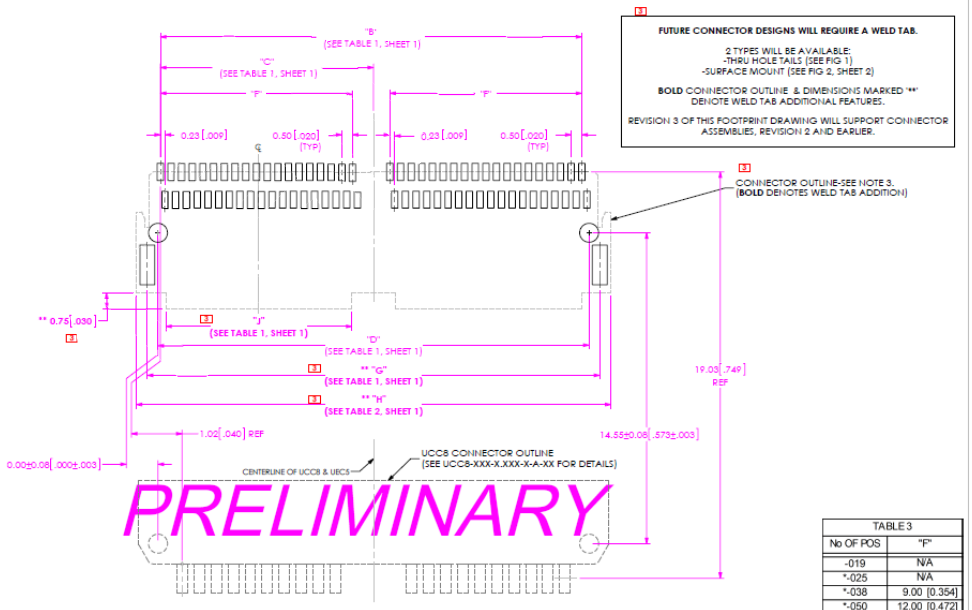
REVISION PRE-3 | RECOMMENDED PCB LAYOUT FOR UEC5-XXX-01-X-D-RA-X-TR-FOOTPRINT



PRELIMINARY

FUTURE CONNECTOR DESIGNS WILL REQUIRE A WELD TAB.

2 TYPES WILL BE AVAILABLE:
-THRU HOLE TAILS (SEE FIG 1)
-SURFACE MOUNT (SEE FIG 2, SHEET 2)

BOLD CONNECTOR OUTLINE & DIMENSIONS MARKED '**' DENOTE WELD TAB ADDITIONAL FEATURES.

REVISION 3 OF THIS FOOTPRINT DRAWING WILL SUPPORT CONNECTOR ASSEMBLIES, REVISION 2 AND EARLIER.

TABLE 3	
No OF POS	"F"
-019	N/A
*-025	N/A
*-038	9.00 [0.354]
*-050	12.00 [0.472]

(*= NOT TOOLED)

FIG 3
UEC5-038-01-X-D-RA-A SHOWN(REVISION 2, W/O WELD TAB)
0.70 x 1.85 SMT PAD MUST BE DESIGNED IN FOR FUTURE GENERATION CONNECTOR
(DIFFERENT AS SHOWN, OTHERWISE SAME AS FIGS 1 & 2)

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REVISION PRE-3 | RECOMMENDED STENCIL LAYOUT FOR UEC5-XXX-01-X-D-RA-X-TR-FOOTPRINT

NOTE:
STENCIL TO BE 0.13[.005] THICK.

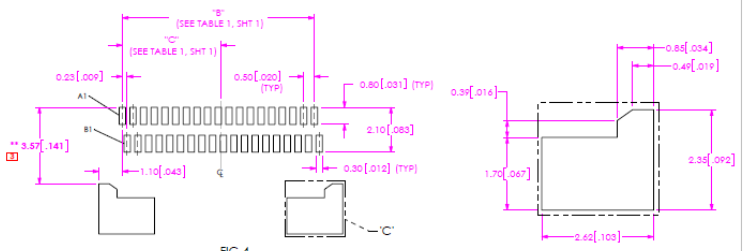

FIG 4
UEC5-019-01-X-D-RA-A (REVISION 2, W/O WELD TAB)
0.75 PTH MUST BE DESIGNED IN FOR FUTURE GENERATION CONNECTOR

DETAIL 'C'
SCALE 12 : 1
THRU HOLE WELD TAB VERSION

PRELIMINARY

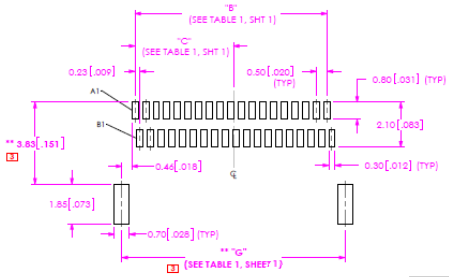

FIG 5
0.70 x 1.85 SMT PADS MUST BE DESIGNED IN FOR FUTURE GENERATION CONNECTOR

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REVISION PRE-3 | RECOMMENDED STENCIL LAYOUT FOR UEC5-XXX-01-X-D-RA-X-TR-FOOTPRINT

NOTE:
STENCIL TO BE 0.13[.005] THICK.

PRELIMINARY

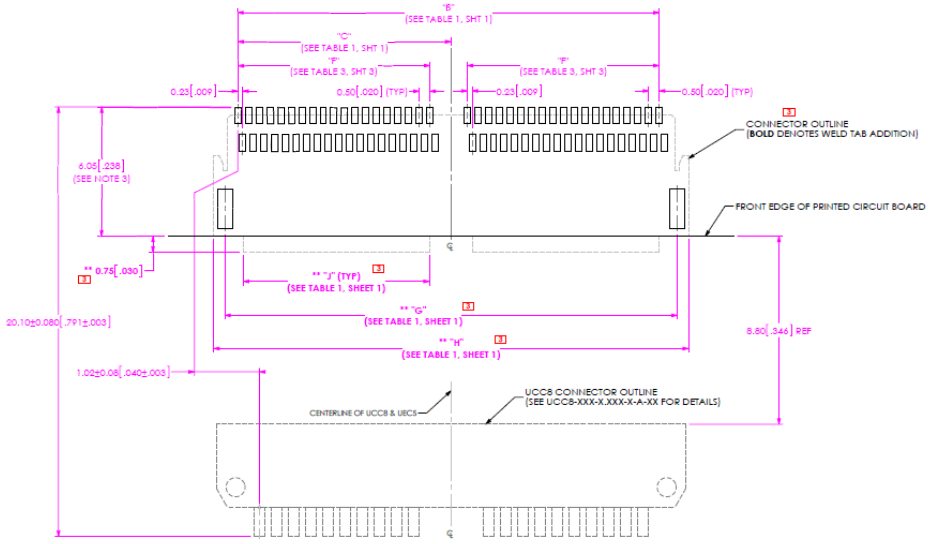

FIG 6
UEC5-038-01-X-D-RA-A SHOWN(REVISION 2, W/O WELD TAB)
0.70 x 1.85 SMT PAD MUST BE DESIGNED IN FOR FUTURE GENERATION CONNECTOR
(DIFFERENT AS SHOWN, OTHERWISE SAME AS FIGS 4 & 5)

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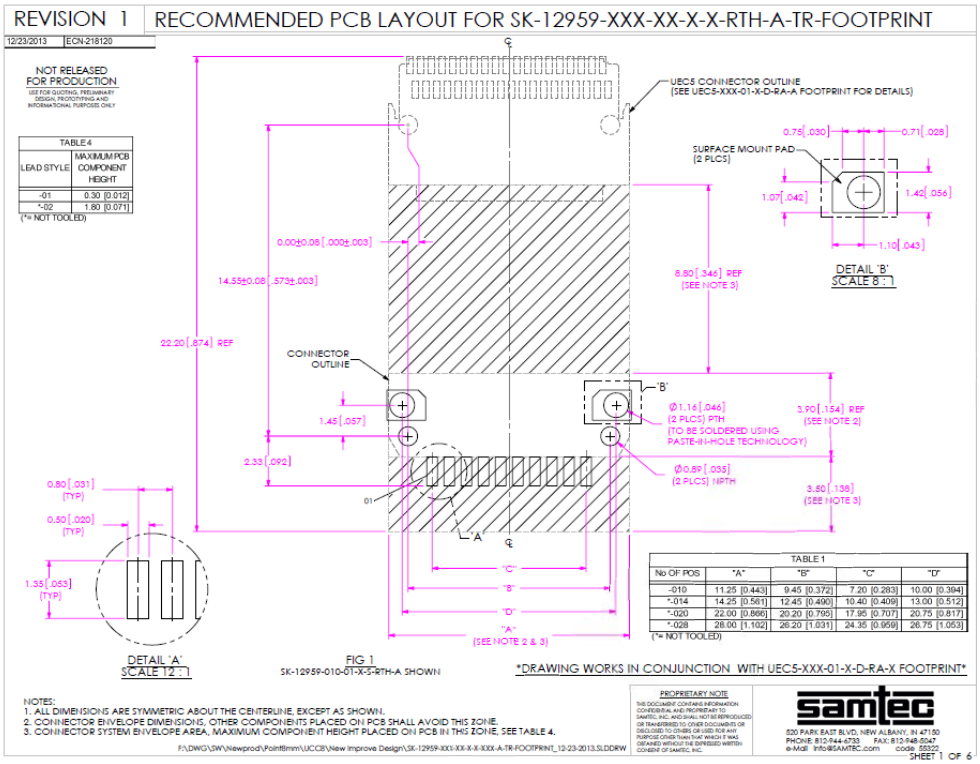
REVISION 1
RECOMMENDED PCB LAYOUT FOR SK-12959-XXX-XX-X-X-RTH-A-TR-FOOTPRINT
12/23/2013
ECN-218120
NOT RELEASED FOR PRODUCTION
USE FOR QUOTING, PRELIMINARY DESIGN, PROTOTYPING AND INFORMATIONAL PURPOSES ONLY
TABLE 4
LEAD STYLE
MAXIMUM PCB COMPONENT HEIGHT
-01
0.30 [0.012]
*-02
1.80 [0.071]
(*= NOT TOOLED)
UEC5 CONNECTOR OUTLINE
(SEE UEC5-XXX-01-X-D-RA-A FOOTPRINT FOR DETAILS)
SURFACE MOUNT PAD
(2 PLCS)
0.75[.030]
0.71[.028]
1.07[.042]
1.42[.056]
1.10[.043]
DETAIL 'B'
SCALE 8 : 1
0.00±0.08 [.000±.003]
14.55±0.08 [.573±.003]
8.80 [.346] REF
(SEE NOTE 3)
22.20 [.874] REF
CONNECTOR OUTLINE
'B'
Ø1.16 [.046]
(2 PLCS) PTH
(TO BE SOLDERED USING PASTE-IN-HOLE TECHNOLOGY)
3.90 [.154] REF
(SEE NOTE 2)
1.45 [.057]
2.33 [.092]
Ø0.89 [.035]
(2 PLCS) NPTH
3.50 [.138]
(SEE NOTE 3)
0.80 [.031]
(TYP)
0.50 [.020]
(TYP)
1.35 [.053]
(TYP)
'A'
"C"
"B"
"D"
"A"
(SEE NOTE 2 & 3)
TABLE 1
No OF POS
"A"
"B"
"C"
"D"
-010
11.25 [0.443]
9.45 [0.372]
7.20 [0.283]
10.00 [0.394]
*-014
14.25 [0.561]
12.45 [0.490]
10.40 [0.409]
13.00 [0.512]
*-020
22.00 [0.866]
20.20 [0.795]
17.95 [0.707]
20.75 [0.817]
*-028
28.00 [1.102]
26.20 [1.031]
24.35 [0.959]
26.75 [1.053]
(*= NOT TOOLED)
DETAIL 'A'
SCALE 12 : 1
FIG 1
SK-12959-010-01-X-5-RTH-A SHOWN
DRAWING WORKS IN CONJUNCTION WITH UEC5-XXX-01-X-D-RA-X FOOTPRINT
NOTES:
1. ALL DIMENSIONS ARE SYMMETRIC ABOUT THE CENTERLINE, EXCEPT AS SHOWN.
2. CONNECTOR ENVELOPE DIMENSIONS, OTHER COMPONENTS PLACED ON PCB SHALL AVOID THIS ZONE.
3. CONNECTOR SYSTEM ENVELOPE AREA, MAXIMUM COMPONENT HEIGHT PLACED ON PCB IN THIS ZONE, SEE TABLE 4.
F:\DWG\SW\Newprod\Point8mm\UCC8\New Improve Design\SK-12959-XXX-XX-X-X-XXX-A-TR-FOOTPRINT_12-23-2013.SLDDRW
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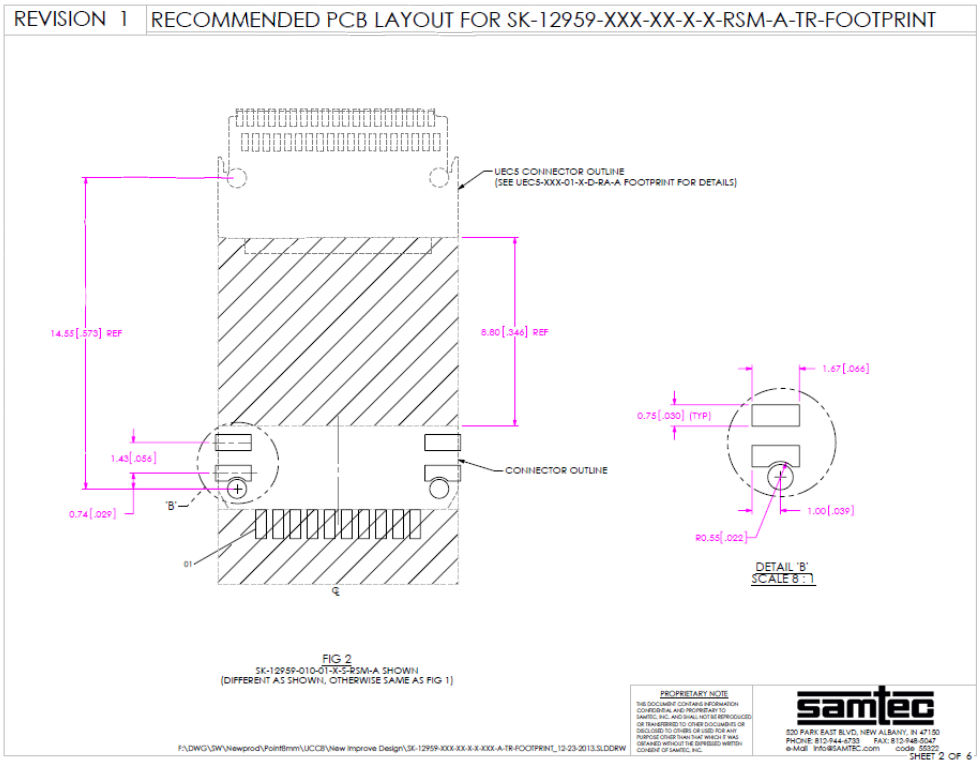
SHEET 1 OF 6


REVISION 1
RECOMMENDED PCB LAYOUT FOR SK-12959-XXX-XX-X-X-RSM-A-TR-FOOTPRINT
UEC5 CONNECTOR OUTLINE
(SEE UEC5-XXX-01-X-D-RA-A FOOTPRINT FOR DETAILS)
14.55[.573] REF
8.80[.346] REF
1.67[.066]
0.75[.030] (TYP)
1.43[.056]
CONNECTOR OUTLINE
0.74[.029]
'B'
1.00[.039]
R0.55[.022]
DETAIL 'B'
SCALE 8 : 1
FIG 2
SK-12959-010-01-X-5-RSM-A SHOWN
(DIFFERENT AS SHOWN, OTHERWISE SAME AS FIG 1)
F:\DWG\SW\Newprod\Point8mm\UCC8\New Improve Design\SK-12959-XXX-XX-X-X-XXX-A-TR-FOOTPRINT_12-23-2013.SLDDRW
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SHEET 2 OF 6

REVISION 1 | RECOMMENDED PCB LAYOUT FOR SK-12959-XXX-XX-X-X-RTH-A-TR-FOOTPRINT

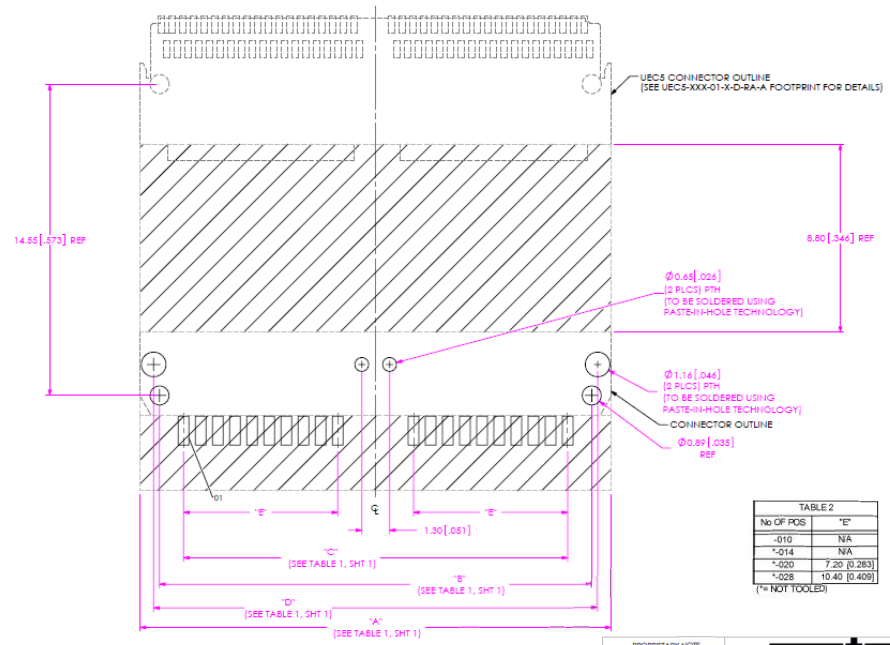

TABLE 2	
No OF POS	"E"
-010	N/A
*-014	N/A
*-020	7.20 [0.283]
*-028	10.40 [0.409]

(* = NOT TOOLED)

FIG 3
SK-12959-020-01-X-5-RTH-A SHOWN
(DIFFERENT AS SHOWN, OTHERWISE SAME AS FIG 1)
(NOT TOOLED)

F:\DWG\SW\Newprod\Point8mm\UCC8\New Improve Design\SK-12959-XXX-XX-X-X-XXX-A-TR-FOOTPRINT_12-23-2013.SLDDRW

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SHEET 3 OF 6

REVISION 1 | RECOMMENDED PCB LAYOUT FOR SK-12959-XXX-02-X-X-RTH-A-TR FOOTPRINT

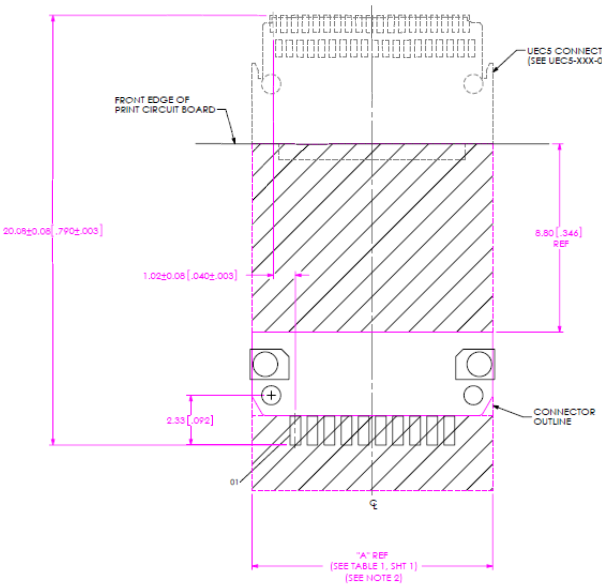

FIG 4
SK-12959-010-02-X-5-RTH-A SHOWN
(DIFFERENT AS SHOWN, OTHERWISE SAME AS FIG 1)
(NOT TOOLED)

F:\DWG\SW\Newprod\Point8mm\UCC8\New Improve Design\SK-12959-XXX-XX-X-X-XXX-A-TR-FOOTPRINT_12-23-2013.SLDDRW

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SHEET 4 OF 6

REVISION 1 | RECOMMENDED STENCIL LAYOUT FOR SK-12959-XXX-XX-X-X-XXX-A-TR-FOOTPRINT

NOTE:
STENCIL TO BE 0.15[.006] THICK.

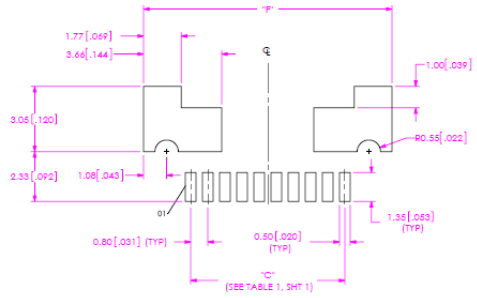

FIG 5
SK-12959-010-XX-X-5-RTH-A STENCIL SHOWN

TABLE 3		
No OF POS	"F"	"G"
-010	11.61 [0.457]	11.45 [0.451]
*-014	14.61 [0.575]	14.45 [0.569]
*-020	22.36 [0.880]	22.20 [0.874]
*-028	28.36 [1.117]	28.20 [1.110]

(*= NOT TOOLED)

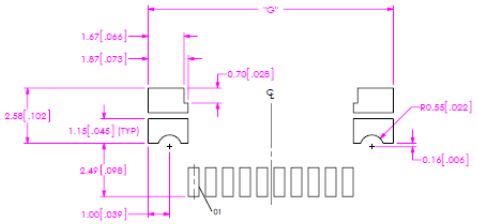

FIG 6
SK-12959-010-XX-X-5-R5M-A STENCIL SHOWN
(DIFFERENT AS SHOWN, OTHERWISE SAME AS FIG 5)

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F:\DWG\SW\Newprod\Point8mm\UCCB\New Improve Design\SK-12959-XXX-XX-X-X-XXX-A-TR-FOOTPRINT_12-23-2013.SLDDRW

SHEET 5 OF 6

REVISION 1 | RECOMMENDED STENCIL LAYOUT FOR SK-12959-XXX-XX-X-X-XXX-A-TR-FOOTPRINT

NOTE:
STENCIL TO BE 0.15[.006] THICK.

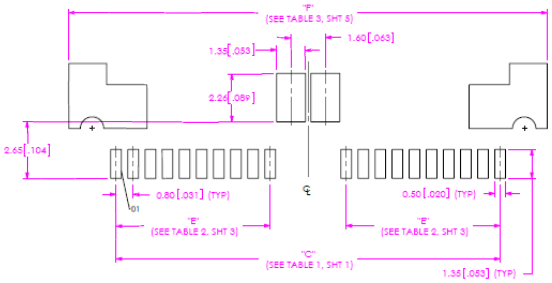

FIG 7
SK-12959-020-XX-X-5-RTH-A STENCIL SHOWN
(DIFFERENT AS SHOWN, OTHERWISE SAME AS FIG 5)
(NOT TOOLED)

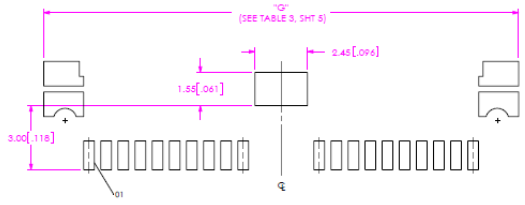

FIG 8
SK-12959-020-XX-X-5-R5M-A STENCIL SHOWN
(DIFFERENT AS SHOWN, OTHERWISE SAME AS FIG 6&7)
(NOT TOOLED)

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SHEET 6 OF 6

2.3 *On-Board Connector Layout*

Layout design breakout regions are available for the FireFly™ connector systems. These are intended to streamline the design process and are available on demand.

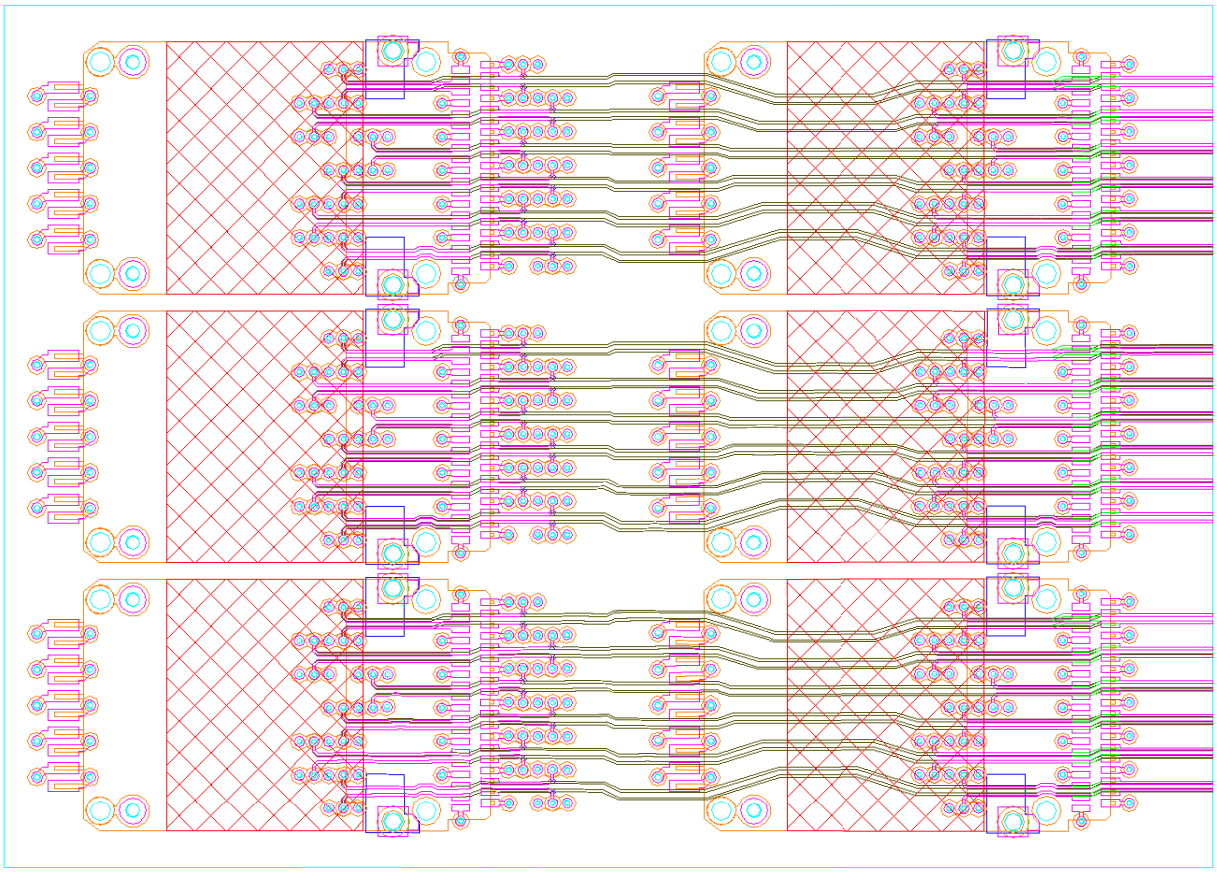


Figure 15: Breakout Region

Please contact SIG@samtec.com for further information.

2.4 *Performance*

The performance of the UEC5 was investigated using a full wave model of the UEC5 to an edge card as shown in Figure 16. Note, ports are 50Ω and de-embedding was not used as only a portion of the traces were retained on the test card.

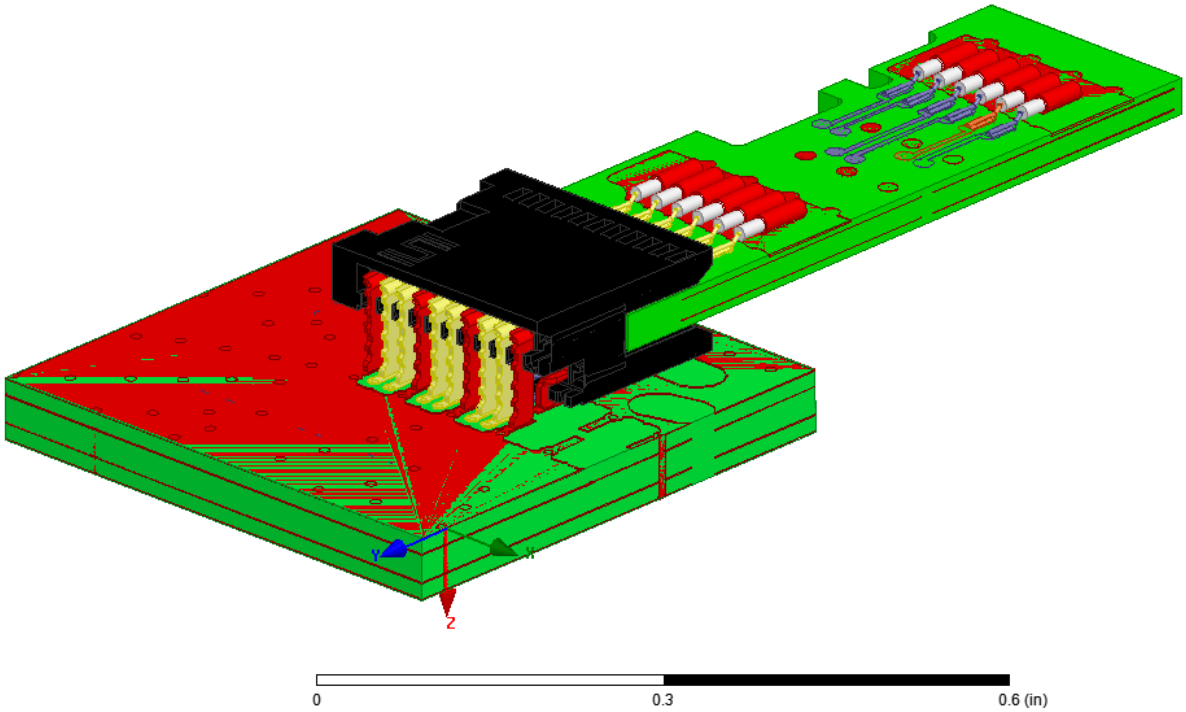


Figure 16: UEC5 Model

The port numbering for the simulation is shown in Figure 17. Note that Row B corresponds to the longer pins.

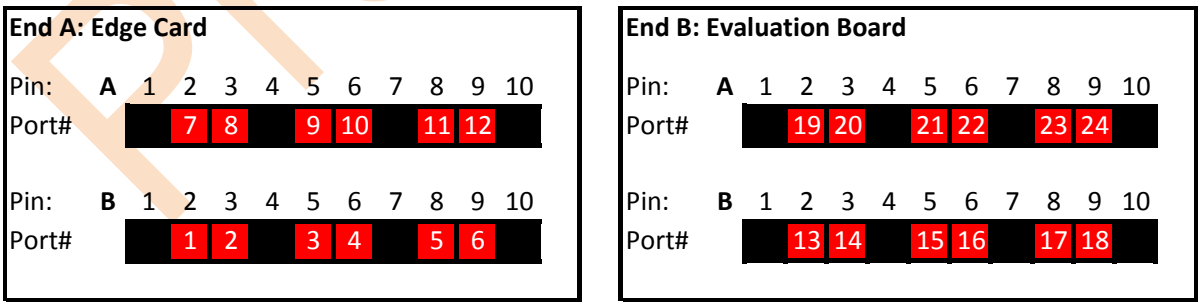


Figure 17: Port Numbering Diagram for Simulation

The simulation results are shown in Figure 18, Figure 19 and Figure 20.

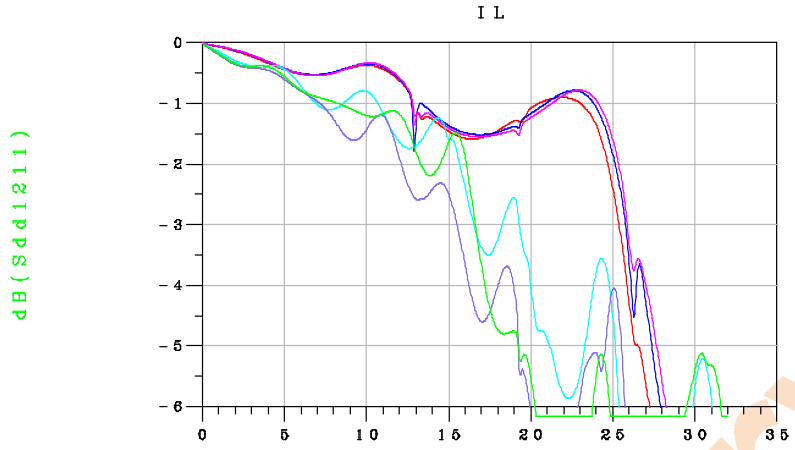


Figure 18: Differential Insertion Loss for Ports 1-12

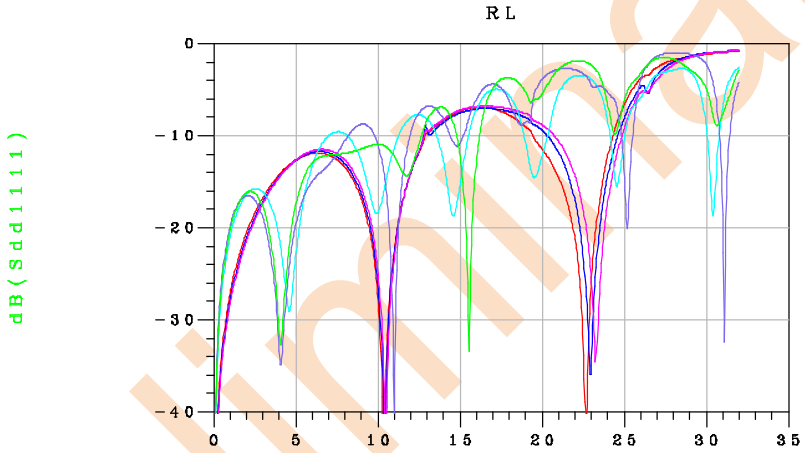


Figure 19: Differential Return Loss for Ports 1-12

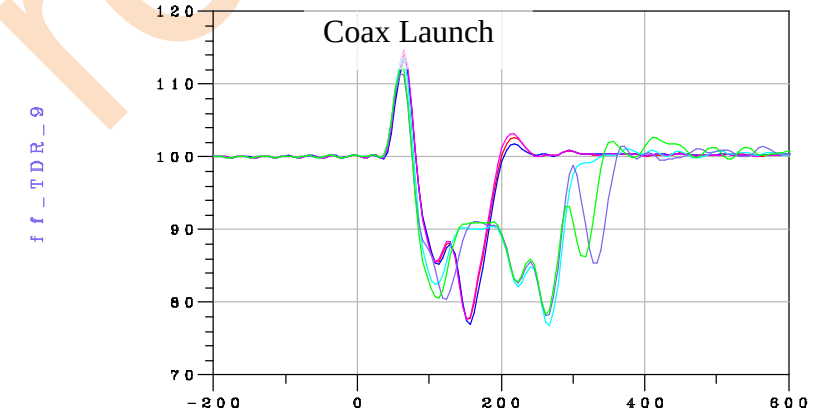


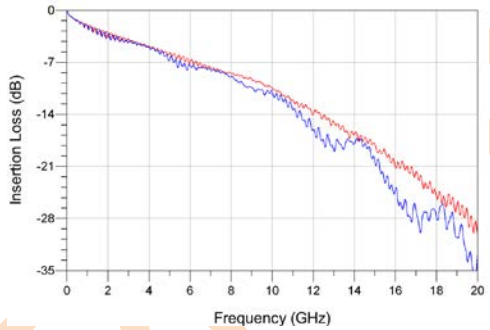
Figure 20: Differential Impedance for Ports 1-12

The performance of the UEC5 was characterised by measuring performance of the connector and a FireFly™ ECUE-12-050-01-01-01-01 cable (50cm, 38awg micro coax cable). These results are summarised in Table 1, Figure 21 and Figure 22. Further information regarding test methodology and results can be found at: http://www.samtec.com/Documents/WebFiles/testrpt/hsc-report_ECUE_web.pdf.

Parameter	Units	Min	Type	Max	Comments
3dB Bandwidth	GHz		5.5		Single Ended
-7dB Insertion Loss	GHz		5.9		Long Row
			5.2		Short Row
10dB Return Loss	GHz	10.9			Long Row
		4.5			Short Row
Near End Crosstalk	dB			-20	In Row-Long Row
				-20	In Row-Short Row
				-20	Xrow
				-20	Diagonal
Far End Crosstalk	GHz			-20	In Row-Long Row
				-20	In Row-Short Row
				-20	Xrow
				-20	Diagonal
Long/Short Delay Skew	Ps		12		Includes Cable Assembly

Table 1: High Speed Performance

Differential Application – Insertion Loss



Differential Application – Return Loss

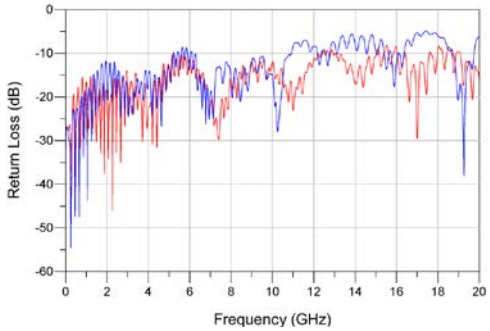
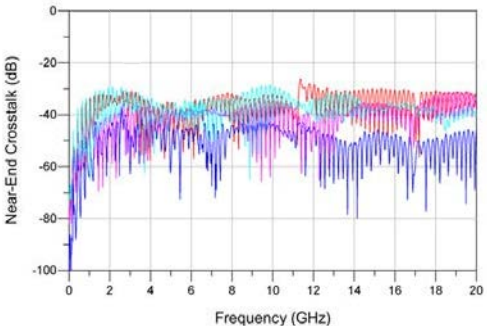


Figure 21: Differential S-parameter Performance

Differential Application - NEXT



Differential Application - FEXT

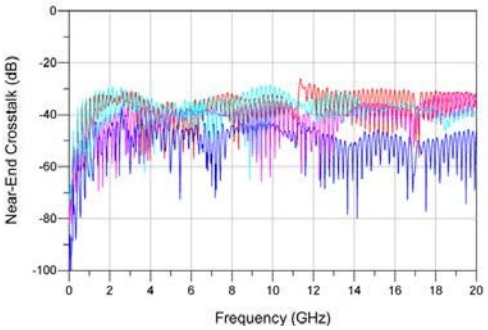


Figure 22: Crosstalk

2.5 *Electrical*

UEC5 Current Rating: 1.7A (1 pin powered, 30°C temperature rise, 20% de-rated)
UCC8 Current Rating: 2.6A (1 pin powered, 30°C temperature rise, 20% de-rated)
UEC5 Operating Voltage Range: 185 VAC
UEC5 Operating Voltage Range: 175 VAC

Requirement	Test Condition	Requirement	Status
Withstanding Voltage	EIA-364-20 (No Flashover, Sparkover, or Breakdown	525VAC	Pass
Insulation Resistance	EIA-364-21 (1000 MΩ minimum)	1,000 MΩ	Pass
Contact Resistance (LLCR)	EIA-364-23	Δ 15 mΩ maximum (Samtec Defined) / No Damage	Pass

Table 2: Electrical Specifications

2.6 *Environmental*

Operating Temperature Range: -55 °C to 125 °C

Requirement	Test Condition	Goal	Status
Thermal Shock	EIA-364-32 Thermal Cycles: 100 (30 minute dwell) Hot Temperature: +85 °C Cold Temperature: -55°C Hot/Cold Transition: Immediate	Visual Inspection: No Damage LLCR: Δ 15m Ω DWV: 720 AC IR: 10,000 M Ω	Pass
Thermal Aging	EIA-364-17 Test Condition 4 @ 105°C Condition B for 250 hours	Visual Inspection: No Damage LLCR: Δ 15m Ω DWV: 720 AC IR: 10,000 M Ω	Not Complete
Cyclic Humidity	EIA-364-31 Test Temp: 25°C to +65°C Relative Humidity: 90 to 95% Test Duration: 240 hours	Visual Inspection: No Damage LLCR: Δ 15m Ω DWV: 720 AC IR: 10,000 M Ω	Pass
Gas Tight	EIA-364-36 Gas Exposure: Nitric Acid Vapour Duration: 60 min Drying Temperature: 50°C ± 3°C Measurements: Within 1 hour of exposure	LLCR: Δ 15m Ω	Pass

Table 3: Environmental Specifications

2.7 Mechanical

Parameter	Units	Min	Typ	Max	Comments
Withdrawal Force	N				Results due mid Jan 2014
Insertion Force	N		9.0		Results due mid Jan 2014
Compression Down Force	N		30[1]		Vertical force through a cable assembly and the connector system

Table 4: Mechanical Forces

Requirement	Test Condition	Requirements	Status
Durability	EIA-364-09C	25 cycles	Pass
Contact Normal Force	EIA-364-04	30 grams minimum for gold interface	Pass

Table 5: Mechanical Specifications

2.8 Processing Recommendations

The following processing rules are recommended for optimal performance of the FireFly™ System:

- **Maximum Reflow Passes:** The parts can withstand three reflow passes at a maximum oven temperature of 260°C.
- **Stencil Thickness:** The stencil thickness is 0.13mm (.005")
- **Placement:** Machine placement of the parts is strongly recommended
- **Thermal Profile:** Due to the large number of processing variables (printed wiring board design, reflow oven type, component quantity, solder paste type, etc.), Samtec does not provide specific reflow profiles for any connector. We recommend that the solder paste manufacturer's guidelines be followed for optimum soldering results.
- **Reflow Environment:** Samtec recommends the use of a low level oxygen environment (typically achieved through a nitrogen gas infusion) in the reflow process to improve solderability.
- **ROHS Compliant:** The UEC5 and UCC8 connectors are suitable for ROHS compliant processes

2.9 Additional Resources

For additional mechanical testing or product information, contact our Customer Engineering Support Group at CES@samtec.com

For additional information on high speed performance testing, contact our Signal Integrity Group at SIG@samtec.com

For additional Processing information, contact our Interconnect Processing Group at IPG@samtec.com

For ROHS, REACH or other environmental compliance information, contact our Product Environmental Compliance Group at PEC@samtec.com

[1] Product tested successfully with 30N Down Force. Additional testing planned to investigate increased force in late Q1 2014.

3 Optical Assembly Specifications

3.1 *Power*

The ECUO-X12 requires a 3.3V supply voltage supplied to pins 1 and 10 of the low speed/power connections on the base of the board as shown in Figure 42 and Table 72. The power supply specifications are listed in Table 6.

Parameter	Unit	Min	Nom	Max	Notes
Vcc Supply	V	3.15	3.3	3.45	
Power Supply Noise	mV			50	On all power supply pins
Inrush Current	A			TBD	Duration < 50µs, spread evenly between both power pins
Current Ramp rate	mA/µs			100	
Steady State Current	A			0.7	spread evenly between power pins

Table 6: Low Speed and Power Specifications

The power filtering circuit shown in Figure 23 or am equivalent should be used to power ECUO-X12 optical assemblies.

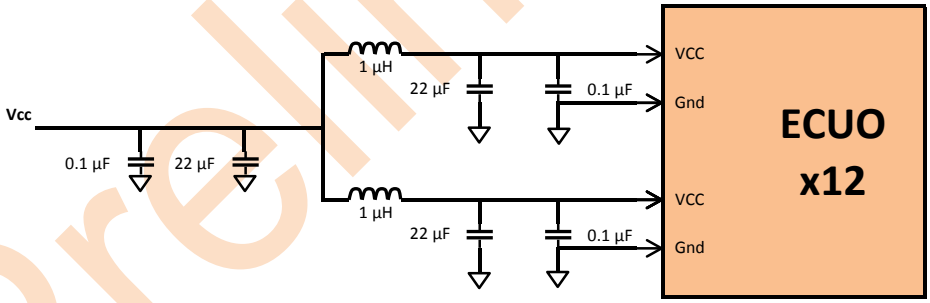


Figure 23: Recommended Power Filtering Circuit

No power sequencing of power supplies is required. The optical assemblies are not hot pluggable and should be fully installed in the connectors before power is applied. An internal brown out monitor enables a link to be established only after the 3.3V power supply is stable and above 3.15V.[1]

[1] Brown out functionality is disabled in V1.5 FireFly™ optical engines

3.2 *High Speed Performance*

FireFly™ reference compliance points for performance evaluation are defined in Table 7.

Compliance Point	Label
Host Output at UEC5 Connector	TP1
Transmitter Electrical Input	TP1’
Transmitter Optical Output	TP2
Receiver Optical Input	TP3
Receiver Electrical Output	TP4’
Host Input at UEC5 Connector	TP4

Table 7: Reference Compliance Points

A simplified version of this (omitting the evaluation and the evaluation cable) is shown in Figure 24.

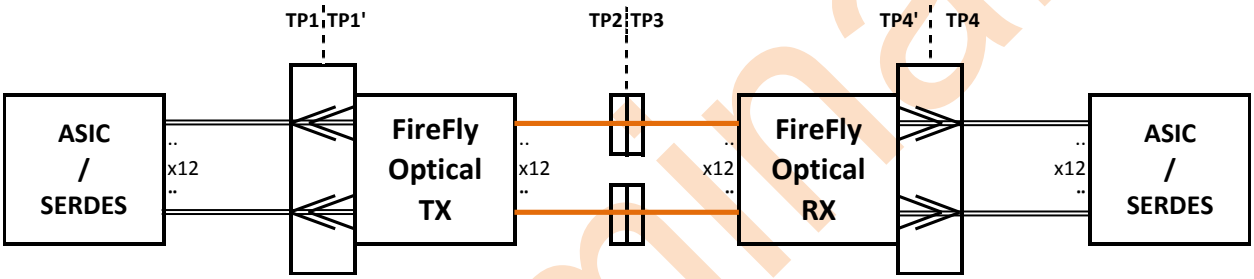


Figure 24: FireFly™ Compliance Test Points

All specified parameters are measured with either a FireFly™ Evaluation Board (See Section 1.4) or the FireFly™ Evaluation Cable (Contact optics@samtec.com for further information). This is described in Table 8.

Compliance Point	Definition	Measurement Fixture
TP1	TBD	Cable
TP1’	Section 3.2.1	Board
TP2	Section 3.2.2	Board
TP3	Section 3.2.3	Board
TP4’	Section 3.2.4	Board
TP4	TBD	Cable

Table 8: Compliance Point Specification and Fixture

The reference impedance for differential measurements and S-parameters is 100 Ω and the reference impedance for common mode measurements and S-parameters is 25 Ω.

3.2.1 Compliance Point TP1' - Transmitter Electrical Input

The electrical requirements for the input signal for an ECUO-T12 optical assembly are defined in Table 9.

Specifications	Symbol	Unit	Min	Max	Notes
Data Rate per Channel		Gb/s	1	14.1	
Differential Input Amplitude	V_{DI}	mV	250	1600	Peak to peak differential
Single-ended Voltage		V	-0.3	3.8	
AC Common Mode Voltage		mV		15	RMS
Differential Return Loss	S_{DD}	dB	See Note 1		50 MHz to 14.1 GHz
Common Mode Return Loss	S_{CC}	dB		-2	50 MHz to 14.1 GHz
Common Mode to Differential Return Loss	S_{DC}	dB	See Note 2		50 MHz to 14.1 GHz
Reflected Differential to Common Mode Return Loss	S_{CD}	dB		-10	50 MHz to 14.1 GHz
Total Jitter	TJ	UI_{p-p}		0.28	
Data Dependent Jitter	DDJ	UI_{p-p}		0.1	
Data Dependent Pulse width Shrinkage	DDPWS	UI_{p-p}		0.11	
J2 Jitter Tolerance	J2	UI	0.19		
J9 Jitter Tolerance	J9	UI	0.37		
Eye Mask			See Note 3		Hit ratio = 5 x 10^{-5}

Table 9: TP1'- Transmitter Electrical Input

Notes for Table 9:

1. Maximum S_{DD} is defined by the formula:

   0.05 < f <5.6 $\quad -12 + 1.71\sqrt{f}$

   5.6 ≤ f < 14.1 $\quad -6.7 + 13\log_{10}\left(\frac{f}{7}\right)$

2. Maximum S_{DC} is defined by the formula:

   0.05 < f <5.6 $\quad -16 + \frac{2}{3}f$

3. The worst case eye is shown in Figure 25

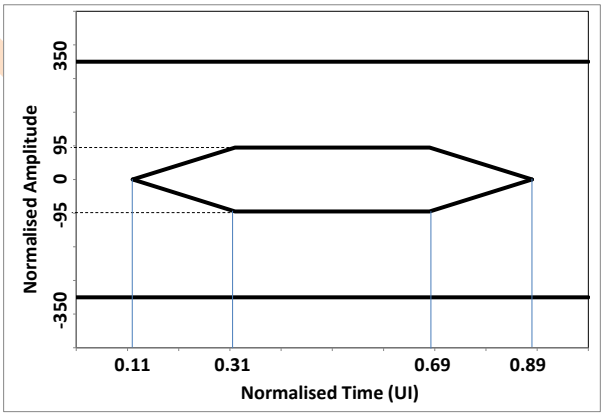


Figure 25: Transmit Electrical Input Eye Mask

3.2.2 Compliance Point TP2 - Transmitter Optical Output

When an electrical signal compliant with that defined in Section 0 is provided to the input of the transmitter, the resulting optical output will be compliant with the performance listed in Table 10.

Specifications	Symbol	Unit	Min	Max	Notes
Center Wavelength	λ	nm	840	860	
Supported Link length (OM3)		M	0.5	100	See Note 1
Supported Link length (OM4)		M		150	
RMS spectral width		nm		0.65	Standard deviation of the spectrum
RIN OMA		dB/Hz		-128	
Encircled Flux		%		86 30	At 19 µm At 4.5 µm
Average Launch Power per Lane	P_{Ave}	dBm	-5.0	-1.2	
Power delta between all lanes		dB		4	
Average power of an off transmitter		dBm		-3	
Extinction Ratio	ER	dB	3		
Return Loss		dB	12		
Eye Mask			See Note 2		

Table 10: TP2- Transmitter Optical Output Specifications

Notes for Table 10:

1. Total link length including Tx and Rx pigtails and external patch cords between them with a total connector loss of < 2dB
2. Worst case optical eye is defined by the mask shown in Figure 26:

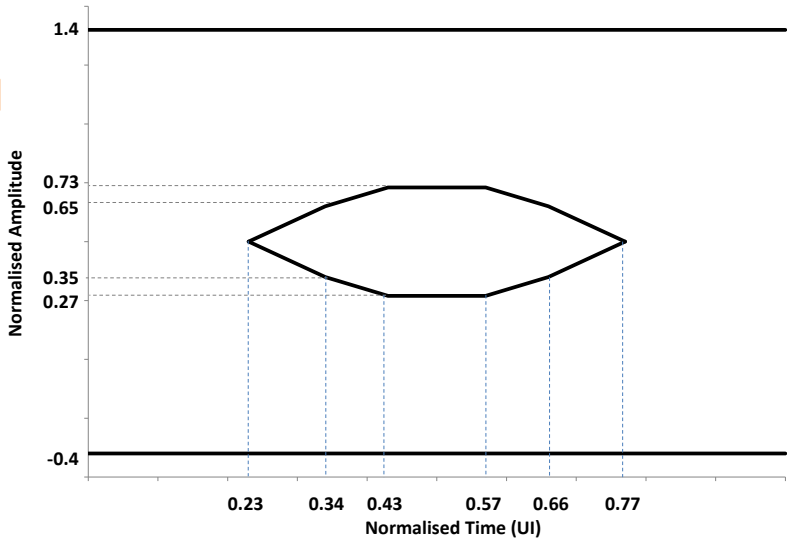


Figure 26: Transmit Output Optical Eye

3.2.3 Compliance Point TP3- Receiver Optical Input

The worst case optical signal tolerated by the ECUO-R12 optical receiver is listed in Table 11.

Specifications	Symbol	Unit	Min	Max	Notes
Center Wavelength	λ	nm	840	860	
Supported Link length (OM3)		M	0.5	100	Note 1
Supported Link length (OM4)		M		150	
Average Optical Power	AOP	dBm	-9.9	2.4	
Sensitivity (OMA)				-11.1	BER ≤ 10^{-12}
Stressed Sensitivity (OMA)		dBm		-5.4	BER ≤ 10^{-12} Note 2
Jitter Tolerance in OMA		dBm		-5.6	
Return Loss	ORL	dB	12		
Peak Power		dBm		4	Per lane

Table 11: TP3 - Receiver Optical Input Specifications

Notes for Table 10:

1. Total link length including Tx and Rx pigtails and external patch cords between them with a total connector loss of < 2dB
2. The input stressed eye is as defined by IEEE 802.3bm:

Vertical Eye Closure penalty (each lane)	3.6dB
J2 Jitter	0.41 UI
J4 Jitter	0.55 UI
OMA	3 dBm

   Worst case optical eye is defined by the mask shown in Figure 27
3. The jitter tolerance conditions are defined by IEEE 802.3bm:

Jitter peak-to-peak amplitude$_1$ and frequency$_1$	5 UI @ 190 kHz
Jitter peak-to-peak amplitude$_2$ and frequency$_2$	1 UI @ 940 kHz
OMA of each aggressor lane	3 dBm

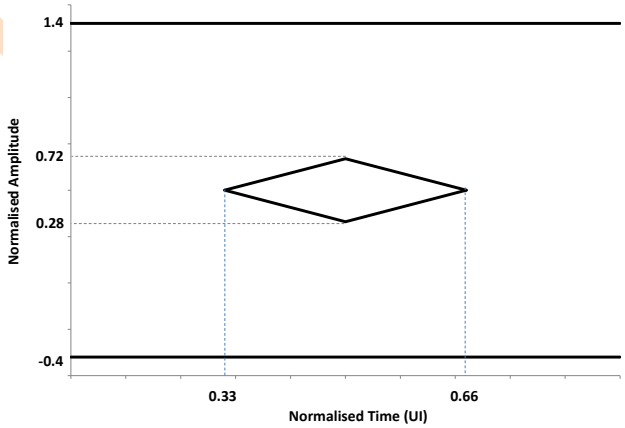


Figure 27: Stressed Receiver Sensitivity Input Eye Mask

3.2.4 Compliance Point TP4'- Receiver Electrical Output

An ECUO-R12 receiver with an input signal compliant to that defined in Section 3.2.3will output a signal as defined in Table 12.

Specifications	Symbol	Unit	Min	Max	Notes
Data Rate per Channel		Gb/s	1	14.1	
Termination Mismatch at 1 MHz	ΔZ_m	%		15	
Differential Output Amplitude in Squelched State		mV		50	Peak to peak differential
Common Mode Return Loss	S_{CC22}	dB	See Note 1		50 MHz to 14.1 GHz
Differential Mode Return Loss	S_{DD22}	dB	See Note 2		50 MHz to 14.1 GHz
Common Mode to Differential Return Loss	S_{DC22}	dB	See Note 3		50 MHz to 14.1 GHz
Output Transition Time	Tr, Tf	Ps	17		20% to 80%
Total Jitter	TJ	UI_{p-p}		0.7	
J2 Jitter	J2	UI		0.44	
J9 Jitter	J9	UI		0.69	
Eye Mask			See Note 4		

Table 12: TP4' Receiver Electrical Output Specifications

Notes for Table 12:

1. Maximum S_{CC22} is defined by the formula:

   0.05 < f < 4.11 $\quad -12 + 2\sqrt{f}$

   4.11 ≤ f < 11.1 $\quad -6.3 + 13\log_{10}\left(\frac{f}{5.5}\right)$

   11.1 ≤ f < 14.1 $\quad$ -2

2. Maximum S_{DD22} is defined by the formula:

   0.05 < f <5.6 $\quad -12 + 1.71\sqrt{f}$

   5.6 ≤ f < 14.1 $\quad -6.7 + 13\log_{10}\left(\frac{f}{7}\right)$

3. Maximum S_{DC11} is defined by the formula:

   0.05 < f <5.6 $\quad -16 + \frac{2}{3}f$

4. The output voltage swing and the de-emphasis of the electrical output are configurable by the user (see Section 0). As a result, an eye mask is not defined.

3.3 Latency

The per end latency (excluding fiber contribution) is shown in Table 13

Specifications	Unit	Min	Typ	Max	Notes
Transmitter latency	ps		70	100	
Receiver latency	ps		100	150	

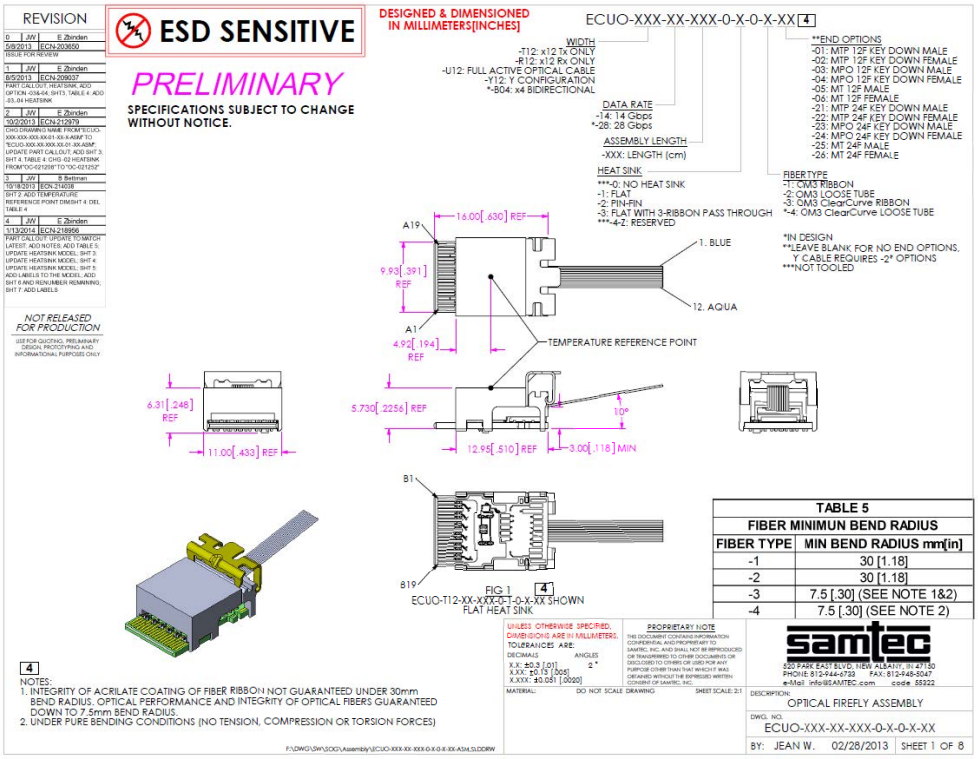
Table 13: Latency

3.4 *ECUO- Mechanical*

Three Dimensional models and product prints for the ECUO-X12 assemblies showing dimensions, and options will be available at:

http://www.samtec.com/cable-systems/active-optics/on-board-optical/firefly.aspx.

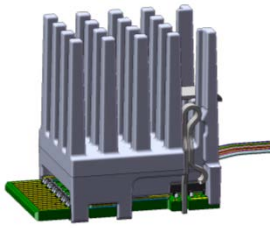
Prior to general release, please contact optics@samtec.com for the most up to date versions.



3.5 *Heat Sinks*

The FireFly™ optical assembly design includes an integral heatsink that is factory installed for optimum thermal performance. The transmit and receive assemblies can be ordered with one of three standard heat sinks (described below) that support air cooling and cold plate cooling. In addition, the design allows the use of custom heat sinks optimised for specific customer applications. Samtec will work with customers to create these optimised heat sinks.

Air Cooling



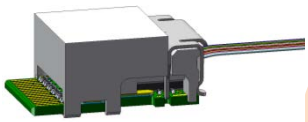
-2 = Pin-Fin

Requires a minimum air flow of 200LFM at a maximum ambient air temperature of 55°C to meet the specifications listed in Section 3.

Increased air flow rate will reduce assembly operating temperature as shown in

Airflow (LFM)	300	400	500
Operating Temperature Reduction (°C)	3	5	6

Cold Plate Cooling



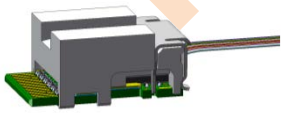
-1 = Flat

Requires the use of a thermally conductive elastomer (such as FujiPoly®) between the heatsink and cold plate

Maximum compression force for cold plate attachment = 30N

-3 = Flat with 3-ribbon pass through

Designed for use in ultra-high density applications. The recess in the top of the heat sink is optimised to accommodate the ribbon fibers from up to three other ECUO optical assemblies without impeding the cold plate contact. An example of this configuration is shown in Figure 11.



Requires the use of a thermally conductive elastomer (such as FujiPoly®) between the heatsink and cold plate

Maximum compression force for cold plate attachment = 30N

3.6 Optical Terminations

3.6.1 Introduction

The optical connector options available for the ECUO optical assembly are shown in Table 14.

Option	Connector
-01	MTP® 12F Key Down Male
-02	MTP® 12F Key Down Female
-03	MPO 12F Key Down Male
-04	MPO 12F Key Down Female
-05	MT 12F Male
-06	MT 12F Female
-21	MTP® 24F Key Down Male
-22	MTP® 24F Key Down Female
-23	MPO 24F Key Down Male
-24	MPO 24F Key Down Female
-25	MT 24F Male
-26	MT 24F Female

Table 14: Optical Connector Options for the ECUO Optical Assembly

All of these connectors are all based on the MT (Mechanical Transfer) ferrule. These were originally developed by NTT in 1985 as a multi fiber connector. These connectors have a rectangular end face and are generally made from polyphenylene sulphide (a glass filled polymer). Polished fibers protrude slightly (~2 µm) from the end face and are arranged in rows of 12 to create a connector with 12 or 24 fibers. Each fiber in the row of 12 is separated from the next by 0.25 mm. A microscopic view of the connector end face showing the polymer material and the connectors is shown in Figure 28.

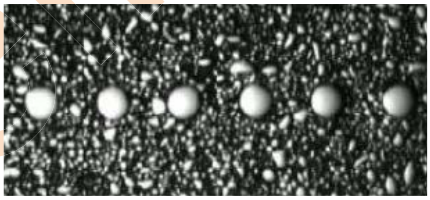


Figure 28: Microscopic view of a MT Ferrule End Face

The rectangular end face also includes precision alignment holes. These are used in association with guide pins to enable the accurate alignment of the fibers when two ferrules are connected together. Connectors using the alignment pins are gendered male and those without female. A close up of a 12 Fiber and a 24 Fiber female MT ferrule is shown in Figure 29

Figure 29: 12F and 24F Female MT Ferrule Connectors

To provide a low insertion loss, low return loss connection when connected, the male and female MT ferrules need to be held together so that the fibers physically contact their opposing pair. To achieve this, a metal clip with spring connections is used. This is shown in Figure 30.

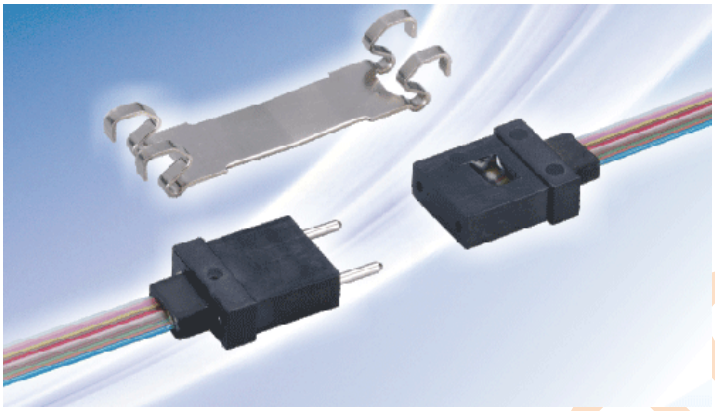


Figure 30: Male and Female MT Ferrules with Connecting Clip

MT Ferrule Connectors are generally used for inside the box applications. Connecting to a bulkhead requires a different type of connector called MPO (Multiple-fiber Push On). An example of an MPO series connector is shown in Figure 31.

Figure 31: MPO Connector

The MPO Connector adds an additional housing around the MT ferrule. This housing provides keying to help with the correct orientation. This is shown in Figure 32.

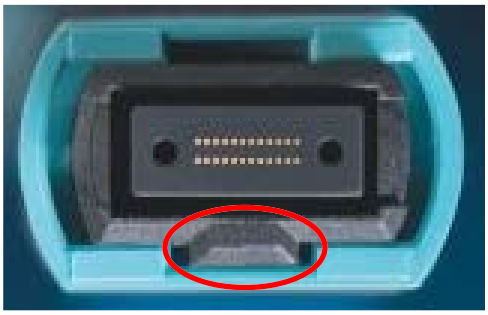


Figure 32: 24F MPO Connector with Keying Feature Highlighted

This key is used as a reference to number the fibers and can be oriented “key up” or “key down”. Note Samtec ECUO optical assemblies are only offered with key down orientation. This does not affect performance or connectivity.

The Samtec fiber numbering convention is:

- With the key down, start with the top right hand fiber and number this 1
- Count sequentially from right to left
- If there is a second row, move down to second row and continue counting at the right hand fiber.
- Again, count sequentially form right to left.

Examples for a 12F and 24F connector are shown in Figure 33.

Figure 33: Fiber Numbering Convention for 12F and 24F Connectors

Finally, the MTP® is a high performance version of the MPO connector made by US Conec. It offers several enhancements over the MPO connector:

- Ability to rework and re-polish the MT ferrule
- Change the gender after assembly or in the field
- Ferrule float which allows mated connectors to maintain physical contact while under an increased load.
- The use of elliptical guide pin tips reduces guide hole wear which increases the number of mate/demate cycles

MPO/MTP connectors are mated by using a connector adaptor. An example is shown in Figure 34. Note that these are available in different alignments. These are discussed in Section 9.

Figure 34: Example of an MPO/MTP Adaptor

3.6.2 MT Prizm

US Conec will be releasing a new MT Ferrule variant, called the *MT Prizm* (shown in Figure 35) in early 2014. This will be dimensionally the same as the standard MT ferrule, but will not require a physical contact of each fiber tip with its pair from the second connector for a low loss connection. Instead, micro lenses are situated in a recess of each tip that collimates an exiting signal or captures an incoming signal.

Figure 35: MT Prizm Ferrule

This will provide the following performance benefits:

- A reduction in spring force required to hold two connectors together.
- Improved optical return loss
- Improved dirt/debris immunity

In addition, the connector will hermaphroditic removing the uncertainty of the keying and key alignment, but is otherwise compatible with the MPO and MTP connector housing platforms.

Due to the uncertainty of the form factor for the release (possibly 4 rows of 16 fibers), Samtec is not committing to a pin out at this time, however is committed to supplying this connector option.

3.6.3 MT / MPO / MTP Performance

The specifications for MT ferrule and MPO and MTP connectors are listed in Table 15

Specifications	Unit	Min	Max
Insertion Loss			0.75
Back Reflection	dB		20
Number of Insertions		500	

Table 15: MT, MPO and MTP Specifications

3.6.4 Connector Cleaning

It is important to always clean and inspect connectors prior to connection due to the physical contact between the fibers. Dirt can prevent the fibers from contacting correctly (resulting in increased loss), block the light (increased loss) or physically damage the fiber (scratches or pits). All of these can result in increased loss and performance degradation with the optical links. Several companies have instructions for inspecting and cleaning multimode connectors available on the web. One example is provided by Panduit Corp at www.panduit.com/heiler/InstallInstructions/PN446.pdf.

3.6.5 Fiber

FireFly™ optical assemblies are available with different types of fiber. These can provide advantages when trying to route the fiber inside the box due to the form factor (loosed tubed fibers will bend in all axis unlike the ribbon fiber) and minimum bend radius (see Table 16).

Option	Description	Min Bend radius[1] (mm)
-01	OM3 Ribbon	30
-02	OM3 Loose Tube	30
-03	OM3 ClearCurve™ Ribbon	7.5[2]

Table 16: Fiber Options

Strain Relief

Under Investigation

Specs

TBD

Assembly Length

Under Investigation. Please contact FireFly@samtec.com to discuss your requirements.

[1] Under pure bending conditions (i.e. no tension, compression or torsion forces)
[2] Integrity of acrylate coating of fiber ribbon not guaranteed under 30 mm bend radius. Optical performance and integrity of optical fibers guaranteed down to 7.5 mm bend radius.

4 Control and Memory Map

4.1 *Control*

A management interface is provided based on an industry standard two-wire serial interface scaled for 3.3 volt LVTTL. The specification has been modelled on the definition of the CXP multi-lane interface modified to fully separate transmitter and receiver functionality.

The specification provides separate addresses for the receive and transmit portions of the CXP module. The FireFly™ ECUO-X12 follows this and provides different addresses as shown in Table 17.

End	7 bit Address	8 bit address	
		Write	Read
Transmit	50h	A0h	A1h
Receive	54h	A8h	A9h

Table 17: I2C Addressing

Enhanced functionality, based on the QSFP management interface is provided to enable multiple devices to reside on the same bus through the use of a Mod_Select pin. This pin allows multiple FireFly™ optical assemblies to be on a standard I2C Serial control bus. By default, this pin is held low by the host. In this state, the module will respond to the I2C interface. When the ModSelL pin is pulled high by the host, the module will not respond to or acknowledge any I2C query or command.

Care must be taken to ensure that the ModSelL pin is used to toggle control of different modules, the assert and de-assert times must be taken into account to prevent communication conflicts.

4.1.1 Voltage and Timing Specification

Management Interface Voltage Specification

Management signalling logic levels are based on Low Voltage CMOS operating at 3.3V Vcc. The host should use a pull-up to Vcc3.3 for the two wire interface SCL (clock), SDA (address& data), and Int_L/Reset_L signals. The electrical specifications are given in Table 1.

Parameter	Symbol	Min	Max	Unit
Input Voltage Low	V_{il}	-0.3	0.4	V
Input Voltage High	V_{ih}	2.3	3.6	V
Output Voltage Low	V_{ol}	-0.3	0.3	V
Output Voltage High	V_{oh}	2.8	3.6	V
Output Current High	I_{oh}	-10	10	µA
Capacitance on SCL and SDA contacts	Ci,SCLSDA		14	pF
Capacitance on Int_L/Reset_L I/O contacts	Ci,INT_L		14	pF
Total Bus capacitive load	C_b		28	pF

Table 18: Low Speed Control and Sense Signal Specifications

Management Interface Timing specification

In order to support a multi-lane device a 400 kHz clock rate for the serial interface is expected. The timing requirements are shown in Figure 36 and specified in Table 18. All values are referred to V_{ih}(min) and V_{il}(max) levels shown in Table 1.

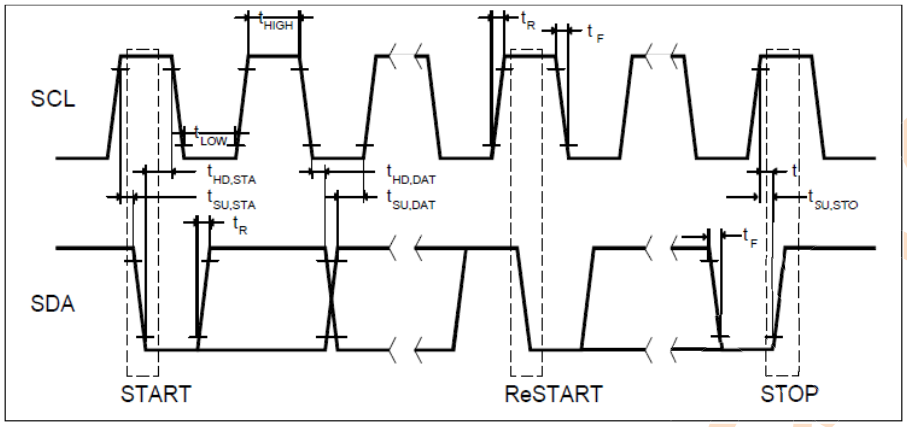


Figure 36: Management interface two wire serial interface timing diagram

Parameter	Symbol	Min	Max	Unit	Condition
Clock Frequency	f_{SCL}	5	400	kHz	
Clock Pulse Width Low	t_{LOW}		1.3	µs	
Clock Pulse Width High	t_{HIGH}		0.6	µs	
Time bus free before new transmission can start	t_{BUF}			µs	1
START Set-up Time	$t_{SU,STA}$		0.6	µs	
START Hold Time	$t_{HD,STA}$		0.6	µs	
Data Set-up Time	$t_{SU,DAT}$		0.1	µs	2
Data Hold Time	$t_{HD,DAT}$		0	µs	3
SDA and SCL rise time	t_{R},400		0.3	µs	4
SDA and SCL fall time	t_{F},400		0.3	µs	5
STOP Set-up Time	$t_{SU,STO}$		0.6	µs	
ModSelL Set-up Time (QSFP)	$t_{host\_select\_setup}$		2	ms	6
ModSelL Hold Time (QSFP)	$t_{ho}st_{\_select\_hold}$		10	µs	7
ModSelL Aborted sequence - bus release	$t_{deselect\_abort}$		2	ms	8

Table 19: Management interface two wire serial interface timing specifications

1. Between STOP & START and between ACK & ReSTART.
2. Data in Set UP Time is measured from V_{il}(max)SDA or V_{ih}(max)SCL.
3. Data in Hold Time is measured from V_{il}(max)SCL or V_{ih}(max)SDA or V_{ih}(min)SDA.
4. Rise Time is measured from V_{ol}(max)SDA to V_{oh}(min)SDA.
5. Fall Time is measured from V_{oh}(min)SDA to V_{ol}(max)SDA.
6. Setup time on the select lines before start of a host-initiated serial bus sequence.
7. Delay from completion of a serial bus sequence to changes of the module select status.
8. Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the FireFly™ optical engine releasing SCL and SDA.

4.1.2 Memory interaction Specifications

Non-volatile memory may be accessed in either single-byte or multiple-byte memory blocks. The largest multiple-byte contiguous write operation that a module shall handle is 4 bytes. The minimum size write block is 1 byte.

Timing for Memory Transactions

The management interface memory transaction timings are given in Table 20.

Parameter	Symbol	Min	Max	Unit	Condition
Serial Interface Clock Holdoff- "Clock Stretching"	T_clock_hold		500	µs	1
Complete Single or Sequential Write	t_{WR}		40	ms	2
Endurance (write cycles)		50,000		cycles	3

Table 20: Management interface memory transaction timing specification

1. Maximum time the optical assembly may hold the SCL line low before continuing with a read or write operation.
2. Complete up to 4 Byte write. Timing should start from Stop bit at the end of the sequential write operation and continue until the module responds to another operation.
3. 50,000 write cycles at 70 °C.

Timing for Control and Status Functions

Timing for the FireFly™ optical assemblies' control and status functions are described in Table 21:

Parameter	Symbol	Min	Max	Unit	Notes
Initialisation Time	tinit		2000	ms	1, 2, 3
Reset Pulse Width – Min	treset_L,PW-min	25		ms	4
Monitor Data Ready Time	tdata		2	s	5
Reset Assert Time	tRSTL,OFF		2	ms	6
Int_L Assert Time	tInt_L,ON		200	ms	7
Interrupt Pulse Width - Min	tInt_L,PW-min	5		µs	8
Interrupt Pulse Width – Max	tInt_L,PW-max		50	ms	9
Int_L Deassert Time	tInt_L,OFF		100	ms	10
Rx LOS Assert Time	tLOS,ON		100	ms	11
Tx Fault Assert Time	tTxfault,ON		200	ms	12
Flag Assert Time	tflag,ON		200	ms	13
Mask Assert Time	tmask,OFF		100	ms	14
Mask Deassert Time	tmask,ON		100	ms	15
Page Select Wait Time, Upper Page 00 or 01	tpage_00/01_select		100	ms	16
Page Select Wait Time, Upper Page 02 or 0b	tpage_02_select		600	ms	17

Table 21: I/O timing for Control and Status Functions

1. Time from power on, hot plug or rising edge of Reset until the optical assembly is fully functional.
2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level
3. Fully functional is defined as Int_L asserted due to Data Not Ready (Byte 2, bit 0) deasserted.
4. This is the minimum Reset_L pulse width required to reset the optical assembly. Assertion of Reset_L activates a complete reset, i.e., the optical assembly returns to the factory default control settings. While Reset_L is Low, Tx and Rx outputs are disabled and the optical assembly does not response to the two-wire serial interface.
5. Time from power on to Data Not Ready (Byte 2, bit 0) deasserted and Int_L asserted.
6. Time from rising edge on the Reset_L contact until the Firefly™ optical assembly is fully functional. During the Reset Time the optical assembly will not respond to a "low" on the Int_L/Reset_L signal.
7. Time from occurrence of condition triggering Int_L until Vout:Int_L = Vol.
8. Int_L operates in pulse mode. Static mode (Int_L stays low until reset by host) is not supported for Int_L.
9. Int_L pulse width must not exceed t_{Int_L},PW-max, to distinguish Int_L from a Reset for other devices on bus.
10. Time from clear on read operation of associated flag until Int_L Status (Lower page, byte 2, bit 1) is cleared. This includes deassert times for Rx LOS, Tx Fault and other flag bits. Measured from falling clock edge after stop bit of read transaction.
11. Time from Rx LOS state to Rx LOS bit set (value = 1b) and Int_L asserted.
12. Time from Tx Fault state to Tx Fault bit set (value = 1b) and Int_L asserted.
13. Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and Int_L asserted.
14. Time from mask bit set (value = 1b) until associated Int_L assertion is inhibited.
15. Time from mask bit cleared (value = 0b) until associated Int_L operation resumes.
16. Time from setting the Upper Page Select Byte (Lower Page Byte 127) to 01h from 00h, or to 00h from 01h, until the associated upper page is accessible.
17. Time from setting the Upper Page Select Byte (Lower Page Byte 127) to 02h or from 02 to either 00h or 01h, until the associated upper page is accessible. This longer period for Upper Page 02, vs. other Upper Pages, allows more complex memory management for this infrequently-accessed upper page.

Timing for Squelch and Disable Functions

Squelch and disable times are described in Table 22.

Parameter	Symbol	Max	Unit	Notes
Rx Squelch Assert Time	$t_{Rxsq,ON}$	0.08	ms	1
Rx Squelch Deassert Time	$t_{Rxsq,OFF}$	0.08	ms	2
Tx Squelch Assert Time	$t_{Txsq,ON}$	400	ms	3
Tx Squelch Deassert Time	$t_{Txsq,OFF}$	400	ms	4
Tx Channel Disable Assert Time	$t_{Txdis,ON}$	100	ms	5
Tx Channel Disable Deassert Time	$t_{Txdis,OFF}$	400	ms	6
Rx Output Disable Assert Time	$t_{Rxdis,ON}$	100	ms	7
Rx Output Disable Deassert Time	$t_{Rxdis,OFF}$	100	ms	8
Squelch Disable Assert Time	$t_{Sqdis,ON}$	100	ms	9
Squelch Disable Deassert Time	$t_{Sqdis,OFF}$	100	ms	10

Table 22: I/O Timing for Squelch and Disable

1. Time from loss of Rx input signal until the squelched output condition is reached.
2. Time from resumption of Rx input signals until normal Rx output condition is reached.
3. Time from loss of Tx input signal until the squelched output condition is reached.
4. Time from resumption of Tx input signals until normal Tx output condition is reached.
5. Time from Tx Disable bit set until optical output falls below 10% of nominal.
6. Time from Tx Disable bit cleared until optical output rises above 90% of nominal. Measured from Stop bit low to high SDA transition.
7. Time from Rx Output Disable bit set (value = 1b) until Rx output falls below 10% of nominal.
8. Time from Rx Output Disable bit cleared (value = 0b) until Rx output rises above 90% of nominal.
9. This applies to Rx and Tx Squelch and is the time from bit set until squelch functionality is disabled
10. This applies to Rx and Tx Squelch and is the time from bit cleared) until squelch functionality is enabled.

4.1.3 Device Operation

Serial Clock (SCL): The host supplied SCL input to the engine is used to positive edge clock data into each FireFly™ optical assembly and negative-edge clock data out of each optical assembly. The SCL line will be pulled low by the module during clock stretching

Serial Data (SDA): The SDA signal is bidirectional for serial data transfer. This signal is open-drain or open-collector driven and may be wire-ORed with multiple open-drain or open collector devices, limited by aggregate capacitance vs. clock speed.

Master/Slave: FireFly™ optical assemblies operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Multiple devices per SCL/SDA: Support of multiple ports in a host is provided through the use of ModSelL

Clock and Data Transitions: The SDA signal is normally pulled high in the host. Data on the SDA signal may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition**.** All addresses and data words are serially transmitted to and from the module in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host are acknowledged by the optical assemblies. Read data bytes transmitted by the module shall be acknowledged by the host for all but the final byte read which will be a NACK then host shall respond with a STOP.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the management interface can be reset. Memory reset is intended only to reset the module management interface (to correct a hung bus). No other transceiver functionality is implied.

Device Addressing: FireFly™ optical assemblies require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits. The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address the module shall output a zero (ACK) on the SDA line to acknowledge the address.

Nomenclature for all registers more than 1 bit long is MSB-LSB.

4.1.4 Read/Write Functionality

This section describes the functionality for read/write operations. Further information can be obtained from Section 8.6 of the “Infiniband™ Architecture” Release 1.3.

Memory Access Counter (Read Operations)

FireFly™ optical assemblies maintain an internal data word address counter containing the last address accessed during the latest read operation, incremented by one. This address stays valid between operations as long as power is maintained. The address “roll over” during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

Read Operations (Current Access Read)

A current address read operation requires only the device address read word (10100001-Tx base address or 10101001-Rx base address) be sent. Once acknowledged by the FireFly™ optical assembly, the current address data word is serially clocked out. The host responds with an acknowledge and generates a STOP condition once the data word is read.

Read Operations (Random Read)

A random read operation requires a write operation to load in the target byte Address. This is accomplished by the following sequence:

- The target 8-bit data word address is sent following the device address write word (1010 0000 or 1010 1000) and acknowledged by the optical assembly.
- The host then generates another START (restart) condition and a current address read by sending a device read base address (1010 0001 for Tx or 1010 1001 for Rx).
- The FireFly™ optical assembly acknowledges the device address and serially clocks out the requested data word.
- The host should generate a STOP condition once the data word is read.

Read Operations (Sequential Read)

Sequential reads are initiated by either a current address read or a random address read. To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the FireFly™ optical assembly receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

Write Operations (Byte Write)

A write operation requires an 8-bit data word address following the device address write word and acknowledgement. Upon receipt of this address, the optical assembly will again respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word. Following the receipt of the 8-bit data word, the optical assembly shall output a zero (ACK) and the host master must terminate the write sequence with a STOP condition for the write cycle to begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START per the two wire interface specification) the write is aborted and the data received during that operation is discarded. Upon receipt of the proper STOP condition, the FireFly™ optical assembly enters an internally timed write cycle, t_{WR}, to internal memory.

The optical assembly disables its management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the write is complete. Note that two wire interface "Combined Format" using repeated START conditions is not supported on write commands.

Write Operations (Sequential Write)

FireFly™ optical assemblies support up to a 4 sequential byte write without repeatedly sending engine address and memory address information. A "sequential" write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the FireFly™ optical assembly acknowledges receipt of the first data word, the host can transmit up to three more data words. The FireFly™ optical assembly will send an acknowledge after each data word received. The host must terminate the sequential write sequence with a STOP condition or the write operation shall be aborted and data discarded. Note that two wire interface "combined format" using repeated START conditions is not supported on write.

4.2 Memory Map

This section defines the Memory Map for the FireFly™ x12 optical assemblies used for serial ID, digital monitoring and control functions. The interface has been derived from the CXP Interface as defined in "*InfiniBand™ Architecture Specification Volume 2*" Release 1.3. The memory map has been modified to separate the transmit and receive functions as well as to remove functionality that is not available within FireFly™ x12 optical assemblies. Paging on upper pages is used to allow slower access to less time-critical information.

The SFF-8436 specification calls for a list of cable parameters to be readable through an I2C interface, commonly referred as the "EEPROM" parameters. When the first standard revision was written, all the parameters were static and were stored in an on-board EEPROM. As revisions evolved, some of the fields became dynamic (such as temperature or optical power readings), while others (such as interrupts and alarms) became Read/Write (R/W). As a result, an EEPROM based implementation does not suffice anymore, although the term is still used to refer to the Memory Map.

Consequently, the Samtec current implementation, although referred to as an "EEPROM map", does not use an actual direct EEPROM read or write. Instead, each I2C read or write request is interpreted by the embedded microprocessor in the optical engine. The microprocessor then reads or stores data which could come from, or go to, different sources:

- The processor's own internal EEPROM
- The processor's static, dynamic RAM or register memory
- Sensors or internal chipset readings
- Internal processor calculations or registers

An important consequence is that EEPROM byte addresses used in I2C requests are virtual – they will not always correspond to the physical address in the processor internal EEPROM, or might not have a physical EEPROM location at all. This is invisible to the end user, who just reads and writes to the I^2C as if it were an actual EEPROM according to the standard Memory Map. The processor will take care of fetching and writing the data internally from/to the correct physical location.

The structure of the memory map is shown in Figure 37. It is assumed that both a TX engine and a RX engine will share the same I2C bus with each having its own I2C address (see Table 17). Each address contains one lower page and four upper pages per address. Each page contains 128 bytes of address space. The lower page or pages contain the most accessed functionality.

This structure permits timely access to fields in the lower page, which contain time-critical information, such interrupt flags, alarms, critical monitors and per-lane control. Read-only device information such as serial ID information and vendor information is available in Upper Page 00, which is similar for both transmit and receive devices.

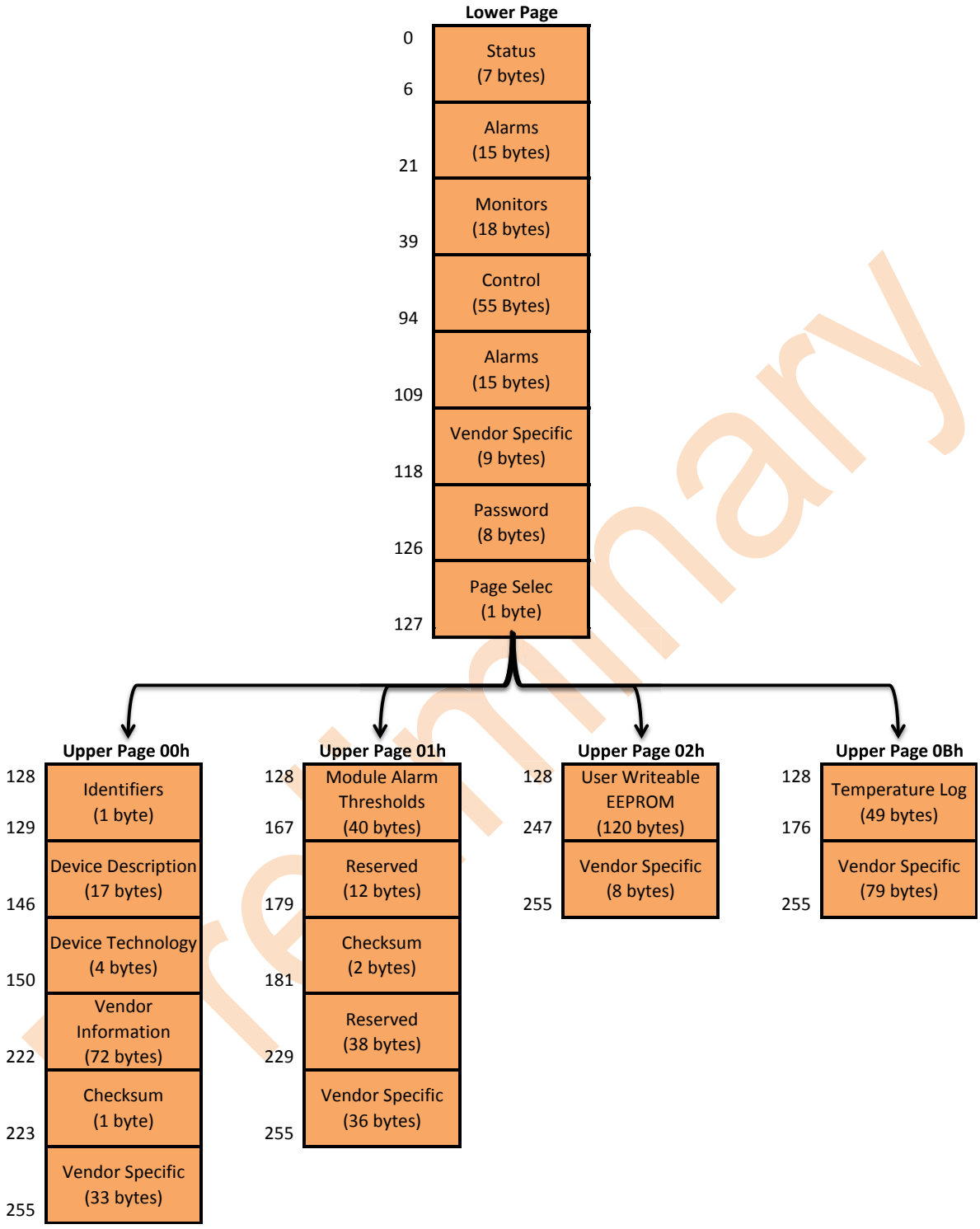


Figure 37: FireFly™ x12 Optical Assembly Memory Map

4.2.1 Transmit Lower Memory Map

The lower 128 bytes of the 2-wire serial bus address space is used to access a variety of measurement and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent reads. This portion of the address space is always directly addressable and is used for monitors and control functions that may need to be repeatedly accessed.

Address	Type	Name	Original CXP field	Function
0	-	Reserved	Reserved	Status
1	-	Reserved	Reserved: Extended Status	
2	RO	Paging Capabilities and Status	Paging Capabilities and Status	
3	-	Reserved	Version Control	
4-5	-	Reserved	Reserved	
6	RO	Status Summaries	Status Summaries	
7-8	-	Reserved	Latch-LOS per Lane	Interrupt Flags
9-10	RO	Latched Alarm – Laser Fault	Latched Alarm – Laser Fault	
11-13	-	Reserved	Latched Alarm – Laser Bias	
14-16	-	Reserved	Latched Alarm – Laser Power	
17	RO	Latched Alarm - Temperature	Latched Alarm - Temperature	
18	RO	Latched Alarm - Vcc	Latched Alarm - Vcc	
19	-	Reserved	Reserved – Vendor Specific	
20-21	-	Reserved	Reserved – Module Alarms	
22	RO	Temperature Monitor	1st Temp Monitor MSB	Monitor Bytes
23	-	Reserved	1st Temp Monitor LSB	
24-25	-	Reserved	2nd Temp Monitor MSB	
26-27	RO	Vcc Monitor	Vcc3.3 Monitor	
28-29	-	Reserved	Vcc12 Monitor	
30-37	-	Reserved	Reserved- Module Monitors	
38-39	RO	Elapsed Operating Time	Elapsed Operating Time	
40	-	Reserved	TX Module Application Select	Control Bytes
41	-	Reserved	TX Rate Select	
42	RW	High Power Mode	High Power Mode	
43-50	-	Reserved	Reserved – Module Control	
51	RW	Reset	Reset	
52-53	RW	Channel Disable	Channel Disable	
54-55	-	Reserved	Output Disable	
56-57	-	Reserved	Squelch Disable	
58-59	RW	Channel Polarity Flip	Channel Polarity Flip	
60-61	-	Reserved	Channel Margin Select	
62-67	-	Reserved	Input Equalization	
68-94	-	Reserved	Reserved	
95-96	-	Reserved	Mask LOS Flag	Alarm Masks
97-98	RW	Mask Fault Flag	Mask Fault Flag	
99-101	-	Reserved	Mask Bias Alarms	
102-104	-	Reserved	Mask Power Alarms	
105	RW	Mask Temperature Alarms	Mask Temperature Alarms	
106	RW	Mask Vcc Alarms	Mask Vcc Alarms	
107	-	Reserved	Vendor Specific Mask	
108-109	-	Reserved	Reserved	
110	RO	EEPROM version	Vendor Specific	Vendor Specific
111-116	RO	Firmware Information	Vendor Specific	
117-118	RO	Reserved	Vendor Specific	
119-122	RW	Password Change Entry Area	Password Change Entry Area	Password
123-126	RW	Password Entry Area	Password Entry Area	
127	RW	Page Select Byte	Page Select Byte	Page Select

Table 23: Transmit Lower Memory Map Overview

Bytes 1 – 6: Status

Status Indicators are defined in Table 24:

Address	Bit	Name	Description	Default Value
1	All	Reserved		-
2	7	Reserved		-
	6	Reserved		-
	5	Tx Upper Page 02 Presence	Upper Page 02 Supported, Tx Addressing	1b
	4	Reserved		-
	3	Rx A8h Address Presence	RX Device Address fields are not present	1b
	2	Flat/Paging Memory Presence	Paging is present	0b
	1	Int_L Status	Value of 1 when asserted Clears to 0 when all flags are cleared	0b
	0	Data_Not_Ready[1]	Indicates optical engine has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low	0b
3	All	Reserved		-
4	All	Reserved		-
5	All	Reserved		-
6	7	Reserved		-
	6	Reserved		-
	5	Fault Status Summary	=1 when a fault flag is asserted for any channel =0 when fault flags are cleared	1b
	4	Reserved		-
	3	Reserved		-
	2	Reserved		-
	1	Module Status Summary	=1 when any Temperature or Voltage alarm is asserted =0 when alarms are cleared	0b
	0	Reserved		-

Table 24: Transmit Lower Page Bytes 1 - 6

[1] The Data_Not_Ready bit is high during module power up and prior to a valid suite of monitor reading. Once all monitor readings are valid, the bit is set low until the device is powered down.

Bytes 7 - 21: Interrupt Flags

Bytes 7 through 21 form a flag field. Within this field, the status of LOS and Tx Fault as well as alarms and warnings for the various monitored items are reported. For normal operation and default state, the bits in this field have the value of 0b. For the defined conditions of LOS, Tx Fault, module and channel alarms and warnings, the appropriate bit or bits are set, value = 1b. Once asserted, the bits remained set (latched) until cleared by a read operation that includes the affected bit or reset by the ResetL pin.

Fault bits that are cleared while the underlying fault persists MAY be immediately set again by the module. This may or may not cause the IntL to de-assert and then re-assert quickly. The Channel Status Interrupt Flags are defined in Table 24. These flags may be masked.

Address	Bit	Name	Description	Default Value
7	All	Reserved		-
8	All	Reserved		-
9	7-4	Reserved		0b
	3	L-Fault TX-11	Latched laser channel fault indicator Default = 0 Fault condition = 1. Value clears on read. .	0b
	2	L-Fault TX-10		
	1	L-Fault TX-09		
	0	L-Fault TX-08		
10	7	L-Fault TX-07		
	6	L-Fault TX-06		
	5	L-Fault TX-05		
	4	L-Fault TX-04		
	3	L-Fault TX-03		
	2	L-Fault TX-02		
	1	L-Fault TX-01		
	0	L-Fault TX-00		
11	All	Reserved		-
12	All	Reserved		-
13	All	Reserved		-
14	All	Reserved		-
15	All	Reserved		-
16	All	Reserved		-
17	7	L-Temp High Alarm	Latched temperature alarm, default value =0 High / Low alarm value =1. Resets on read	0b
	6	L-Temp Low Alarm		
	5-0	Reserved		-
18	7	L-$Vcc_{3.3}$ High Alarm	Latched bias alarm, default value = 0 High / Low alarm value =1. Resets on read	0b
	6	L-$Vcc_{3.3}$ Low Alarm		
	5-0	Reserved		-
19	All	Reserved		-
20	All	Reserved		-
21	All	Reserved		-

Table 25: Transmit Lower Page Bytes 7 - 21

Bytes 22 – 39: Monitor Bytes

Real time monitoring for the FireFly™ x12 Tx optical assembly includes case temperature, supply voltage, and elapsed operating time. These monitor bytes are defined in Table 26.

Internally measured case temperature is represented as an 8-bit signed two's complement value in increments of 1 °Celsius, yielding a total range of –128°C to +128°C that is considered valid between –40°C and +125°C. Accuracy is ± TBD °C

Internally measured module supply voltage are represented as a 16-bit unsigned integer with the voltage defined as the full 16 bit value (0 – 65535) with LSB equal to 100 µVolt, yielding a total measurement range of 0 to +6.55 Volts. Accuracy is ± 0.1 Volts.

Elapsed Operating Time is represented as a 16-bit unsigned integer with the time defined as the full 16 bit value (0 – 65535) with LSB equal to 2 hours, yielding a total measurement range of 0 to 131,070 hours or >14 years. Accuracy is ± 10%.

Address	Bit	Name	Description	Default Value
22	All	Case Temp Monitor	Signed bit twos complement [°C] Accuracy is ±TBD °C	-
23	All	Reserved		-
24	All	Reserved		-
25	All	Reserved		-
26	All	Vcc Monitor MSB	16-bit unsigned integer [µV]. Accuracy is ± 0.1 V	-
27	All	Vcc Monitor LSB		-
28	All	Reserved		-
29	All	Reserved		-
30	All	Reserved		-
31	All	Reserved		-
32	All	Reserved		-
33	All	Reserved		-
34	All	Reserved		-
35	All	Reserved		-
36	All	Reserved		-
37	All	Reserved		-
38	All	Elapsed Operating Time MSB	16-bit unsigned integer [2hours]. Accuracy is ± 10%	-
39	All	Elapsed Operating Time LSB		-

Table 26: Transmit Lower Page Bytes 22 – 39

Bytes 40 - 94: Control Bytes

Control Bytes are used to configure different behaviours within the device. These are defined in Table 27:

Address	Bit	Name	Description	Default Value
40	All	Reserved		-
41	All	Reserved		-
42	All	High Power Mode	Normally used to switch between low power mode (≤ 6 W) and high power mode. This has no affect as the max power consumption is 1.5W	0b
43	All	Reserved		-
44	All	Reserved		-
45	All	Reserved		-
46	All	Reserved		-
47	All	Reserved		-
48	All	Reserved		-
49	All	Reserved		-
50	All	Reserved		-
51	All	Reset	Writing 1 returns all registers to factory default values	0b
52	7-4	Reserved		-
	3	Channel Disable Tx11	Writing 1 will disable channel. Channel will stay disabled until enabled by writing 0, or via reset	0b
	2	Channel Disable TX10		
	1	Channel Disable TX-09		
	0	Channel Disable TX-08		
53	7	Channel Disable TX-07		
	6	Channel Disable TX-06		
	5	Channel Disable TX-05		
	4	Channel Disable TX-04		
	3	Channel Disable TX-03		
	2	Channel Disable TX-02		
	1	Channel Disable TX-01		
	0	Channel Disable TX-00		
54	All	Reserved		-
55	All	Reserved		-
56	All	Reserved		-
57	All	Reserved		-
58	All	Reserved		-
59	All	Reserved		-
60	All	Reserved		-
61	All	Reserved		-
62	All	Reserved		-
63	All	Reserved		-
64	All	Reserved		-
65	All	Reserved		-
66	All	Reserved		-
67	All	Reserved		-
68-94	All	Reserved		-

Table 27: Transmit Lower Page Bytes 40 - 94

Bytes 95 – 109: Alarm Masks

The host system may control which flags trigger an interrupt (IntL) by setting individual bits from a set of masking bits in bytes 95 -109. These are described in Table 28. A "1" value in a masking bit prevents the assertion of the hardware IntL pin by the corresponding latched flag bit. Masking bits are volatile and start up with all unmasked ("0").

The mask bits may be used to prevent continued interruption from on-going conditions, which would otherwise continually re-assert the hardware IntL pin. A mask bit is provided whenever the associated flag bit is implemented.

Address	Bit	Name	Description	Default Value
95	All	Reserved		0b
96	All	Reserved		0b
97	7-4	Reserved		0b
	3	Mask Fault Flag Tx11	Writing 1 prevents Int_L on Fault.	0b
	2	Mask Fault Flag Tx10		
	1	Mask Fault Flag Tx09		
	0	Mask Fault Flag Tx08		
98	7	Mask Fault Flag Tx07		
	6	Mask Fault Flag Tx06		
	5	Mask Fault Flag Tx05		
	4	Mask Fault Flag Tx04		
	3	Mask Fault Flag Tx03		
	2	Mask Fault Flag Tx02		
	1	Mask Fault Flag Tx01		
	0	Mask Fault Flag Tx00		
99	All	Reserved		0b
100	All	Reserved		0b
101	All	Reserved		0b
102	All	Reserved		0b
103	All	Reserved		0b
104	All	Reserved		0b
105	7	Mask Temp High Alarm	Writing 1 prevents Int_L on High/Low Temp Alarm. Default =0	0b
	6	Mask Temp Low Alarm		0b
	5-0	Reserved		0b
106	7	Mask Vcc3.3 High Alarm	Writing 1 prevents Int_L on High/Low Temp Alarm.	0b
	6	Mask Vcc3.3 Low Alarm		0b
	5-0	Reserved		0b
107	All	Reserved		0b
108	All	Reserved		0b
109	All	Reserved		0b

Table 28: Transmit Lower Page Bytes 95 - 109

Bytes 110 – 118: Vendor Specific

Address	Bit	Name	Description	Default Value
110	All	EEPROM Revision		-
111	All	Firmware Version, Major		-
112	All	Firmware Version, Minor		-
113	All	Firmware Revision		-
114	All	Firmware Build Number		-
115	All	Firmware Compile Flags, High		-
116	All	Firmware Compile Flags, Low		-
117	All	Reserved		-
118	All	Reserved		-

Table 29: Transmit Lower Page Bytes 110 - 118

Bytes 119 – 126: Password

Bytes 119-126 are provided for password functionality. Passwords are used to protect specific vendor information. Please contact optics@samtec.com if protected information is required to be changed.

Address	Bit	Name	Description	Default Value
119	All	Password Change Entry		-
120	All	Password Change Entry		-
121	All	Password Change Entry		-
122	All	Password Change Entry		-
123	All	Password Entry		-
124	All	Password Entry		-
125	All	Password Entry		-
126	All	Password Entry		-

Table 30: Transmit Lower Page Bytes 119 - 126

Page Select

Address	Bit	Name	Description	Default Value
127	All	Page Select Byte		0h

Table 31: Transmit Lower Page Byte 127

4.2.3 Transmit Upper Page 00h

The Upper page 00h consists of read only information that describes the cable performance capabilities, technology and length as well as vendor information.

Address	Type	Name	Original CFP field	Function
128	-	Reserved	Reserved	Identifiers
129	RO	Power Class / CDR Identifier	Power Class / CDR Identifier	
130	RO	Connector / Cable	Connector / Cable	Device Description
131	RO	Voltage Requirements	Voltage Requirements	
132	RO	Max Temperature	Max Temperature	
133	RO	Min per channel bit rate	Min per channel bit rate	
134	RO	Max per channel bit rate	Max per channel bit rate	
135-136	RO	Laser Wavelength	Laser Wavelength	
137-138	RO	Wavelength Deviation	Wavelength Deviation	
139-141	RO	TX/RX Identifiers	TX/RX Identifiers	
142-143	RO	TX Identifiers	TX Identifiers	
144-145	-	Reserved	RX Identifiers	
146	RO	Reserved	Identifiers	
147	RO	Device Technology	Device Technology	Device Technology
148	RO	Maximum Power	Max Power Utilization	
149	RO	Data Rates supported	Data Rates supported	
150-151	RO	Cable Length	Cable Length	
152-167	RO	Vendor Name	Vendor Name	Vendor Information
168-170	RO	Vender OUI	Vender OUI	
171-186	RO	Vendor Part Number	Vendor Part Number	
187-188	RO	Vendor Revision Number	Vendor Revision Number	
189-204	RO	Vendor Serial Number	Vendor Serial Number	
205-212	RO	Vendor Date Code	Vendor Date Code	
213-222	RO	Lot Code	Lot Code	
223	RO	Checksum	Checksum	Checksum
224-255	RO	Reserved	Vendor Specific	Vendor Specific

Table 32: Transmit Upper Page 00 Overview

Bytes 128 and 129: Identifiers

Address	Bit	Name	Description	Default Value
128	All	Reserved		-
129	7-5	Power Class	Used to identify the maximum power drawn: Value = 000b: 0.25W max – Class 0 Device Value = 001b: 1.0W max – Class 1 Device Value = 010b: 1.5W max – Class 2 Device Value = 011b: 2.5W max – Class 3 Device Value = 100b: 4.0W max – Class 4 Device Value = 101b: 6.0W max – Class 5 Device Value = 111b: >6.0W max – Class 6 Device	010b
	4-0	Reserved		-

Table 33: Transmit Upper 00h Bytes 128 & 129

Bytes 130 - 151: Device Description

Address	Bit	Name	Description	Default Value
130	All	Connector/ Cable	32h: Active Optical Cable Assembly 80h: Pigtailed Transmitter Assembly	-
131	7	3.3V Voltage Requirement	1: Supported 0: Not supported	1
	6-0	Reserved		-
132	All	Maximum Recommended Operating Case Temp	8-bit unsigned integer [°C]	46h
133	All	Min per Channel bit Rate (units of 100Mb/s)	7-bit unsigned integer * 100 Mb/s	0Ah
134	All	Max per Channel bit Rate (units of 100Mb/s)	7-bit unsigned integer * 100 Mb/s	8DH
135	All	Laser Wavelength	16 bit hex value with byte 135 as high order byte and byte 136 as low order byte. The laser wavelength is equal to the 16 bit integer value divided by 20 in nm (units of 0.05nm)	42h
136	All	Laser Wavelength		68h
137	All	λ Deviation Tolerance	16 bit value with byte 137 as high order byte and byte 138 as low order byte. The laser wavelength (850nm) is equal to the 16 bit integer value divided by 200 in nm (units of 0.005nm)	07h
138	All	λ Deviation Tolerance		D0h
139	7	Support for Fault	1: Supported 0: Not supported	1
	6	Reserved	Reserved	-
	5	Support for LOS	1: Supported 0: Not supported	0
	4	Reserved	Reserved	-
	3	Support for Squelch	1: Supported 0: Not supported	0
	2	Reserved	Reserved	-
	1	Support for CDR LOS	1: Supported 0: Not supported	0
	0	Reserved	Reserved	-
140	7	Support for Bias Current Monitor	1: Supported 0: Not supported	0
	6	Support for LOP Monitor	1: Supported 0: Not supported	0
	5	Reserved	Reserved	-
	4	Reserved	Reserved	-
	3	Support for Case Temp Monitor	1: Supported 0: Not supported	1
	2	Support for Internal Temp Monitor	1: Supported 0: Not supported	0
	1	Support for Peak Temp Monitor	1: Supported 0: Not supported	1
	0	Support for Elapsed Time Monitor	1: Supported 0: Not supported	1
141	7	BER Monitor Flag	1: Supported 0: Not supported	0

Address	Bit	Name	Description	Default Value
	6	Vcc3.3 Tx monitor Flag	1: Supported 0: Not supported	1
	5	Reserved	Reserved	-
	4	Reserved	Reserved	-
	3	Reserved	Reserved	-
	2	Reserved	Reserved	-
	1	Reserved	Reserved	-
	0	Reserved	Reserved	-
142	7	Tx Channel Disable Capabilities	1: Supported 0: Not supported	1
	6	Reserved	Reserved	-
	5	Reserved	Reserved	-
	4	Reserved	Reserved	-
	3	Reserved	Reserved	-
	2	Reserved	Reserved	-
	1	Tx Polarity Flip Mode Flag	1: Supported 0: Not supported	1
	0	Reserved	Reserved	-
143	All	Reserved		0h
144	All	Reserved		0h
145	All	Reserved		0h
146	All	Reserved		0h

Table 34: Transmit Upper 00h Bytes 130 - 151

Bytes 147-151: Device Technology

The technology used in the device is described in Table 35. The top four bits of Byte 147 describe the technology used.

Address	Bit	Name	Description	Default Value
147	7-4	Device Technology	850 nm VCSEL	0000b
	3	Wavelength Control	0: No wavelength control 1: wavelength control	0b
	2	Cooled Transmitter	0: Uncooled device 1: Cooled laser device	0b
	1	Detector Compatibility	0: PiN detector 1: APD detector	0b
	0	Tuneable Transmitter	0: Fixed wavelength 1: Tuned	0b
148	All	Max Power	8-bit unsigned integer in units of 0.1 W	0fh
149	7	IEEE802.3 CPPI	1: 10x10Gb for 100GbE rate capable 0: not 10x10Gb for 100GbE rate capable	1b
	6	Reserved		-
	5	EDR	1: 25.78125 Gb/s rate capable 0: not 25.78125 Gb/s rate capable	0b
	4	FDR	1: 14.0625 Gb/s rate capable 0: not 14.0625 Gb/s rate capable	1b
	3	QDR	1: 10.0Gb/s rate capable 0: not 10.0Gb/s rate capable	1b
	2	DDR	1: 5.0 Gb/s rate capable 0: not 5.0 Gb/s rate capable	1b
	1	SDR	1: 2.5 Gb/s rate capable 0: not 2.5 Gb/s rate capable	1b
	0	12x to 3-4x	1: Breakout Cable 0: Normal	0b
150-151	All	Cable length	16-bit unsigned integer in units of 0.5 m	-

Table 35: Transmit Upper 00h Bytes 147-151

Bytes 152 – 222: Vendor Information

Address	Bit	Name	Description	Default Value
152-167	All	Vendor Name	16 character ASCII field, left-aligned and padded on the right with ASCII spaces (20h). Value = “Samtec Inc “	-
168-170	All	Vendor OUI	The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor.	04h C8h 80h
171-186	All	Vendor Part Number	16 character ASCII field. Format is “OT1214GLLLHHVVCC” where LLL=length in cm HH = heatsink variant VV = variant CC= connector	-
187-188		Vendor Revision Number	2 character ASCII field	“0 “
189-204		Vendor Serial Number	16 character ASCII field, left-aligned and padded on the right with ASCII spaces (20h).	-
205-212		Vendor Date Code	16 character ASCII field. Format is “YYYYMMDD” where: YYYY = Numerical year MM = Numerical month DD = Numerical day	-
213-222		Lot Code	10 character ASCII field, left-aligned and padded on the right with ASCII spaces (20h).	-

Table 36: Transmit Upper 00h Bytes 152-222

Byte 223: Checksum

Address	Bit	Name	Description	Default Value
223	All	Checksum	The checksum shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 222, inclusive.	-

Table 37: Transmit Upper 00h Byte 223

Bytes 2224 – 255: Reserved Bytes

These bytes are reserved for future functionality.

Address	Bit	Name	Description	Default Value
224-255	All	Reserved		FFh

Table 38: Transmit Upper 00h Bytes 224-255

4.2.4 Transmit Upper Page 01h

Transmit Upper Page 01h provides Module Alarm Thresholds plus capacity for future Channel Alarm Threshold functionality. High and Low threshold values for the module alarms are stored in read-only memory in bytes 128 – 167 of the Upper Page 01h as shown in Table 40. These factory-preset values correspond to the values at which the module alarms (Bytes 22-39) are triggered as performance is not guaranteed. If no corresponding mask is set then the IntL signal will be triggered.

Address	Type	Name	Original CFP field	Function
128	RO	Temp Alarm Threshold Hi	1st Temp Alarm Threshold Hi MSB	Module Alarm Threshold Settings
129	-	Reserved	1st Temp Alarm Threshold Hi LSB	
130	RO	Temp Alarm Threshold Low	1st Temp Alarm Threshold Lo MSB	
131	-	Reserved	1st Temp Alarm Threshold Lo LSB	
132	-	Reserved	2nd Temp Alarm Threshold Hi MSB	
133	-	Reserved	2nd Temp Alarm Threshold Hi LSB	
134	-	Reserved	2nd Temp Alarm Threshold Lo MSB	
135	-	Reserved	2nd Temp Alarm Threshold Lo LSB	
136-143	-	Reserved	Reserved	
144-145	RO	Vcc Bias Alarm Threshold Hi	Vcc3.3 Bias Alarm Threshold Hi	
146-147	RO	Vcc Bias Alarm Threshold Low	Vcc3.3 Bias Alarm Threshold Low	
148-149	-	Reserved	Vcc12 Bias Alarm Threshold Hi	
150-151	-	Reserved	Vcc12 Bias Alarm Threshold Low	
152-167	-	Reserved	Reserved	
168-169	-	Reserved	Laser Bias Alarm Threshold Hi	Channel Alarm Threshold Settings
170-171	-	Reserved	Laser Bias Alarm Threshold Low	
172-173	-	Reserved	Laser Power Alarm Threshold Hi	
174-175	-	Reserved	Laser Power Alarm Threshold Low	
176-179	-	Reserved	Reserved	
180-181	RO	Checksum	Checksum	Checksum
182-205	-	Reserved	Bias Current Monitor	Per Channel Monitors
206-229	-	Reserved	Output Power Monitor	
230-255	-	Reserved	Vendor Specific	Vendor Specific

Table 39: Transmit Upper Page 01h Overview

Bytes 128 – 167: Module Alarm Thresholds

Address	Bit	Name	Description	Default Value
128	All	Temp Alarm Threshold Hi	8-bit unsigned integer [°C] Value = 70 °C	46h
129	All	Reserved		-
130	All	Temp Alarm Threshold Low	8-bit unsigned integer [°C] Value = 0 °C	0h
131	All	Reserved		-
132	All	Reserved		-
133	All	Reserved		-
134	All	Reserved		-
135	All	Reserved		-
136-143	All	Reserved		-
144	All	V_{cc}3.3 Alarm Threshold Hi MSB	16-bit unsigned integer in 100µV units Value = 3.465V	87h
145	All	V_{cc}3.3 Alarm Threshold Hi LSB		5Ah
146	All	V_{cc}3.3 Alarm Threshold Lo MSB	16-bit unsigned integer in 100µV units Value = 3.135V	7Ah
1474	All	V_{cc}3.3 Alarm Threshold Lo LSB		76h
148	All	Reserved		-
149	All	Reserved		-
150	All	Reserved		-
151	All	Reserved		-
152-167	All	Reserved		-

Table 40: Upper 01h Bytes 128-255

Bytes 168 -179: Channel Alarm Thresholds: bytes 168-179

As there are no individual channel alarms available through the digital interface, there are no corresponding channel alarm thresholds.

Address	Bit	Name	Description	Default Value
168-179	All	Reserved		-

Table 41: Upper 01h Bytes 168-179

Bytes 180 -181: Checksum

Address	Bit	Name	Description	Default Value
180	All	Checksum	The checksum is the low order 16 bits of the sum of the contents of all bytes from byte 128 to byte 179, inclusive.	-
181	All	Checksum		-

Table 42: Upper 01h Bytes 180-181

Bytes 182-205: Per Channel Monitors

Bytes 182-205 are reserved as there are no individual channel monitors (bias current and output power) available through the digital interface.

Address	Bit	Name	Description	Default Value
182-205	All	Reserved		-

Table 43: Upper 01h Bytes 168-179

Bytes 205 – 255: Reserved Bytes

These bytes are reserved for future functionality.

Address	Bit	Name	Description	Default Value
205-255	All	Reserved		FFh

Table 44: Upper 01h Bytes 224-255

4.2.5 Transmit Upper Page 02h

Upper Page 02h provides 120 sequential bytes for User/Host writeable non-volatile EEPROM.

Address	Type	Name	Original CFP field	Function
128-247	RW	User EEPROM	User EEPROM	User Writeable EEPROM
230-255	-	Reserved	Vendor Specific	Vendor Specific

Table 45: Transmit Upper Page 02h Overview

4.2.6 Transmit Upper Page 0Bh

Time at temperature information is provided for possible end of life prediction. Time at temperature bytes are represented as a 16-bit unsigned integer with the time defined as the full 16 bit value (0 – 65535) with LSB (higher byte) equal to 2 hours.

A peak temperature monitor is also provided. Temperature is recorded as an 8-bit unsigned integer corresponding to the maximum recorded case temperature [°C]. Accuracy is ±TBD °C.

Address	Type	Name	Function
128-129	RO	Time at Temperature < 0°C	Temperature Monitors
130-131	-	Reserved	
132-133	RO	0 °C ≤ Time at Temperature < 10 °C	
134-135	-	Reserved	
136-137	RO	10 °C ≤ Time at Temperature < 20 °C	
138-139	-	Reserved	
140-141	RO	20 °C ≤ Time at Temperature < 30 °C	
142-143	-	Reserved	
144-145	RO	30 °C ≤ Time at Temperature < 40 °C	
146-147	-	Reserved	
148-149	RO	40 °C ≤ Time at Temperature < 50 °C	
150-151	-	Reserved	
152-153	RO	50 °C ≤ Time at Temperature < 60 °C	
154-155	-	Reserved	
156-157	RO	60 °C ≤ Time at Temperature < 70 °C	
158-159	-	Reserved	
160-161	RO	70 °C ≤ Time at Temperature < 80 °C	
162-163	-	Reserved	
164-165	RO	80 °C ≤ Time at Temperature < 90 °C	
166-167	-	Reserved	
168-169	RO	90 °C ≤ Time at Temperature < 100 °C	
170-171	-	Reserved	
172-173	RO	Time at Temperature ≥ 100 °C	
174-175	-	Reserved	
176	RO	Peak Temperature Monitor	
177-255	-	Reserved	Vendor Specific

Table 46: Transmit Upper Page 0Bh Overview

4.2.7 Receive Lower Memory Map

The lower 128 bytes of the 2-wire serial bus address space is used to access a variety of measurement and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent reads. This portion of the address space is always directly addressable and is used for monitors and control functions that may need to be repeatedly accessed.

Address	Type	Name	Original CXP field	Function
0	-	Reserved	Reserved	Status
1	-	Reserved	Reserved: Extended Status	
2	RO	Paging Capabilities and Status	Paging Capabilities and Status	
3	-	Reserved	Reserved	
4-5	-	Reserved	Reserved	
6	RO	Status Summaries	Status Summaries	
7-8	RO	Latched Alarm – LOS	Latch-LOS per Lane	Interrupt Flags
9-10	-	Reserved	Latched Alarm – Fault	
11-13	-	Reserved	Reserved	
14-16	-	Reserved	Latched Alarm – Optical Power	
17	RO	Latched Alarm - Temperature	Latched Alarm - Temperature	
18	RO	Latched Alarm - Vcc	Latched Alarm - Vcc	
19	-	Reserved	Reserved – Vendor Specific	
20-21	-	Reserved	Reserved – Module Alarms	
22	RO	Temperature Monitor	1st Temp Monitor MSB	Monitor Bytes
23	-	Reserved	1st Temp Monitor LSB	
24-25	-	Reserved	2nd Temp Monitor MSB	
26-27	RO	Vcc Monitor	Vcc3.3 Monitor	
28-29	-	Reserved	Vcc12 Monitor	
30-37	-	Reserved	Reserved- Module Monitors	
38-39	RO	Elapsed Operating Time	Elapsed Operating Time	
40	-	Reserved	RX Module Application Select	Control Bytes
41	-	Reserved	RX Rate Select	
42	RW	High Power Mode	Reserved	
43-50	-	Reserved	Reserved – Module Control	
51	RW	Reset	Reset	
52-53	RW	Channel Disable	Channel Disable	
54-55	RW	Output Disable	Output Disable	
56-57	-	Reserved	Squelch Disable	
58-59	-	Reserved	Channel Polarity Flip	
60-61	-	Reserved	Channel Margin Select	
62-67	-	Output Amplitude	Output Amplitude	
68-73	-	Output De-emphasis	Output De-emphasis	
74-94	-	Reserved	Reserved	
95-96	RW	Mask LOS Flag	Mask LOS Flag	Alarm Masks
97-98	-	Reserved	Mask Fault Flag	
99-101	-	Reserved	Reserved	
102-104	-	Reserved	Mask Power Alarms	
105	RW	Mask Temperature Alarms	Mask Temperature Alarms	
106	RW	Mask Vcc Alarms	Mask Vcc Alarms	
107	-	Reserved	Vendor Specific Mask	
108-109	-	Reserved	Reserved	

Address	Type	Name	Original CXP field	Function
110	RO	EEPROM version	Vendor Specific	Vendor Specific
111-116	RO	Firmware Information	Vendor Specific	
117-118	RO	Reserved	Vendor Specific	
119-122	RW	Password Change Entry Area	Password Change Entry Area	Password
123-126	RW	Password Entry Area	Password Entry Area	
127	RW	Page Select Byte	Page Select Byte	Upper Page Select

Table 47: Receive Lower Memory Map Overview

Bytes 1 – 6: Status

Status Indicators are defined in Table 24:

Address	Bit	Name	Description	Default Value
0	All	Reserved		-
1	All	Reserved		-
2	7	Reserved		-
	6	Reserved		-
	5	Reserved		-
	4	RX Upper Page 02 Presence	Upper Page 02 Supported, Rx Addressing	1b
	3	Rx A8h Address Presence	RX Device Address fields are present	0b
	2	Flat/Paging Memory Presence	Paging is present	1b
	1	Int_L Status	Value of 1 when asserted Clears to 0 when all flags are cleared	0b
	0	Data_Not_Ready	Indicates optical engine has not yet achieved power up and monitor data is not ready. Bit remains high until data is ready to be read at which time the device sets the bit low	0b
3	All	Reserved		-
4	All	Reserved		-
5	All	Reserved		-
6	7	Reserved		-
	6	LOS Status Summary	=1 when a fault flag is asserted for any channel =0 when fault flags are cleared	0b
	5	Reserved		-
	4	Reserved		-
	3	Reserved		-
	2	Reserved		-
	1	Module Status Summary	=1 when any Temperature or Voltage alarm is asserted =0 when alarms are cleared	0b
	0	Reserved		-

Table 48: Receive Lower Page Bytes 1 - 6

Bytes 7 - 21: Interrupt Flags

Bytes 7 through 21 form a flag field. Within this field, the status of LOS and Tx Fault as well as alarms and warnings for the various monitored items are reported. For normal operation and default state, the bits in this field have the value of 0b. For the defined conditions of LOS, Tx Fault, module and channel alarms and warnings, the appropriate bit or bits are set, value = 1b. Once asserted, the bits remained set (latched) until cleared by a read operation that includes the affected bit or reset by the ResetL pin.

Fault bits that are cleared while the underlying fault persists MAY be immediately set again by the module. This may or may not cause the IntL to de-assert and then re-assert quickly. The Channel Status Interrupt Flags are defined in Table 49. These flags may be masked.

Address	Bit	Name	Description	Default Value
7	7-4	Reserved		-
	3	L-LOS RX-11	Latched channel LOS indicator Default = 0 Fault condition = 1. Value clears on read.	0b
	2	L-LOS RX-10		0b
	1	L-LOS RX-09		0b
	0	L-LOS RX-08		0b
8	7	L-LOS RX-07	Latched channel LOS indicator Default = 0 Fault condition = 1. Value clears on read.	0b
	6	L-LOS RX-06		0b
	5	L-LOS RX-05		0b
	4	L-LOS RX-04		0b
	3	L-LOS RX-03		0b
	2	L-LOS RX-02		0b
	1	L-LOS RX-01		0b
	0	L-LOS RX-00		0b
9	All	Reserved		-
10	All	Reserved		-
11	All	Reserved		-
12	All	Reserved		-
13	All	Reserved		-
14	All	Reserved		-
15	All	Reserved		-
16	All	Reserved		-
17	7	L-Temp High Alarm	Latched temperature alarm, default value =0 High / Low alarm value =1. Resets on read	0b
	6	L-Temp Low Alarm		0b
	5-0	Reserved		-
18	7	L-$Vcc_{3.3}$ High Alarm	Latched bias alarm High / Low alarm value =1. Resets on read	0b
	6	L-$Vcc_{3.3}$ Low Alarm		0b
	5-0	Reserved		-
19	All	Reserved		-
20	All	Reserved		-
21	All	Reserved		-

Table 49: Receive Lower Page Bytes 7 - 21

Bytes 22 – 39: Monitor Bytes

Real time monitoring for the FireFly™ x12 Rx optical assemblies includes case temperature, supply voltage, and elapsed operating time. These monitor bytes are defined in Table 50.

Internally measured case temperature is represented as an 8-bit signed two's complement value in increments of 1 °Celsius, yielding a total range of –128°C to +128°C that is considered valid between –40°C and +125°C. Accuracy is ± TBD °C

Internally measured module supply voltage are represented as a 16-bit unsigned integer with the voltage defined as the full 16 bit value (0 – 65535) with LSB equal to 100 µVolt, yielding a total measurement range of 0 to +6.55 Volts. Accuracy is ± 0.1 Volts.

Elapsed Operating Time is represented as a 16-bit unsigned integer with the time defined as the full 16 bit value (0 – 65535) with LSB equal to 2 hours, yielding a total measurement range of 0 to 131,070 hours or >14 years. Accuracy is ± 10%.

Address	Bit	Name	Description	Default Value
22	All	Case Temp Monitor	Signed two's complement [°C] Accuracy is ±TBD °C	-
23	All	Reserved		-
24	All	Reserved		-
25	All	Reserved		-
26	All	Vcc Monitor MSB	16-bit unsigned integer [µV]. Accuracy is ± 0.1 V	-
27	All	Vcc Monitor LSB		-
28	All	Reserved		-
29	All	Reserved		-
30	All	Reserved		-
31	All	Reserved		-
32	All	Reserved		-
33	All	Reserved		-
34	All	Reserved		-
35	All	Reserved		-
36	All	Reserved		-
37	All	Reserved		-
38	All	Elapsed Operating Time MSB	16-bit unsigned integer [2hours]. Accuracy is ± 10%	-
39	All	Elapsed Operating Time LSB		-

Table 50: Receive Lower Page Bytes 22 – 39

Bytes 40 - 94: Control Bytes

Control Bytes are used to configure different behaviours within the device. These are defined in Table 51:

Address	Bit	Name	Description	Default
40	All	Reserved		-
41	All	Reserved		-
42	All	High Power Mode	Normally used to switch between low power mode (≤ 6 W) and high power mode. This has no affect as the max power consumption is 2.2W.	0b
43	All	Reserved		-
44	All	Reserved		-
45	All	Reserved		-
46	All	Reserved		-
47	All	Reserved		-
48	All	Reserved		-
49	All	Reserved		-
50	All	Reserved		-
51	All	Reset	Writing 1 returns all registers to factory default values	0b
52	7-4	Reserved		-
	3	Channel Disable RX11	Writing 1 will disable channel. Channel will stay disabled until enabled by writing 0, or via reset	0b
	2	Channel Disable RX10		
	1	Channel Disable RX-09		
	0	Channel Disable RX-08		
53	7	Channel Disable RX-07		
	6	Channel Disable RX-06		
	5	Channel Disable RX-05		
	4	Channel Disable RX-04		
	3	Channel Disable RX-03		
	2	Channel Disable RX-02		
	1	Channel Disable RX-01		
	0	Channel Disable RX-00		
54	7-4	Reserved		-
	3	Output Disable RX11	Writing 1 will disable output. Output will stay disabled until enabled by writing 0, or via reset	0b
	2	Output Disable RX10		
	1	Output Disable RX-09		
	0	Output Disable RX-08		
55	7	Output Disable RX-07		
	6	Output Disable RX-06		
	5	Output Disable RX-05		
	4	Output Disable RX-04		
	3	Output Disable RX-03		
	2	Output Disable RX-02		
	1	Output Disable RX-01		
	0	Output Disable RX-00		
56	All	Reserved		-
57	All	Reserved		-
58	All	Reserved		-
59	All	Reserved		-

Address	Bit	Name	Description	Default
60	All	Reserved		-
61	All	Reserved		-
62	7	Output Amplitude Rx11	0000, 0001 = level 0 0010, 0011 = low (default) 0100, 0101 = medium 0110, 0111 = High	0b
	6	Output Amplitude Rx11		0b
	5	Output Amplitude Rx11		1b
	4	Output Amplitude Rx11		0b
	3	Output Amplitude Rx10		0b
	2	Output Amplitude Rx10		0b
	1	Output Amplitude Rx10		1b
	0	Output Amplitude Rx10		0b
63	7	Output Amplitude Rx09		0b
	6	Output Amplitude Rx09		0b
	5	Output Amplitude Rx09		1b
	4	Output Amplitude Rx09		0b
	3	Output Amplitude Rx08		0b
	2	Output Amplitude Rx08		0b
	1	Output Amplitude Rx08		1b
	0	Output Amplitude Rx08		0b
64	7	Output Amplitude Rx07		0b
	6	Output Amplitude Rx07		0b
	5	Output Amplitude Rx07		1b
	4	Output Amplitude Rx07		0b
	3	Output Amplitude Rx06		0b
	2	Output Amplitude Rx06		0b
	1	Output Amplitude Rx06		1b
	0	Output Amplitude Rx06		0b
65	7	Output Amplitude Rx05		0b
	6	Output Amplitude Rx05		0b
	5	Output Amplitude Rx05		1b
	4	Output Amplitude Rx05		0b
	3	Output Amplitude Rx04		0b
	2	Output Amplitude Rx04		0b
	1	Output Amplitude Rx04		1b
	0	Output Amplitude Rx04		0b
66	7	Output Amplitude Rx03		0b
	6	Output Amplitude Rx03		0b
	5	Output Amplitude Rx03		1b
	4	Output Amplitude Rx03		0b
	3	Output Amplitude Rx02		0b
	2	Output Amplitude Rx02		0b
	1	Output Amplitude Rx02		1b
	0	Output Amplitude Rx02		0b
67	7	Output Amplitude Rx01		0b
	6	Output Amplitude Rx01		0b
	5	Output Amplitude Rx01		1b
	4	Output Amplitude Rx00		0b
	3	Output Amplitude Rx00		0b
	2	Output Amplitude Rx00		0b
	1	Output Amplitude Rx00		1b
	0	Output Amplitude Rx00		0b

Address	Bit	Name	Description	Default
68	7	Output De-emphasis Rx11	0000, 0001 = off (default) 0010, 0011, 0100, 0101, 0110, 0111 = on	0b
	6	Output De-emphasis Rx11		
	5	Output De-emphasis Rx11		
	4	Output De-emphasis Rx11		
	3	Output De-emphasis Rx10		
	2	Output De-emphasis Rx10		
	1	Output De-emphasis Rx10		
	0	Output De-emphasis Rx10		
69	7	Output De-emphasis Rx09		
	6	Output De-emphasis Rx09		
	5	Output De-emphasis Rx09		
	4	Output De-emphasis Rx09		
	3	Output De-emphasis Rx08		
	2	Output De-emphasis Rx08		
	1	Output De-emphasis Rx08		
	0	Output De-emphasis Rx08		
70	7	Output De-emphasis Rx07		
	6	Output De-emphasis Rx07		
	5	Output De-emphasis Rx07		
	4	Output De-emphasis Rx07		
	3	Output De-emphasis Rx06		
	2	Output De-emphasis Rx06		
	1	Output De-emphasis Rx06		
	0	Output De-emphasis Rx06		
71	7	Output De-emphasis Rx05		
	6	Output De-emphasis Rx05		
	5	Output De-emphasis Rx05		
	4	Output De-emphasis Rx05		
	3	Output De-emphasis Rx04		
	2	Output De-emphasis Rx04		
	1	Output De-emphasis Rx04		
	0	Output De-emphasis Rx04		
72	7	Output De-emphasis Rx03		
	6	Output De-emphasis Rx03		
	5	Output De-emphasis Rx03		
	4	Output De-emphasis Rx03		
	3	Output De-emphasis Rx02		
	2	Output De-emphasis Rx02		
	1	Output De-emphasis Rx02		
	0	Output De-emphasis Rx02		
73	7	Output De-emphasis Rx01		
	6	Output De-emphasis Rx01		
	5	Output De-emphasis Rx01		
	4	Output De-emphasis Rx00		
	3	Output De-emphasis Rx00		
	2	Output De-emphasis Rx00		
	1	Output De-emphasis Rx00		
	0	Output De-emphasis Rx00		
74-94	All	Reserved		-

Table 51: Receive Lower Page Bytes 40 - 94

Bytes 95 – 109: Alarm Masks

The host system may control which flags trigger an interrupt (IntL) by setting individual bits from a set of masking bits in bytes 95 -109. These are described in Table 52. A “1” value in a masking bit prevents the assertion of the hardware IntL pin by the corresponding latched flag bit. Masking bits are volatile and start up with all unmasked (“0”).

The mask bits may be used to prevent continued interruption from on-going conditions, which would otherwise continually re-assert the hardware IntL pin. A mask bit is provided whenever the associated flag bit is implemented.

Address	Bit	Name	Description	Default Value
95	7-4	Reserved		-
	3	Mask LOS Flag Tx11	Writing 1 prevents Int_L on LOS.	0b
	2	Mask LOS Flag Tx10		
	1	Mask LOS Flag Tx09		
	0	Mask LOS Flag Tx08		
96	7	Mask LOS Flag Tx07		
	6	Mask LOS Flag Tx06		
	5	Mask LOS Flag Tx05		
	4	Mask LOS Flag Tx04		
	3	Mask LOS Flag Tx03		
	2	Mask LOS Flag Tx02		
	1	Mask LOS Flag Tx01		
	0	Mask LOS Flag Tx00		
97	All	Reserved		-
99	All	Reserved		-
100	All	Reserved		-
101	All	Reserved		-
102	All	Reserved		-
103	All	Reserved		-
104	All	Reserved		-
105	7	Mask Temp High Alarm	Writing 1 prevents Int_L on High/Low Temp Alarm. Default =0	0b
	6	Mask Temp Low Alarm		0b
	5-0	Reserved		-
106	7	Mask Vcc3.3 High Alarm	Writing 1 prevents Int_L on High/Low Temp Alarm.	0b
	6	Mask Vcc3.3 Low Alarm		0b
	5-0	Reserved		-
107	All	Reserved		-
108	All	Reserved		-
109	All	Reserved		-

Table 52: Receive Lower Page Bytes 95 - 109

Bytes 110 – 118: Vendor Specific

Address	Bit	Name	Description	Default Value
110	All	EEPROM Revision		-
111	All	Firmware Version, Major		-
112	All	Firmware Version, Minor		-
113	All	Firmware Revision		-
114	All	Firmware Build Number		-
115	All	Firmware Compile Flags, High		-
116	All	Firmware Compile Flags, Low		-
117	All	Reserved		-
118	All	Reserved		-

Table 53: Receive Lower Page Bytes 110 - 118

Bytes 119 – 126: Password

Bytes 119-126 are provided for password functionality. Passwords are used to protect specific vendor information. Please contact optics@samtec.com if protected information is required to be changed.

Address	Bit	Name	Description	Default Value
119	All	Password Change Entry		-
120	All	Password Change Entry		-
121	All	Password Change Entry		-
122	All	Password Change Entry		-
123	All	Password Entry		-
124	All	Password Entry		-
125	All	Password Entry		-
126	All	Password Entry		-

Table 54: Receive Lower Page Bytes 119 - 126

Page Select

Address	Bit	Name	Description	Default Value
127	All	Page Select Byte		0h

Table 55: Receive Lower Page Byte 127

4.2.8 Receive Upper Page 00h

The Upper page 00h consists of read only information that describes the cable performance capabilities, technology and length as well as vendor information.

Address	Type	Name	Original CFP field	Function
128	-	Reserved	Reserved	Identifiers
129	RO	Power Class / CDR Identifier	Power Class / CDR Identifier	
130	RO	Connector / Cable	Connector / Cable	Device Description
131	RO	Voltage Requirements	Voltage Requirements	
132	RO	Max Temperature	Max Temperature	
133	RO	Min per channel bit rate	Min per channel bit rate	
134	RO	Max per channel bit rate	Max per channel bit rate	
135-136	RO	Laser Wavelength	Laser Wavelength	
137-138	RO	Wavelength Deviation	Wavelength Deviation	
139-141	RO	TX/RX Identifiers	TX/RX Identifiers	
142-143	RO	Reserved	TX Identifiers	
144-145	RO	RX Identifiers	RX Identifiers	
146	RO	Reserved	Identifiers	
147	RO	Device Technology	Device Technology	Device Technology
148	RO	Max Power	Max Power Utilization	
149	RO	Data Rates supported	Data Rates supported	
150-151	RO	Cable Length	Cable Length	
152-167	RO	Vendor Name	Vendor Name	Vendor Information
168-170	RO	Vender OUI	Vender OUI	
171-186	RO	Vendor Part Number	Vendor Part Number	
187-188	RO	Vendor Revision Number	Vendor Revision Number	
189-204	RO	Vendor Serial Number	Vendor Serial Number	
205-212	RO	Vendor Date Code	Vendor Date Code	
213-222	RO	Lot Code	Lot Code	
223	RO	Checksum	Checksum	Checksum
224-255	RO	Reserved	Vendor Specific	Vendor Specific

Table 56: Receive Upper Page 00 Overview

Bytes 128 and 129: Identifiers

Address	Bit	Name	Description	Default Value
128	All	Reserved		-
129	7-5	Power Class	Used to identify the maximum power: Value = 000b: 0.25W max – Class 0 Device Value = 001b: 1.0W max – Class 1 Device Value = 010b: 1.5W max – Class 2 Device Value = 011b: 2.5W max – Class 3 Device Value = 100b: 4.0W max – Class 4 Device Value = 101b: 6.0W max – Class 5 Device Value = 111b: >6.0W max – Class 6 Device	011b
	4-0	Reserved		-

Table 57: Receive Upper 00h Bytes 128 & 129

Bytes 130 - 151: Device Description

Address	Bit	Name	Description	Default Value
130	All	Connector/ Cable	32h: Active Optical Cable Assembly 81h: Pigtailed Receiver Assembly	-
131	7	3.3V Voltage Requirement	1: Supported 0: Not supported	1
	6-0	Reserved		-
132	All	Maximum Recommended Operating Case Temp	8-bit unsigned integer [°C]	46h
133	All	Min per Channel bit Rate (units of 100Mb/s)	7-bit unsigned integer * 100 Mb/s	0Ah
134	All	Max per Channel bit Rate (units of 100Mb/s)	7-bit unsigned integer * 100 Mb/s	8DH
135	All	Operating Wavelength	16 bit hex value with byte 135 as high order byte and byte 136 as low order byte. The laser wavelength is equal to the 16 bit integer value divided by 20 in nm (units of 0.05nm)	42h
136	All	Operating Wavelength		68h
137	All	λ Tolerance	16 bit value with byte 137 as high order byte and byte 134as low order byte. The laser wavelength (850nm) is equal to the 16 bit integer value divided by 200 in nm (units of 0.005nm)	07h
138	All	λ Tolerance		D0h
139	7	Reserved	Reserved	-
	6	Support for Fault	1: Supported 0: Not supported	1
	5	Reserved	Reserved	-
	4	Support for LOS	1: Supported 0: Not supported	1
	3	Reserved	Reserved	-
	2	Support for Squelch	1: Supported 0: Not supported	0
	1	Reserved	Reserved	-
	0	Support for CDR LOS	1: Supported 0: Not supported	0
140	7	Reserved	Reserved	-
	6	Reserved	Reserved	-
	5	Support for Input Power Monitor	1: Supported 0: Not supported	0
	4	Power Format	1: Average Power 2: OMA	1
	3	Support for Case Temp Monitor	1: Supported 0: Not supported	1
	2	Support for Internal Temp Monitor	1: Supported 0: Not supported	0
	1	Support for Peak Temp Monitor	1: Supported 0: Not supported	1
	0	Support for Elapsed Time Monitor	1: Supported 0: Not supported	1
141	7	BER Monitor Flag	1: Supported per channel 0: Not supported	0

Address	Bit	Name	Description	Default Value
	6	Reserved	Reserved	-
	5	Vcc3.3 monitor Flag	1: Supported 0: Not supported	1
	4	Reserved	Reserved	-
	3	Reserved	Reserved	-
	2	Reserved	Reserved	-
	1	Reserved	Reserved	-
	0	Reserved	Reserved	-
142	All	Reserved		-
143	All	Reserved		-
144	7	Channel Disable Capabilities	1: Supported per channel 0: Not supported	1
	6	Reserved		-
	5	Channel Output Disable Capabilities	1: Supported per channel 0: Not supported	1
	4	Reserved		-
	3	Squelch Capabilities	1: Supported per channel 0: Not supported	0
	2	Reserved		-
	1	Polarity Flip Mode Flag	1: Supported 0: Not supported	0
	0	Margin Mode Flag		0
145	All	Reserved		0h
146	All	Reserved		0h

Table 58: Receive Upper 00h Bytes 130 - 151

Bytes 147-151: Device Technology

The technology used in the device is described in Table 59.

Address	Bit	Name	Description	Default Value
147	7-4	Compatible Technology	850 nm VCSEL	0000b
	3	Reserved		-
	2	Reserved		-
	1	Detector	0: PiN detector 1: APD detector	0b
	0	Reserved		-
148	All	Max Power	8-bit unsigned integer in units of 0.1 W	12h
149	7	IEEE802.3 CPPI	1: 10x10Gb for 100GbE rate capable 0: not 10x10Gb for 100GbE rate capable	1b
	6	Reserved		-
	5	EDR	1: 25.78125 Gb/s rate capable 0: not 25.78125 Gb/s rate capable	0b
	4	FDR	1: 14.0625 Gb/s rate capable 0: not 14.0625 Gb/s rate capable	1b
	3	QDR	1: 10.0Gb/s rate capable 0: not 10.0Gb/s rate capable	1b
	2	DDR	1: 5.0 Gb/s rate capable 0: not 5.0 Gb/s rate capable	1b
	1	SDR	1: 2.5 Gb/s rate capable 0: not 2.5 Gb/s rate capable	1b
	0	12x to 3-4x	1: Breakout Cable 0: Normal	0b
150-151	All	Cable length	16-bit unsigned integer in units of 0.5 m	-

Table 59: Receive Upper 00h Bytes 147-151

Bytes 152 – 222: Vendor Information

Address	Bit	Name	Description	Default Value
152-167	All	Vendor Name	16 character ASCII field, left-aligned and padded on the right with ASCII spaces (20h). Value = “Samtec Inc “	-
168-170	All	Vendor OUI	The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor.	04h C8h 80h
171-186	All	Vendor Part Number	16 character ASCII field. Format is “OR1214GLLLHHVVCC” where LLL=length in cm HH = heatsink variant VV = variant CC= connector	-
187-188		Vendor Revision Number	2 character ASCII field	-
189-204		Vendor Serial Number	16 character ASCII field, left-aligned and padded on the right with ASCII spaces (20h).	-
205-212		Vendor Date Code	16 character ASCII field. Format is “YYYYMMDD” where: YYYY = Numerical year MM = Numerical month DD = Numerical day	-
213-222		Lot Code	10 character ASCII field, left-aligned and padded on the right with ASCII spaces (20h).	-

Table 60: Receive Upper 00h Bytes 152-222

Byte 223: Checksum

Address	Bit	Name	Description	Default Value
223	All	Checksum	The checksum shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 222, inclusive.	-

Table 61: Receive Upper 00h Byte 223

Bytes 224 – 255: Reserved Bytes

These bytes are reserved for future functionality.

Address	Bit	Name	Description	Default Value
224-255	All	Reserved		FFh

Table 62: Receive Upper 00h Bytes 224-255

4.2.9 Receive Upper Page 01h

Receive Upper Page 01h provides Module Alarm Thresholds plus capacity for future Channel Alarm Threshold functionality. High and Low threshold values for the module alarms are stored in read-only memory in bytes 128 – 167 of the Upper Page 01h as shown in Table 40. These factory-preset values correspond to the values at which the module alarms (Bytes 22-39) are triggered as performance is not guaranteed. If no corresponding mask is set then the IntL signal will be triggered.

Address	Type	Name	Original CFP field	Function
128	RO	Temp Alarm Threshold Hi	1st Temp Alarm Threshold Hi MSB	Module Alarm Threshold Settings
129	-	Reserved	1st Temp Alarm Threshold Hi LSB	
130	RO	Temp Alarm Threshold Low	1st Temp Alarm Threshold Lo MSB	
131	-	Reserved	1st Temp Alarm Threshold Lo LSB	
132	-	Reserved	2nd Temp Alarm Threshold Hi MSB	
133	-	Reserved	2nd Temp Alarm Threshold Hi LSB	
134	-	Reserved	2nd Temp Alarm Threshold Lo MSB	
135	-	Reserved	2nd Temp Alarm Threshold Lo LSB	
136-143	-	Reserved	Reserved	
144-145	RO	Vcc Bias Alarm Threshold Hi	Vcc3.3 Bias Alarm Threshold Hi	
146-147	RO	Vcc Bias Alarm Threshold Low	Vcc3.3 Bias Alarm Threshold Low	
148-149	-	Reserved	Vcc12 Bias Alarm Threshold Hi	
150-151	-	Reserved	Vcc12 Bias Alarm Threshold Low	
152-167	-	Reserved	Reserved	
168-175	-	Reserved	Reserved	Channel Alarm Threshold Settings
176-177	-	Reserved	Input power Alarm Threshold Hi	
178-179		Reserved	Input power Alarm Threshold Low	
180-181	RO	Checksum	Checksum	Checksum
182-205	-	Reserved	Bias Current Monitor	Per Channel Monitors
206-229	-	Reserved	Output Power Monitor	
230-255	-	Reserved	Vendor Specific	Vendor Specific

Table 63: Receive Upper Page 01h Overview

Bytes 128 – 167: Module Alarm Thresholds

Address	Bit	Name	Description	Default Value
128	All	Temp Alarm Threshold Hi	8-bit unsigned integer [°C] Value = 70 °C	46h
129	All	Reserved		-
130	All	Temp Alarm Threshold Low	8-bit unsigned integer [°C] Value = 0 °C	0h
131	All	Reserved		-
132	All	Reserved		-
133	All	Reserved		-
134	All	Reserved		-
135	All	Reserved		-
136-143	All	Reserved		-
144	All	V_{cc}3.3 Alarm Threshold Hi MSB	16-bit unsigned integer in 100µV units Value = 3.465V	87h
145	All	V_{cc}3.3 Alarm Threshold Hi LSB		5Ah
146	All	V_{cc}3.3 Alarm Threshold Lo MSB	16-bit unsigned integer in 100µV units Value = 3.135V	7Ah
1474	All	V_{cc}3.3 Alarm Threshold Lo LSB		76h
148	All	Reserved		-
149	All	Reserved		-
150	All	Reserved		-
151	All	Reserved		-
152-167	All	Reserved		-

Table 64: Upper 01h Bytes 128-255

Bytes 168 -179: Channel Alarm Thresholds: bytes 168-179

As there are no individual channel alarms available through the digital interface, there are no corresponding channel alarm thresholds.

Address	Bit	Name	Description	Default Value
168-179	All	Reserved		-

Table 65: Upper 01h Bytes 168-179

Bytes 180 -181: Checksum

Address	Bit	Name	Description	Default Value
180	All	Checksum	The checksum is the low order 16 bits of the sum of the contents of all bytes from byte 128 to byte 179, inclusive.	-
181	All	Checksum		-

Table 66: Upper 01h Bytes 180-181

182-205: Per Channel Monitors

Bytes 182-205 are reserved as there are no individual channel monitors (bias current and output power) available through the digital interface.

Address	Bit	Name	Description	Default Value
182-205	All	Reserved		-

Table 67: Upper 01h Bytes 168-179

Bytes 205 – 255: Reserved Bytes

These bytes are reserved for future functionality.

Address	Bit	Name	Description	Default Value
205-255	All	Reserved		FFh

Table 68: Upper 01h Bytes 224-255

4.2.10 Receive Upper Page 02h

Upper Page 02h provides 120 sequential bytes for User/Host writeable non-volatile EEPROM.

Address	Bit	Name	Description	Default Value
128-247	RW	User EEPROM	User EEPROM	User Writeable EEPROM
230-255	-	Reserved	Vendor Specific	Vendor Specific

Table 69: Receive Upper Page 02h Overview

4.2.11 Receive Upper Page 0Bh

Time at temperature information is provided for possible end of life prediction. Time at temperature bytes are represented as a 16-bit unsigned integer with the time defined as the full 16 bit value (0 – 65535) with LSB (higher byte) equal to 2 hours.

A peak temperature monitor is also provided. Temperature is recorded as an 8-bit unsigned integer corresponding to the maximum recorded case temperature [°C]. Accuracy is ±TBD °C

Address	Type	Name	Function
128-129	RO	Time at Temperature < 0°C	Temperature Monitors
130-131	-	Reserved	
132-133	RO	0 °C ≤ Time at Temperature < 10 °C	
134-135	-	Reserved	
136-137	RO	10 °C ≤ Time at Temperature < 20 °C	
138-139	-	Reserved	
140-141	RO	20 °C ≤ Time at Temperature < 30 °C	
142-143	-	Reserved	
144-145	RO	30 °C ≤ Time at Temperature < 40 °C	
146-147	-	Reserved	
148-149	RO	40 °C ≤ Time at Temperature < 50 °C	
150-151	-	Reserved	
152-153	RO	50 °C ≤ Time at Temperature < 60 °C	
154-155	-	Reserved	
156-157	RO	60 °C ≤ Time at Temperature < 70 °C	
158-159	-	Reserved	
160-161	RO	70 °C ≤ Time at Temperature < 80 °C	
162-163	-	Reserved	
164-165	RO	80 °C ≤ Time at Temperature < 90 °C	
166-167	-	Reserved	
168-169	RO	90 °C ≤ Time at Temperature < 100 °C	
170-171	-	Reserved	
172-173	RO	Time at Temperature ≥ 100 °C	
174-175	-	Reserved	
176	RO	Peak Temperature Monitor	
177-255	-	Reserved	Vendor Specific

Table 70: Receive Upper Page 0Bh Overview

5 Power Management

5.1 *Receiver*

The power consumption of the receiver is dependent on several factors:

- Output Swing
- De-emphasis
- Operating conditions (Temperature and Voltage)

The Output swing of each individual channel is controlled through the half octets of bytes 62 – 67 of the receiver lower memory map. The available settings are:

0000, 0001	off	
0010, 0011	Low	(factory default)
0100, 0101	Medium	
0110, 0111	High	

The De-emphasis for each individual channel is controlled though the half octets of bytes 68-73 of the receiver lower memory map. By default, there are two settings available:

0000, 0001	off	(factory default)
0010 – 0111	on	

Changing these settings will change the shape of the electrical output as well as the power consumption. This is shown in Figure 38 (note typical power values listed).

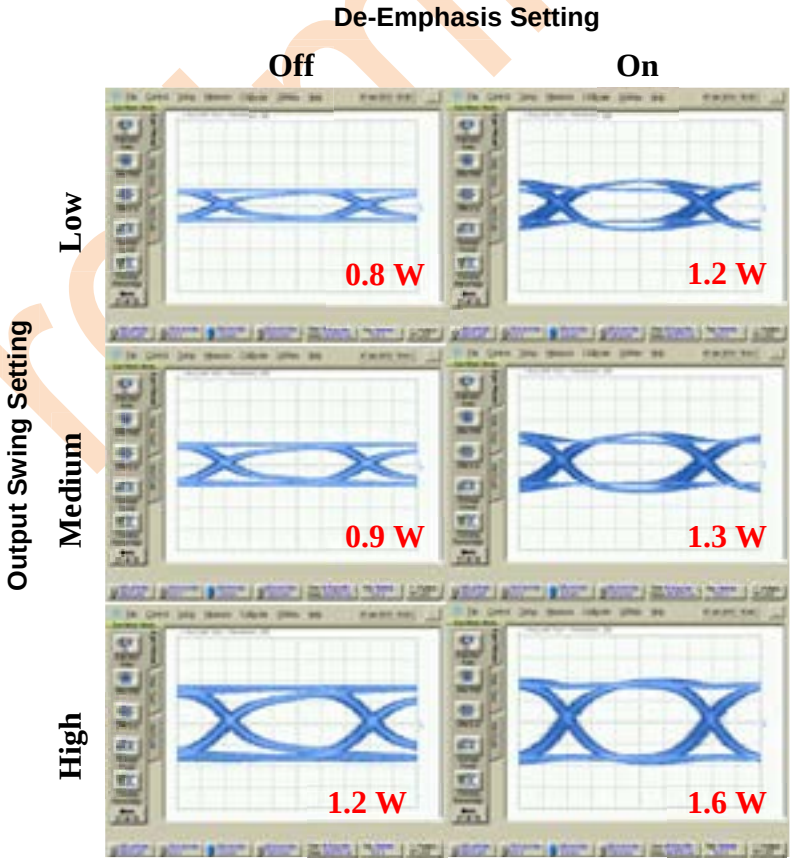


Figure 38: Receiver Output Signal Matrix

Note: the eye diagrams shown in Figure 38 were measured through a Samtec FireFly™ evaluation board, RF switches and through RF cables.

Based on process, voltage and temperature, the absolute worst case maximum power dissipation is shown in Table 71.

		De-emphasis	
		Off	**On**
Output Swing	**Low**	1240 mW	1792 mW
	Medium	1390 mW	1902 mW
	High	1640 mW	2152 mW

Table 71: Absolute Worst Case Receiver Power Dissipation

Note: as these settings can be changed independently for each channel, it is possible to tune only the worse performing channels to fully optimize performance versus power.

5.2 *Transmitter*

The transmitter does not have any user controls that affect the power dissipation. The default factory settings are laser dependent and are optimised for power consumption and performance. The worst case power consumption (over process, voltage and temperature) is 1.5W.

6 On Board Connector Pin Out

6.1 *Electrical Connector Pin Outs*

A simplified foot print showing pin numbers (when viewed from the top) is shown in Figure 39.

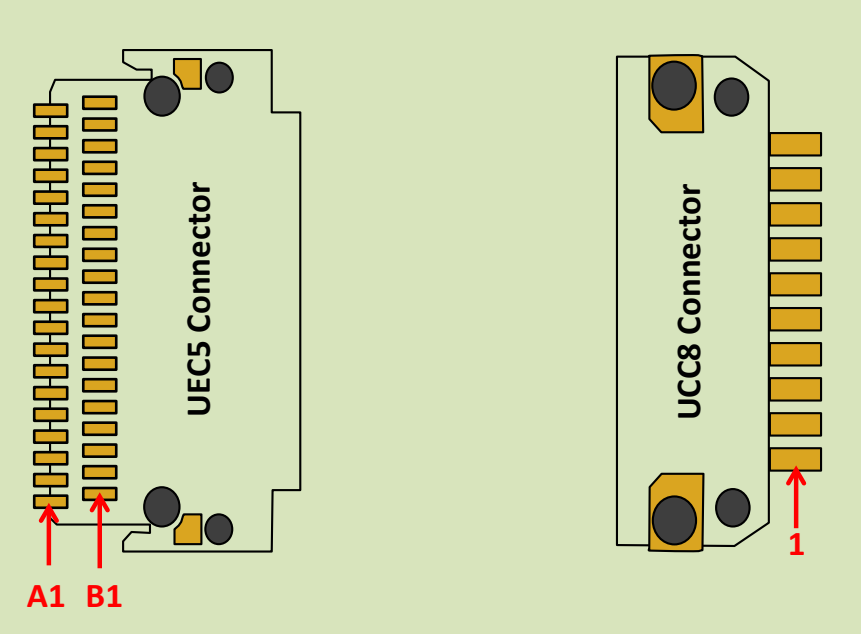


Figure 39: FireFly™ Connector Footprint

6.1.1 UCC8 Connector Pin Out

Standard ECUE copper assemblies do not use the UCC8 connector for electrical connections. ECUO Optical assemblies require these connections which are defined in Table 72.

Pin Number	Description	Symbol	Notes
1	Tx/Rx Supply	VCC	3.3V supply (required)
2	Ground	GND	Signal and Heatsink Ground
3	Module Present	PRESENTL	Module present, active low
4	Module Select	SELECTL	Module select, active low
5	Interrupt	INTL	Interrupt signal for optical module: dual function: Pulsed low to indicate a fault condition Host can reset module and all settings by pulling pin low
6	Module Reset	INTL_RESETL	Module reset pin, active low
7	I2C Data	SDA	I2C interface data lane
8	I2C Clock	SCL	I2C interface clock lane
9	Not used		Not used
10	Tx/Rx Supply	VCC	3.3V supply (required)

Table 72: UCC8 Pin Out

6.1.2 UEC5 Connector Pin Out

The ECUE copper cable assembly can be ordered with two wiring options as shown in Figure 40 and Figure 41. The connector pin out is dependent on the cable assembly used. In both cases, the connector is configured as Ground-Signal-Signal-Ground. However the through connectivity will depend on the wiring option selected.

Figure 40: ECUE-12-XXX-01-01-01-01 Straight Configuration (A1 to A19)

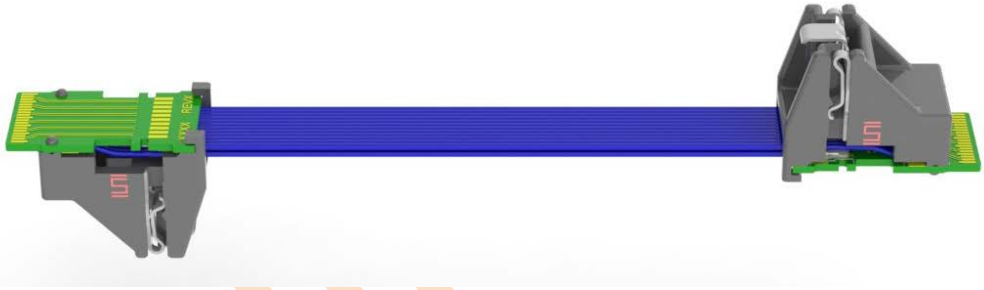


Figure 41: ECUE-12-XXX-01-01-02-01 Cross Configuration (A1 to B1)

The cross configuration is intended for use with applications where an ECUO optical assembly is also used as this provides an equivalent pin-out. If ECUO optical assembly compatibility is not required, the cross configuration can still provide mechanical advantages when routing the cable. The UEC5 connector pin outs for both copper cables are listed in Table 73

Straight Cable			Cross Cable		
Pin Number	Name	End 2 Connection	Pin Number	Name	End 2 Connection
A1	GND	A19	A1	GND	B1
A2	Signal	A18	A2	Signal	B2
A3	Signal	A17	A3	Signal	B3
A4	GND	A16	A4	GND	B4
A5	Signal	A15	A5	Signal	B5
A6	Signal	A14	A6	Signal	B6
A7	GND	A13	A7	GND	B7
A8	Signal	A12	A8	Signal	B8
A9	Signal	A11	A9	Signal	B9
A10	GND	A10	A10	GND	B10
A11	Signal	A9	A11	Signal	B11
A12	Signal	A8	A12	Signal	B12
A13	GND	A7	A13	GND	B13
A14	Signal	A6	A14	Signal	B14
A15	Signal	A5	A15	Signal	B15
A16	GND	A4	A16	GND	B16
A17	Signal	A3	A17	Signal	B17
A18	Signal	A2	A18	Signal	B18
A19	GND	A1	A19	GND	B19
B1	GND	B19	B1	GND	A1
B2	Signal	B18	B2	Signal	A2
B3	Signal	B17	B3	Signal	A3
B4	GND	B16	B4	GND	A4
B5	Signal	B15	B5	Signal	A5
B6	Signal	B14	B6	Signal	A6
B7	GND	B13	B7	GND	A7
B8	Signal	B12	B8	Signal	A8
B9	Signal	B11	B9	Signal	A9
B10	GND	B10	B10	GND	A10
B11	Signal	B9	B11	Signal	A11
B12	Signal	B8	B12	Signal	A12
B13	GND	B7	B13	GND	A13
B14	Signal	B6	B14	Signal	A14
B15	Signal	B5	B15	Signal	A15
B16	GND	B4	B16	GND	A16
B17	Signal	B3	B17	Signal	A17
B18	Signal	B2	B18	Signal	A18
B19	GND	B1	B19	GND	A19

Table 73: ECUO Pin Out when used with ECUE Copper Assemblies

When using ECUO optical cables (or cross configuration ECUE electrical cable), care must be taken to account for the unidirectional nature of the link. This means that row A connections on a connector on one side of the cable are routed to Row B on the connector on the other side. The resulting pin out is shown in Table 74

ECUO TX		
Pin Number	Row A	Row B
1	GND	GND
2	Tx 12N	Tx 11N
3	Tx 12P	TX 11P
4	GND	GND
5	Tx 10N	Tx 9N
6	Tx 10P	TX 9P
7	GND	GND
8	Tx 8N	Tx 7N
9	Tx 8P	TX 7P
10	GND	GND
11	Tx 6N	Tx 5N
12	Tx 6P	TX 5P
13	GND	GND
14	Tx 4N	Tx 3N
15	Tx 4P	TX 3P
16	GND	GND
17	Tx 2N	Tx 1N
18	Tx 2P	TX 1P
19	GND	GND

ECUO RX		
Pin Number	Row A	Row B
1	GND	GND
2	Rx 11N	Rx 12N
3	RX 11P	Rx 12P
4	GND	GND
5	Rx 9N	Rx 10N
6	RX 9P	Rx 10P
7	GND	GND
8	Rx 7N	Rx 8N
9	RX 7P	Rx 8P
10	GND	GND
11	Rx 5N	Rx 6N
12	RX 5P	Rx 6P
13	GND	GND
14	Rx 3N	Rx 4N
15	RX 3P	Rx 4P
16	GND	GND
17	Rx 1N	Rx 2N
18	RX 1P	Rx 2P
19	GND	GND

Table 74: UCE5 Pin Out For ECUO X12 Optical Assemblies

6.2 *Transmit*

The electrical pin out for the ECUO optical assembly is as per Figure 42, Table 72 and Table 74.

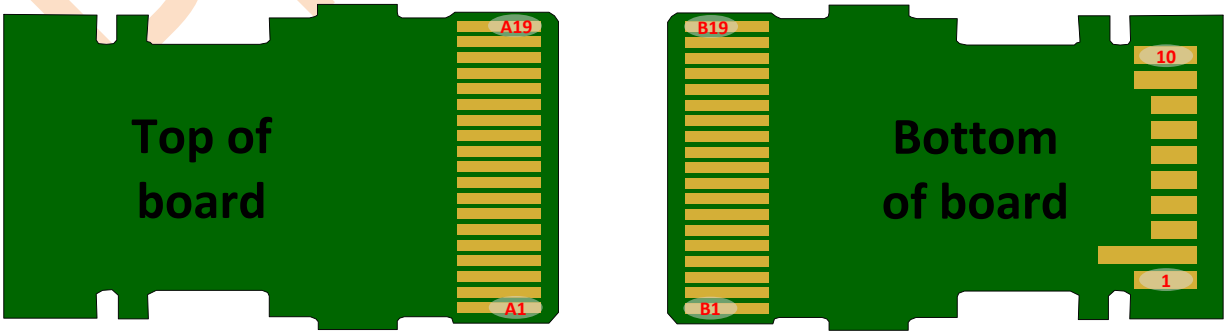


Figure 42: ECUO Pin Out

7 Optical Connector Pin Out

7.1 *ECUO-T12 Optical Connector Pin Out*

The ECUO-T12 uses a 12F MT, MPO or MTP connector. The connector pin out for the optical assembly is shown in Table 75. The colour corresponding to each fiber is also listed for reference.

Fiber Number	Function	Fibre Colour
1	Tx1	Dark Blue
2	Tx2	Orange
3	Tx3	Green
4	Tx4	Brown
5	Tx5	Slate
6	Tx6	White
7	Tx7	Red
8	Tx8	Black
9	Tx9	Yellow
10	Tx10	Violet
11	Tx11	Rose
12	Tx12	Aqua

Table 75: ECUO-T12 Optical Connector Pin Out

7.2 *ECUO-R12 Optical Connector Pin Out*

The ECUO-R12 also uses a 12F MT, MPO or MTP connector. The connector pin out for the optical assembly is shown in Table 76. Again, the colour corresponding to each fiber is also listed for reference.

Fiber Number	Function	Fibre Colour
1	Rx1	Dark Blue
2	Rx2	Orange
3	Rx3	Green
4	Rx4	Brown
5	Rx5	Slate
6	Rx6	White
7	Rx7	Red
8	Rx8	Black
9	Rx9	Yellow
10	Rx10	Violet
11	Rx11	Rose
12	Rx12	Aqua

Table 76: ECUO-R12 Optical Connector Pin Out

7.3 *ECUO-Y12 Optical Connector*

The ECUO-Y12 (described in Section 1.3) has two 12 fiber cables combining in a 24F MT, MPO or MTP connector. The connector pin out for the optical assembly is shown in Table 77. Again, the colour corresponding to each fiber is also listed for reference. For the ECUO-Y12 optical assembly, the two fiber cables will have the same fiber colours. Both cables will have wrapped labels identifying whether they are transmit or receive. In addition, the transmit cable will also have a laser safety warning label.

Note, ECUO-Y12 cables require 24F connectors (Connector option -2*).

Fibre Number	Function	Fiber Colour
1	Tx1	Dark Blue
2	Tx2	Orange
3	Tx3	Green
4	Tx4	Brown
5	Tx5	Slate
6	Tx6	White
7	Tx7	Red
8	Tx8	Black
9	Tx9	Yellow
10	Tx10	Violet
11	Tx11	Rose
12	Tx12	Aqua
13	Rx1	Dark Blue
14	Rx2	Orange
15	Rx3	Green
16	Rx4	Brown
17	Rx5	Slate
18	Rx6	White
19	Rx7	Red
20	Rx8	Black
21	Rx9	Yellow
22	Rx10	Violet
23	Rx11	Rose
24	Rx12	Aqua

Table 77: ECUO-Y12 Optical Connector Pin Out

8 Ordering Information

UEC5 Connector

UEC5 - 019 - 01 - L - D - RA - Weld Tab - A

-1 = Through-hole
-2 = Surface Mount

UCC8 Connector

UCC8 - 010 - 01 - G - S - TH - A - TR

ECUE Copper Assemblies

ECUE - 12 - Cable Length - C1 - End 2 Options - Wiring Options

-XXX = Length (cm)

-FF = ECUE
Also Available = Q Rate®. Edge Rate™
Edge Card, SEARAY™, Q Series®

-01 = Pin A1 to Pin A19
-02 = Pin A1 to Pin B1
For pin for pin compatability with ECUO series, -02 option is required

ECUO Optical Assemblies

ECUO - Width - Data Rate - Cable Length - 0 - Heat Sink - 0 - Fiber Type - End 2 Options

-T12 = x12 Tx
-R12 = x12 Rx
-U12 = Full Active Optical Cable
-Y12 = Y configuration

-B04 = x4 Bidirectional
(in development)

-14 = 14Gb/s

-28 = 28Gb/s
(in development)

-XXX = Length (cm)

-0 = None
-1 = Flat
-2 = Pin-Fin
-3 = Flat HD

-1 = OM3 Ribbon
-2 = OM3 Loose Tube
-3 = OM3 ClearCurve® Ribbon

-4 = OM3 ClearCurve® Loose Tube
(in development)

Leave blank for full AOC
"Y Cable" requires -2* option

-01 = MTP® 12F Key Down Male
-02 = MTP® 12F Key Down Female
-03 = MPO 12F Key Down Male
-04 = MPO 12F Key Down Female
-05 = MT 12F Male
-06 = MT 12F Female

-21 = MTP® 24F Key Down Male
-22 = MTP® 24F Key Down Female
-23 = MPO 24F Key Down Male
-24 = MPO 24F Key Down Female
-25 = MT 24F Male
-26 = MT 24F Female

9 Fiber Connectivity

Care should be taken when interconnecting ECUO optical assemblies to preserve lane numbering assignments. For the Tx1 transmitter to map to the Rx1 receiver there must be one inversion (cross-over) in the fiber link. Recommended methods to retain lane numbering relationship between the Tx and the Rx module are shown in Figure 43.

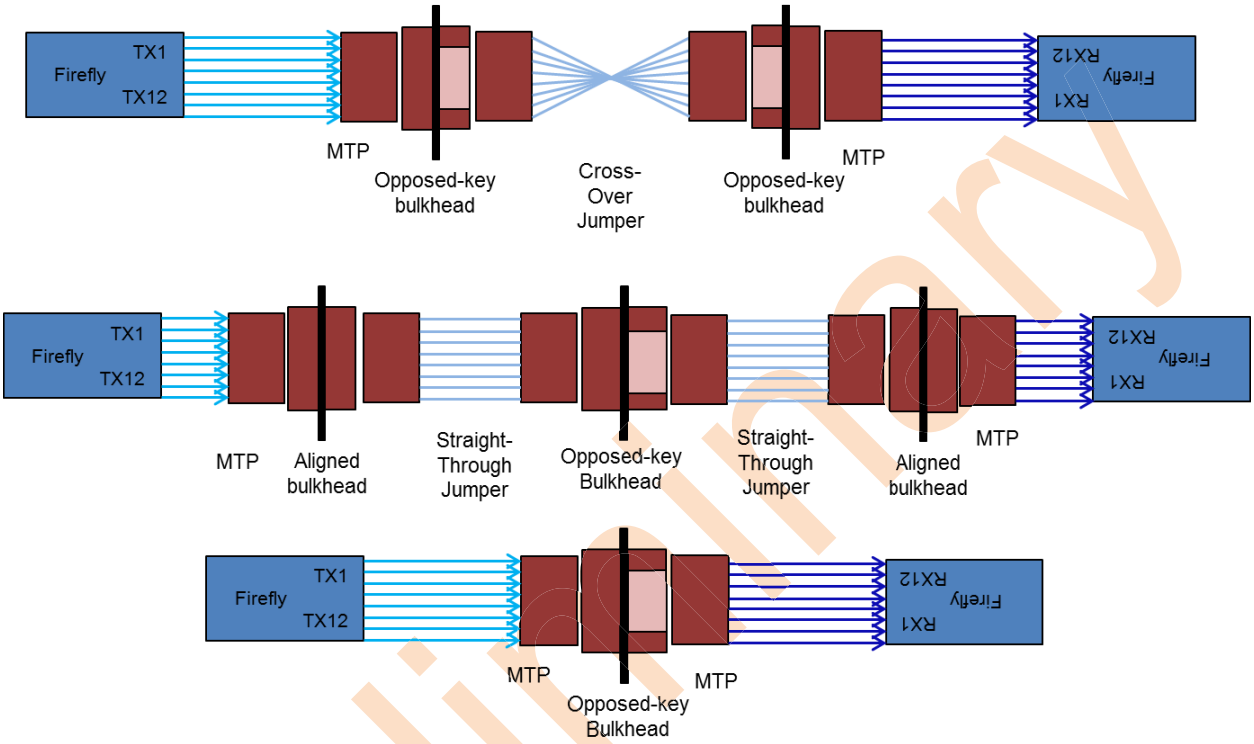


Figure 43: Recommended Fiber Link Implementations

MTP connectors mate through a MT-RJ keyed adapter. These adapters are available in two configurations, an aligned-key and an opposed-key configuration. The opposite key is used to perform a fiber cross-over. The examples shown in Figure 43 are not the only way to achieve inversion, however the examples shown above work for 12F and 24F connector versions of the ECUO optical assembly.

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