OPERATING MANUAL

MODEL 71861

4−channel 200 MHz A/D
with DDCs and Kintex UltraScale FPGA
Jade Family XMC Module

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Model 71861 Operating Manual − Revision History		
Date	**Revision**	**Comments**
12/8/16	0.1	Initial publication
2/8/17	0.2	In General Description − Principle of Operation, Memory, and Model 71861 Specifications, deleted Option 150 − DDR4 memory is standard.
5/15/17	1.0	Updated software description. Register information is only available in the HTML help version of this manual.
7/12/17	1.1	Added Getting the Model 71861 User Manual Library. Added note to DMA section in Chapter 4. Added memory map addresses for Linked List Descriptor RAM to DMA channels in the Data Acquisition table in Chapter 5.
9/19/17	1.2	Revised Getting the Model 71861 User Manual Library and Updates to It.
1/15/18	1.3	Added maximum power input and power consumption data to Model 71861 Specifications. Revised PMC Connector (Option 104). Revised SW1 default configuration in DIP Switch Settings. Revised diagram in Sync Bus. Moved Navigator BSP section into a separate new chapter.
5/18/18	1.4	Revised Pre- Trigger Control.

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Chapter 1: Introduction

General Description

Pentek's Jade™ family Model 71861 is a multichannel, high-speed data converter. The 71861 includes four A/D converters, programmable Digital Downconverters (DDCs), and a large DDR4 memory. In addition to supporting PCI Express Gen 3 as a native interface, the Model 71861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Model 71861 XMC can be attached directly to any digital signal processing (DSP) baseboard equipped with an XMC expansion site, or to an XMC carrier/adaptor, such as the Pentek Model 7807 XMC PCI Express carrier.

This 71861 Operating Manual applies to all of Pentek's Jade family products that include Pentek's Model 71861 XMC, such as the Model 78861 PCIe board, the Model 52861 VPX board, and others.

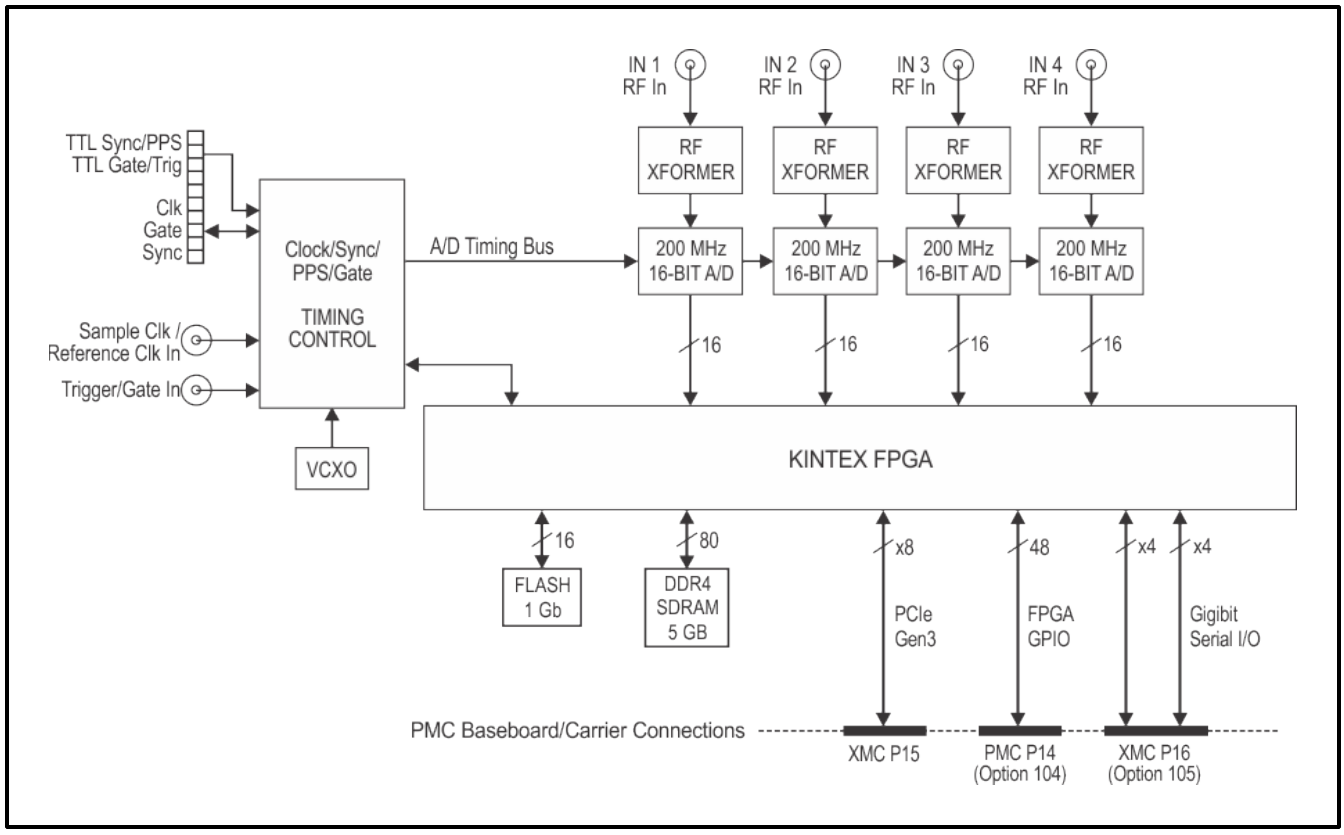
For access to detailed documentation of the IP Core modules and their programmable registers, refer to the HTML help version of this user manual. You can obtain the HTML version by downloading the User Manual Library for the specific board you are using. Instructions are provided in Getting the Model 71861 User Manual Library and Updates to It.

Features

- Four 200-MHz 16-bit A/D converters
- Xilinx® Kintex® UltraScale™ FPGA (Field-Programmable Gate Array)
- Four multiband DDC (digital downconverter) IP Core
- Five gigabytes of DDR4 (Double Data Rate 4th Generation) SDRAM
- Clock synthesizer with programmable clock rates
- LVPECL (Low-Voltage Positive Emitter-Coupled Logic) clock/sync bus for multiboard synchronization
- PCI Express (Gen 1, 2, or 3) interface up to x8 wide
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface to the Kintex FPGA
- Optional LVDS (Low-Voltage Differential Signaling) connections to the Kintex FPGA
- Ruggedized and conduction cooled versions available

Model 71861 Block Diagram

Below is a simplified block diagram of the Model 71861 XMC.



Principle of Operation

Model 71861 is an A/D module suitable for direct connection to HF or IF ports of a communications or radar system. Using the XMC format, it includes four 200−MHz A/D converters, four digital downconverters, and a Xilinx Kintex UltraScale FPGA.

The 71861 features a Xilinx Kintex UltraScale FPGA for signal interfaces and processing. The FPGA is pre−configured by Pentek to provide signal acquisition buffering functions. This FPGA also provides board interfaces including PCIe and XMC. Custom general purpose I/O connections are provided to the FPGA through the optional PMC P14 connector (Option 104). Custom gigabit serial interfaces may be implemented through the optional XMC P16 connector (Option 105).

Four 200−MHz, 16−bit A/D converters provide data to the FPGA, where the data can be formatted, processed, or routed to board resources, including four multiband digital downconverters.

Model 71861 includes an onboard voltage−controlled crystal oscillator (VCXO) and a programmable clock synthesizer for clocking, but can also accept external clocks through front panel connectors. Model 71861 is equipped with an front panel sync bus that allows synchronizing A/D processing on multiple boards.

Model 71861 includes five gigabytes of DDR4 SDRAM. This memory is controlled by the FPGA and is available as a memory resource for custom FPGA applications.

Model 71861 is compatible with VITA 42 XMC carrier boards. This standard provides separate serial data links between the XMC and the carrier. These links support Serial RapidIO, PCI Express, and Aurora protocols and provide a dedicated high−speed streaming data path.

Each member of the Jade family is delivered with factory−installed applications ideally matched to the board's analog interfaces, including IP modules for ADC acquisition and digital signal processing, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface.

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory−installed functions or use the Navigator Design Kit to completely replace the Pentek IP with their own.

Analog to Digital Input Conversion

The 71861 front end accepts four full−scale analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200−MHz, 16−bit A/D converters (ADCs). The ADC digital outputs are delivered into the Kintex UltraScale FPGA for signal processing by the ADC Acquisition Modules and the Digital Downconverters.

A/D Acquisition

The 71861 features four blocks of A/D Acquisition IP Core modules for capturing and moving data. Each block of IP modules can receive data from any of the four A/Ds or from a test signal generator.

Each block of IP modules includes a DMA IP module for easily moving A/D data through the PCIe interface. Each powerful linked-list DMA module is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA module can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

Digital Downconversion

The 71861 provides four DDC IP Core channels. Because of the flexible input routing of A/D Acquisition, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to fs, where fs is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*fs/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of fs/N.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync, and gate or trigger signals. An on-board clock generator receives an external sample clock from a front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. Alternatively, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10-MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts inputs that drive the clock, sync and gate signals. In the master mode, it can drive the timing signals for synchronizing multiple boards. Multiple boards can be driven from the bus master, supporting synchronous sampling and sync functions across all connected boards.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower−cost FPGA can be installed.

Option 104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O. Option 105 installs the P16 XMC connector with dual x4 gigabit links to the FPGA to support serial protocols.

Memory

The 71861 architecture supports a 5−GB bank of DDR4 SDRAM memory. Custom user−installed functions within the FPGA can take advantage of the memory for many purposes. A 1−gigabit FLASH memory supports booting and FPGA configuration.

PCI Express Interface

The Model 71861 includes an industry−standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the baseboard or carrier.

XMC Interface

The Model 71861 complies with the VITA 42.0 XMC specification. Two connectors each provide dual x4 links or a single x8 link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71861 supports x8 PCIe on the first XMC connector leaving the second connector free to support user−installed transfer protocols specific to the application.

Board Support Software: Navigator Design Suite

Pentek's Navigator Design Suite includes the Navigator Board Support Package for creating host applications and the Navigator FPGA Design Kit for integrating custom IP into Pentek's factory-shipped design. These two components of the Suite are described below.

Navigator Board Support Package (BSP)

The Navigator BSP contains software support for Jade boards. This includes a device driver, the Navigator BSP Board Support Library data structures and routines, and example programs. The Navigator BSP enables operational control of the hardware and the IP functions in the FPGA.

The BSP allows software developers to work at a higher level, abstracting many of the details of the hardware through an API. The API allows developers to focus on the task of creating the application by letting the API, the hardware, and the IP-control libraries below it to handle many of the board-specific functions. For developers who want full access to the entire BSP library, complete C-language source code is available.

New applications can be developed on their own or by building on one of the included example programs. All Jade boards are shipped with a full suite of built-in functions, allowing operation without the need for any custom IP development.

The *Navigator BSP User's Guide* describes how to install and use the BSP software.

The *API Reference Guide for the Navigator BSP* describes the source and include files in the BSP and is available in both HTML and PDF format (**`API_Reference.html`** and **`API_Reference.pdf`**). The *API Reference Guide* is available in the following location:

Windows: `C:\Pentek\BSP\BSP_X.Y\docs` (where **`X.Y`** is the version number) or **`%NAVBSP%\docs`**

Linux: `/home/username/Pentek/BSP/BSP_X.Y/docs` (where **`X.Y`** is the version number) or **`$NAVBSP/docs`**

The *Navigator BSP API Reference Guide* describes the BSP header and source files. These manuals are available in PDF format. The *API Reference Guide* is also available in HTML format.

Navigator FPGA Design Kit (FDK)

The Navigator FDK was designed to be used with the Xilinx Vivado Design Suite. Vivado includes the IP Integrator design environment. Built around a graphical block diagram interface, the IP Integrator allows developers to leverage existing IP by importing it into their block diagram design. The Navigator FDK provides the complete IP for a specific Jade board. When the design is opened in Vivado's IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for an application.

The Navigator FDK is a very specialized software package intended for users with experience in FPGA logic programming. This package may not be required if the default functions included in the FPGA code, as written by Pentek, satisfy the requirements of your application. The Navigator Board Support Package (BSP) is always required and should be installed before the Navigator FDK.

The *Navigator FDK User's Guide* describes how to install and use the FDK software. In addition, an *IP Core Manual* is provided for each IP core in the FDK. These can be accessed via the Vivado IP Integrator. Several tutorials also are available:

- *IP Core Conventions Guide and Example Labs* (807.48111)
- *Designing with the PDTI Type AXI−Stream Bus* (807.48112)
- *Designing with the Navigator DDR4 SDRAM Access Interface* (807.48113)

You can get the Navigator FDK and user manuals by contacting sales@pentek.com.

Getting the Model 71861 User Manual Library and Updates to It

A set of user manuals for Model 71861 is provided in HTML help format. This documentation is provided on a DVD and shipped with the board. When the user manuals are updated, you will be notified. You can get the latest user manual library for your product by following the instructions provided below.

If you have any questions please contact your local representative or Pentek directly:

Mario Schiavone, Sales Director, Pentek, Inc.
Phone: +1 (201) 818−5900; Email: sales@pentek.com

To get the user manual library for Model 71861, follow the procedure for the operating system you're using:

Instructions for Windows

1. If your system does not have a recent version of file compression software installed (such as WinZip™), you must install it in order to be able to unlock the zip file containing the user manual library. Older file compression utilities may not be able to unlock the zip file. You can obtain free file compression software from 7−Zip at http://www.7−zip.org/download.html.
2. Click on **this link** to download the self−extracting zip file for the Model 71861 XMC module user manual library. The file name is **71861_docs.exe**.

The zip file for the user manual library is large so downloading it may take a few minutes.

3. Put the **71861_docs.exe** file in the location (folder) in which you want to unzip (extract) the files and double−click **71861_docs.exe**.
4. The zip file is password protected, so you will be prompted to enter the password, which is **71861PEN**.
5. A folder named **71861** is extracted. In this folder you'll see several folders (Content, Data, etc.) and several files, including **71861_docs.htm**.
6. To open the user manual library (HTML help), double−click this file: **71861_docs.htm**. Your browser will display the online help welcome page that provides access to all the user documentation for your board.

The online help welcome page should display a table of contents panel on the left. If that panel is not shown on the left, make your browser window wider. Or reduce the text size using CTRL − (minus).

Instructions for Linux

A self−extracting archive is not available for the Linux platform. The encrypted archive should be extracted using the POSIX port of the 7−zip utility, called **p7zip**. The standard 'unzip' utility in Linux does not support the AES−256 encryption used to password−protect this archive. Binaries (x86, 32−bit) and source code for p7zip are available here: http://-sourceforge.net/projects/p7zip/files/. The program is also available as a package in most major Linux distributions and may already be installed on the system.

1. Click on **this link** to download the zip file for the Model 71861 XMC module user manual library. The file name is **71861_docs.zip**.

The zip file for the user manual library is large so downloading it may take a few minutes.

2. Put the **71861_docs.zip** file in the location (folder) in which you want to unzip (extract) the files.
3. Execute the following command on the console to extract the files:
   7z x 71861_docs.zip
4. The zip file is password protected, so you will be prompted to enter the password, which is **71861PEN**.
5. Refer to steps 5 and 6 in the Windows procedure, above.

Supporting Documentation

Vendor Datasheets and User Guides

In addition to the operating instructions provided in this manual, you can refer to manufacturer datasheets for the programmable devices on the Model 71861:

- Texas Instruments Inc., ADS5485 Analog−to−Digital Converter Datasheet
- Texas Instruments Inc., LM95234 Temperature Sensor Datasheet
- Texas Instruments Inc., LM83 Temperature Sensor Datasheet
- Silicon Labs, Inc., Si571 Any−Rate VCXO Datasheet
- Texas Instruments, Inc., CDCM7005 Clock Synthesizer Datasheet
- Linear Technology Corp., LTC2990 Quad I2C Voltage, Current, and Temperature Monitor Datasheet
- Silicon Labs, Inc., Si5341 Clock Generator Datasheet
- Xilinx Inc., Kintex UltraScale FPGA System Monitor Users Guide

The documents listed above can be accessed from the HTML version of this manual. Pentek provides these datasheets and user guides for your convenience. However, they might be updated by the manufacturer after we obtain them. The latest version of a product's documentation can be found on the manufacturer's website.

Pentek IP Core User Guides

Links to Pentek's IP Core User Guides (PDF format) are provided in the HTML version of the user documentation. The Navigator FPGA Design Kit software also links to Pentek's IP Core User Guides.

Model 71861 Specifications

Analog Signal Inputs

Connectors: Four front panel SSMC connectors: **IN 1**, **IN 2**, **IN 3**, & **IN 4**
Input Type: Single-ended, non-inverting
Full Scale Input: +8 dBm
Maximum Power Input: 14 dBm
Coupling: Transformer coupled
Input Impedance: 50 ohms
Analog Input Transformers:
3dB Passband: 300 kHz to 700 MHz
Insertion Loss: 0.58 dB max.

Analog to Digital Converters

Quantity: Four Texas Instruments ADS5485 A/D converters
Sampling Rate: 10-200 MHz
Resolution: 16 bits
Clock Source: Selectable from onboard VCXO, front panel SSMC clock, or Sync Bus LVPECL clock input

Digital Downconverters (four separate channels)

Decimation Range: 2 to 32,768 in three stages of 2 to 32
LO Tuning Freq. Resolution: 32 bits, 0 to *f*s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients (user-programmable)
24-bit output
Default Filter Set: 80% bandwidth
<0.3 dB passband ripple
>100 dB stopband attenuation

Sync Bus Inputs/Outputs

Connector Type: Front panel 26-pin connector, **SYNC/GATE**
Signals:
CLK In/Out: 2 pins (LVPECL pair)
GATE In/Out: 2 pins (LVPECL pair)
SYNC In/Out: 2 pins (LVPECL pair)
LVTTL GATE/TRIG In: 1 pin (single-ended)
LVTTL SYNC/PPS In: 1 pin (single-ended)
Spares: 6 pins (3 LVPECL pairs)
Grounds: 12 pins
Bus Master/Slave: Bus master or bus slave mode selectable via software
Bus Termination: Bus termination provided by in-line cable end terminator
Number of Boards Supported: Up to four boards can be synchronized with a ribbon cable. Systems requiring more synchronized channels can be supported with the Model 7893 Clock Synthesizer.

Clock

Clock Source: Selectable from external or internal clock
External: Front panel SSMC CLK, or Sync Bus LVPECL CLK
Internal: Generated from programmable VCXO

External Clock Input

Connector Type: Front panel SSMC connector, **CLK**
Signal Type: Sine wave
Frequency Range: 10 to 800 MHz divider input clock or PLL system reference (when greater than 200 MHz, the input clock must be divided down by the CDCM7005 for the ADC clock)
Voltage Range: +0 to +10 dBm
Coupling: AC coupled
Input Impedance: 50 ohms

Internal Sample Clock

Device: Silicon Labs Si571 Any−Rate VCXO
Type: Programmable VCXO
Frequency Range: 10−810 MHz
Start−Up Freq: 200 MHz
Freq Resolution: 0.09 ppb
Interface: FPGA I^2C Bus 0

Clock Synthesizer

Device: Texas Instruments CDCM7005 Clock Synthesizer
Frequency Dividers: 1, 2, 4, 6, 8, and 16
Output Clocks: Five LVPECL output clocks
Interface: FPGA

Gate

Gate Sources: Selectable from external or internal gate
External: Front panel SSMC TRIG, or Sync Bus LVPECL GATE
Internal: Generated from programmable register
Gate Polarity: Programmable polarity for external gate
Triggering: Gate can be programmed as a trigger with a programmable trigger length

Sync

Sync Source: Selectable from external or internal sync
External: Front panel SSMC TRIG, or Sync Bus LVPECL SYNC
Internal: Generated from programmable register
Sync Pulse Width: 2 clock cycles, minimum

External Trigger Input

Connector Type: Front panel SSMC connector, **TRIG**
Signal Type: LVTTL

Field−Programmable Gate Arrays (FPGA)

Standard: Xilinx Kintex UltraScale XCKU035−2
Option 084: Xilinx Kintex UltraScale XCKU060−2
Option 087: Xilinx Kintex UltraScale XCKU115−2
Configuration: Factory programmed by Pentek: A/D, DDC, IP Cores

FPGA MGT Clock Generator

Device: Silicon Labs Si5341B Any−Rate Clock Generator
Type: 10 separate programmable clock outputs
Frequency Range: 100 Hz to 350 MHz
Interface: FPGA I^2C Bus 0

RAM memory

Size: 5 Gigabytes of DDR4 SDRAM
Speed: 1200 MHz (2400 MHz DDR)
Bus Width: 80 bits
Interface: FPGA

Configuration FLASH memory

Size: 1 Gigabit
Bus Width: 16 bits
Interface: FPGA

XMC Interfaces

PCI Express Interface
XMC Connector: 114−pin (XMC standard Pn5 connector), **P15**
Compliance: ANSI/VITA 42.3 XMC PCI Express Protocol Standard
Lanes/Speed:
Gen1 x8 − 2 GB/sec
Gen2 x8 − 4 GB/sec
Gen3 x8 − 8 GB/sec

Secondary XMC Interface (Option 105)
XMC Connector: 114−pin (XMC standard Pn6 connector), **P16**
Compliance: ANSI/VITA 42.0 XMC Standard
Protocol (user must implement these protocols with user FPGA code):
ANSI/VITA 42.2 XMC Serial RapidIO Protocol Standard
ANSI/VITA 42.3 XMC PCI Express Protocol Standard
ANSI/VITA 42.5 Aurora Pin Assignments

PMC Interface (Option 104)

PMC Connector: 64−pin PMC standard Pn4 connector, **P14**
Compliance: 48 I/O lines routed to the FPGA as 24 LVDS pairs or 48 LVCMOS single−ended (2.5V)
Note: Not 3.3V tolerant

Temperature and Voltage Sensors

Main PCB Temperature
Quantity: Four temperature sensors
Controller: Texas Instruments LM95234
Interface: FPGA I^2C Bus 0

Main PCB Power
Quantity: Four voltage inputs (two for 3.3V, two for 12V)
Controller: Linear Technology LTC2990
Interface: FPGA I^2C Bus 0

Main PCB Voltage
Quantity: Ten voltage sensors
Controller: Kintex UltraScale System Monitor
Interface: FPGA

Front Panel Interface Module Temperature
Quantity: Three temperature sensors
Controller: Texas Instruments LM83
Interface: FPGA I^2C Bus 0

Nominal Power Consumption*

Current Draw:	+3.3V (Watts)	VPWR (12V or 5V) (Watts)	Total
XCKU035 (Standard)	TBD	TBD	TBD
XCKU060 (Option 084)	4.79	32.61	37.4
XCKU115 (Option 087)	2.68	37.33	40.02
*With factory IP at the maximum clock rate.			

Physical

Dimensions: Single PMC/XMC board
Depth: 149.0 mm (5.87 in)
Height: 74 mm (2.91 in)
Weight: Approximately 14 oz (400 grams), with 2−slot heatsink

Environmental

Standard: Level L0
Cooling Method (operational): Forced Air
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non−condensing

Pentek Ruggedization Level L1
Pentek Option Number: −701
Cooling Method (operational): Forced Air
Operating Temperature: 0° to 50° C
Storage Temperature: −40° C to +100° C
Sine Vibration: 2g, 20−500 Hz
Random Vibration: 0.01g2/Hz, 20−2000 Hz
Shock: 10g, 11ms
Relative Humidity:
No conformal coating: 0% to 95% non−condensing
Conformal coating (Option 720): 0% to 100% non−condensing

Pentek Ruggedization Level L2
Option Number: −702
Cooling Method (operational): Forced Air
Operating Temperature: −20° to 65° C
Storage Temperature: −40° C to +100° C

Sine Vibration: 2g, 20−500 Hz
Random Vibration: 0.04g2/Hz, 20−2000 Hz
Shock: 20g, 11ms
Relative Humidity:
No conformal coating: 0% to 95% non−condensing
Conformal coating (Option 720): 0% to 100% non−condensing

Pentek Ruggedization Level L3

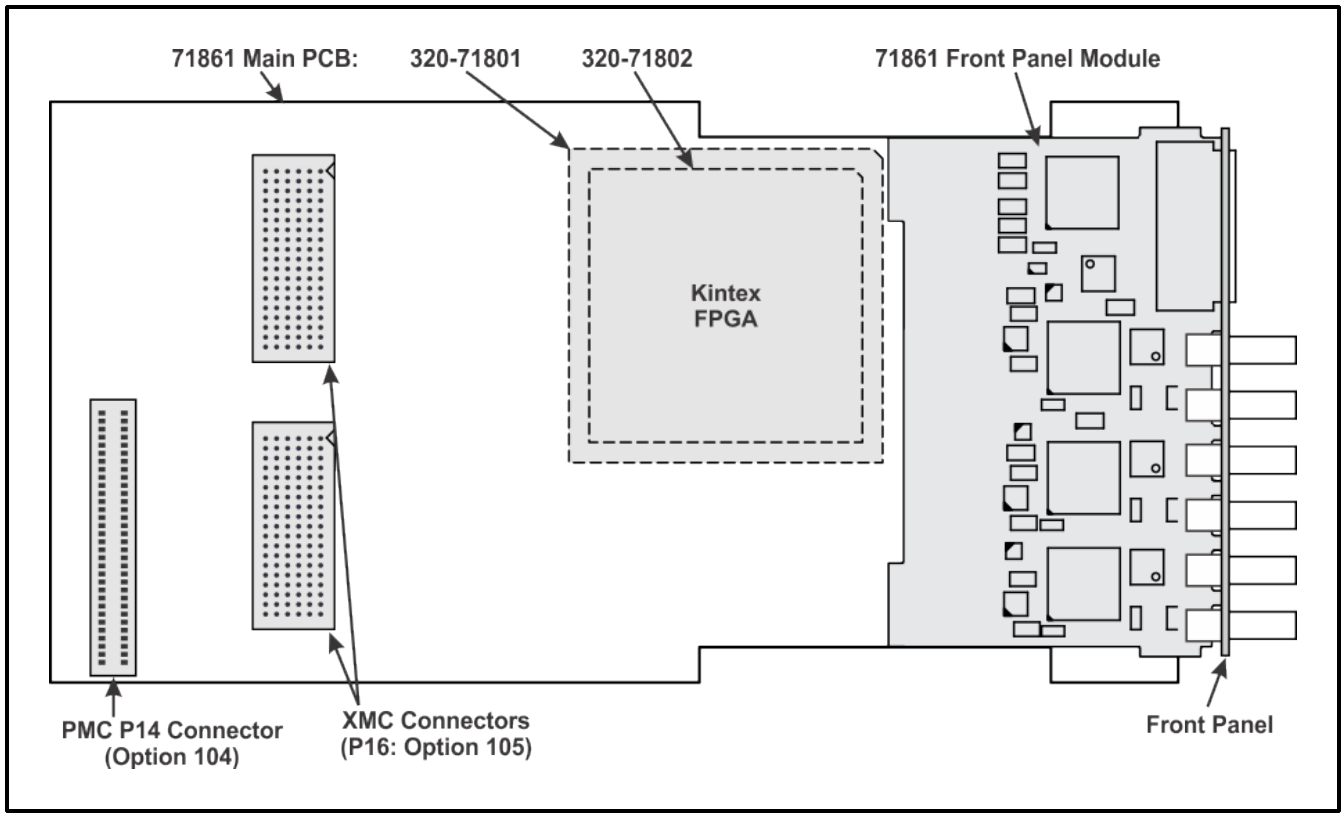
Option Number: −713
Cooling Method (operational): Conduction Cooled
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non−condensing

Chapter 2: Installation and Connections

Inspection

After unpacking, inspect the unit carefully for possible damage to connectors or components. If any damage is discovered, contact Pentek immediately at (201) 818−5900. Please save the shipping container and packing material in case reshipment is required.

The simplified assembly drawing of Model 71861 (below) shows the complete PCB assembly as shipped, including the front panel I/O module and the connectors for Options 104 and 105. Depending on the FPGA option ordered, there are two different main PCBs, part number 320−71801 or 320−71802 as identified below, to accommodate different Kintex FPGA physical profiles.



Note that a heat sink can be mounted on the Model 71861 PCB assembly as shipped.

Minimum System Requirements: The system in which you install this Pentek product should have the latest Intel® Core™ i7 processor with a minimum RAM of 8 GB. PCIe Gen 3 x8 is required. Model 71861 is shipped to boot with Gen 3 x8 PCIe default FPGA code. For more information, refer to "DIP Switch Settings" on the next page.

DIP Switch Settings

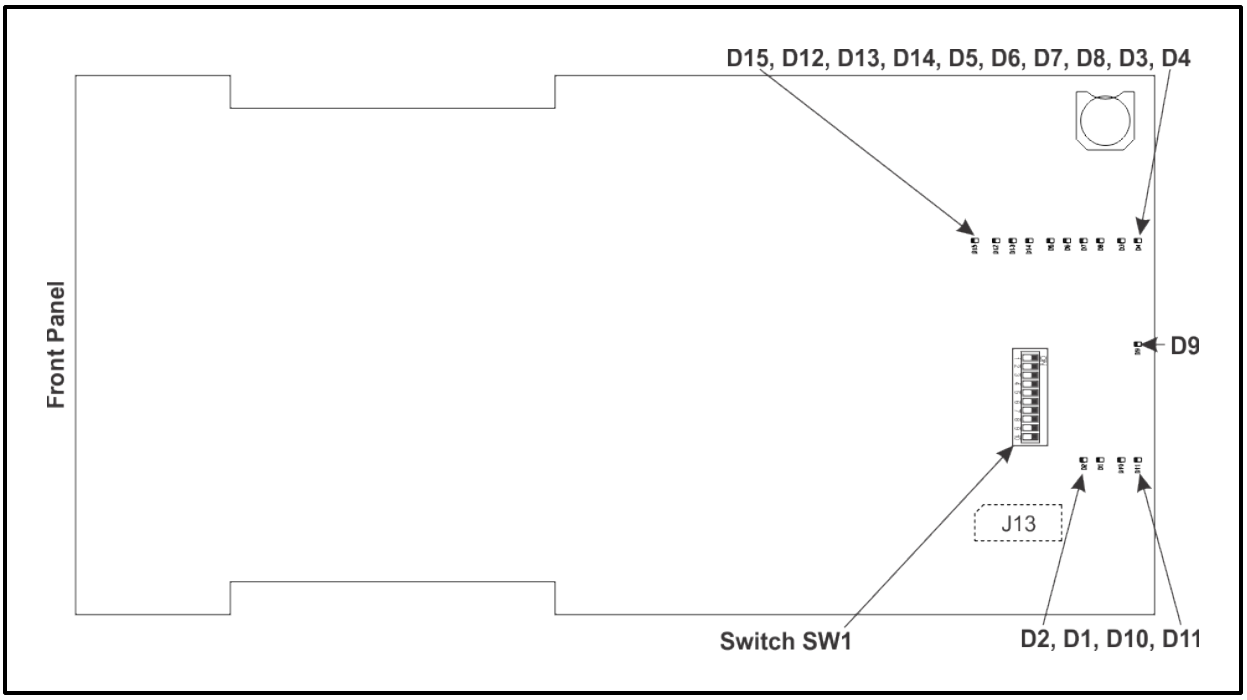
This section describes operating parameters that are set by DIP switch **SW1** on the Model 71861 main PCB (Pentek part number 320−71801 or 320−71802). As shipped from the factory, all switches are set in default positions on your board. The default operating parameters they select may or may not meet your requirements. Before installing your board, please review the default settings shown in the table below to determine whether you need to change any of these settings.

You should not change any switches that are not described in this section; those are reserved for factory test and setup purposes only.

Use a ballpoint tip only for setting DIP switches.
DO NOT USE paper clips, tweezers, or any other sharp objects, as they may damage the switch.

SW1 is located on the solder side of the main PCB, as shown in the drawing below, and is accessible while the heat sink is mounted on the PCB. (Refer to "PCB LEDs" on page 26 for a description of the LEDs identified below, and "JTAG Connector" on page 29 for a description of the JTAG connector **J13** shown below).

Main PCB, Solder Side



Switch **SW1** controls access to the FPGA configuration functions. The table below shows the settings for this switch.

SW1 – FPGA Configuration			
Switch	**Function**	**ON**	**OFF**
SW1–1	FLASH Memory Write Protect/Write Enable	Write Protected	Write Enabled *
SW1–2	FLASH Memory V_{PP}	Voltage Applied *	No Voltage
SW1–3	Select Boot Configuration at power on	See the table below.	
SW1–4			
SW1–5	PCIe Clock Select	XMC P15 Clock *	On–board Clock
SW1–6	P16 Clock Select	XMC P16 Clock	On–board Clock *
SW1–7	JTAG Source Select	XMC JTAG	Board JTAG *
SW1–8	JTAG Bypass (factory use only)[a]	Not Bypassed	Bypassed *
SW1–9	Not connected	–	–
SW1–10	User Spare	–	–
* Factory default settings **Note:** For Model 78861, JTAG Source Select will be set to ON (XMC JTAG) by default.			

FPGA Configuration Select – Switches SW1–3:4		
SW1–3	**SW1–4**	**Configuration Select (FLASH)**
ON *	ON *	Version 0 Boot Code – Gen 3 x8 PCIe
OFF	ON	Version 1 Boot Code
ON	OFF	Version 2 Boot Code
OFF	OFF	Version 3 Boot Code
* Factory default setting		

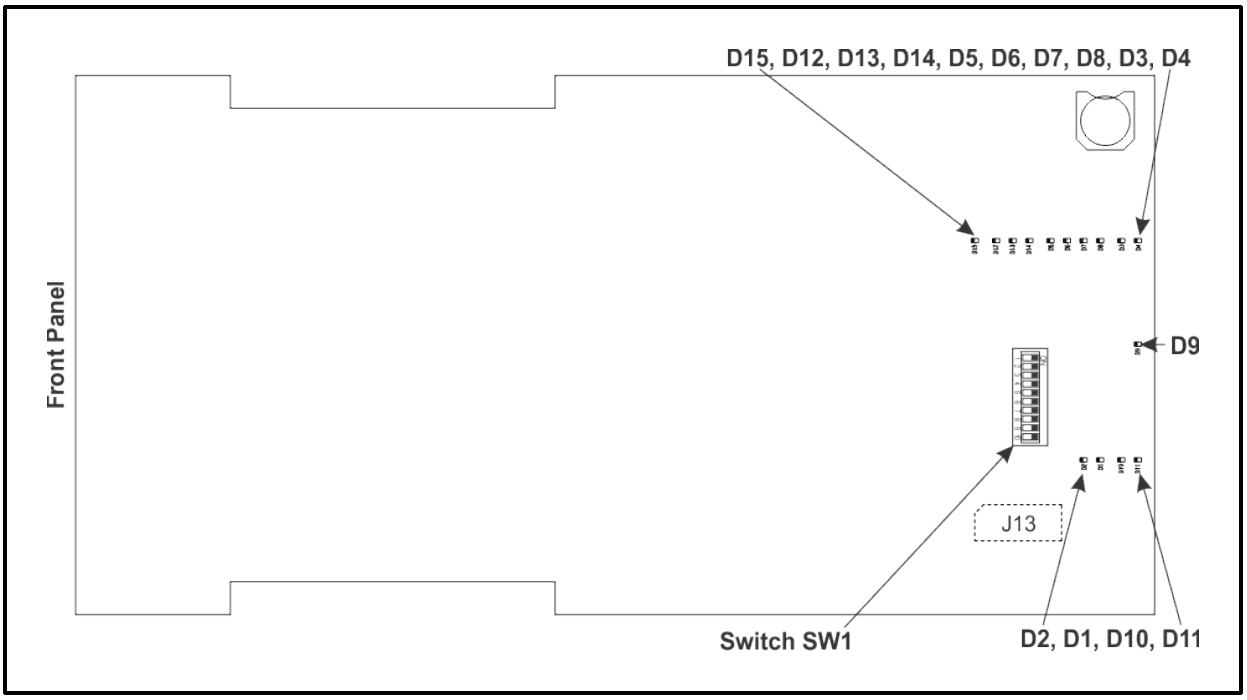
Model 71861 is shipped with a default FPGA configuration on FLASH memory, which is loaded at power–up. Up to four FPGA configurations can be stored in FLASH, identified as Version 0, Version 1, Version 2, and Version 3. The Pentek default FPGA configuration is located in the Version 0 space. The other three positions are empty.

The Pentek default FPGA configuration sets the PCIe interface to Gen 3 x8. However, the board can negotiate down to Gen 2 or Gen 1 x4, as needed.

[a]**SW1–8** (factory use only) selects whether all JTAG–linked components on the board are inserted into the JTAG chain or whether only the Kintex FPGA is in the JTAG chain. Only the Kintex can be user modified. Customers should maintain the factory setting of "bypassed". When not bypassed, JTAG activity may affect the PCIe link.

PCB LEDs

The PCB LEDs, labeled **Dnn**, are positioned on the solder side of the 71861 main PCB, as shown below. The use of each LED is indicated in the table below.



PCB LED Use							
LED	**Color**	**USE**					
D1	Green	Power supply sequencer done					
D2	Red	Power supply sequencer fault detected					
D3	Green	Kintex FPGA initialization complete					
D4	Red	Kintex FPGA initialization in progress					
D5	Green	Kintex PCIe link has been established					
D6 D7	Yellow	Kintex active lanes (LED0 = D6 and LED1 = D7):		x1	x2	x4	x8
			D6	Off	On	Off	On
			D7	Off	Off	On	On
D8	Green	Kintex P16 link has been established					
D9	Green	User−defined LED					
D10	Red	System monitor alarm					
D11	Red	Temperature alarm					
D12	Green	CDCM7005 VCXO is OK					
D13	Green	CDCM7005 reference clock is OK					
D14	Green	CDCM7005 is locked					
D15	Red	0.75 V (FPGA Core Power) power failure (LED is off if power is OK)					

Baseboard Connectors

The following sections describe the baseboard PMC/XMC connectors on the 71861 PCB.

XMC Connectors

Model 71861 provides an XMC high-speed serial connector, identified as **P15**, that complies with the VITA 42.3 XMC Switched Mezzanine Card Auxiliary Standard. This interface is configured as PCI Express Gen 3 x8.

Option 105 for the 71861 provides high-speed serial connections from FPGA spare pins using XMC connector **P16**. This connector complies with the VITA 42.0 XMC Standard and can support various interfaces including VITA 42.2 Serial RapidIO, VITA 42.3 PCI Express, or VITA 42.5 Aurora.

The table below identifies the FPGA to XMC **P16** pin connections.

Option 105 XMC P16 FPGA Pin Connections

Pin	A	B	C	D	E	F
01	S2_TD_P0	S2_TD_N0	n/c	S2_TD_P1	S2_TD_N1	n/c
02	GND	GND	n/c	GND	GND	n/c
03	S2_TD_P2	S2_TD_N2	n/c	S2_TD_P3	S2_TD_N3	n/c
04	GND	GND	n/c	GND	GND	n/c
05	S3_TD_P0	S3_TD_N0	n/c	S3_TD_P1	S3_TD_N1	n/c
06	GND	GND	n/c	GND	GND	n/c
07	S3_TD_P2	S3_TD_N2	n/c	S3_TD_P3	S3_TD_N3	n/c
08	GND	GND	n/c	GND	GND	n/c
09	n/c	n/c	n/c	n/c	n/c	n/c
10	GND	GND	n/c	GND	GND	n/c
11	S2_RD_P0	S2_RD_N0	n/c	S2_RD_P1	S2_RD_N1	n/c
12	GND	GND	n/c	GND	GND	n/c
13	S2_RD_P2	S2_RD_N2	n/c	S2_RD_P3	S2_RD_N3	n/c
14	GND	GND	n/c	GND	GND	n/c
15	S3_RD_P0	S3_RD_N0	n/c	S3_RD_P1	S3_RD_N1	n/c
16	GND	GND	n/c	GND	GND	n/c
17	S3_RD_P2	S3_RD_N2	n/c	S3_RD_P3	S3_RD_N3	n/c
18	GND	GND	n/c	GND	GND	n/c
19	XMC_REFCLK1_P	XMC_REFCLK1_N	n/c	n/c	n/c	n/c

Sn_TD_Pm, Sn_TD_Nm = Serial Transmit, FPGA Auxiliary Port n, lane m
Sn_RD_Pm, Sn_RD_Nm = Serial Receive, FPGA Auxiliary Port n, lane m

PMC Connector (Option 104)

Option 104 for Model 71861 provides connections from FPGA spare pins to the baseboard or carrier using PMC connector **P14**. These connections are programmed for low−voltage differential signals (LVDS) in the default FPGA configuration; you can reconfigure these pins with custom FPGA programming (see "Navigator FPGA Design Kit (FDK)" on page 13).

The P14 signals can be configured in the FPGA as either LVDS (the default) or LVCMOS, but in either case are limited to 2.5V, and also cannot be driven with a negative voltage.

The table below identifies the LVDS signals that are connected from the FPGA to the PMC **P14** connector pins.

Option 104 PMC FPGA Pin Connections

FPGA Signal	PMC P14 Pin	FPGA Signal	PMC P14 Pin
P14_DATA_N0	2	P14_DATA_N16	1
P14_DATA_P0	4	P14_DATA_P16	3
P14_DATA_N1	6	P14_DATA_N17	5
P14_DATA_P1	8	P14_DATA_P17	7
P14_DATA_N2	10	P14_DATA_N18	9
P14_DATA_P2	12	P14_DATA_P18	11
P14_DATA_N3	14	P14_DATA_N19	13
P14_DATA_P3	16	P14_DATA_P19	15
P14_DATA_N4	18	P14_DATA_N20	17
P14_DATA_P4	20	P14_DATA_P20	19
P14_DATA_N5	22	P14_DATA_N21	21
P14_DATA_P5	24	P14_DATA_P21	23
P14_DATA_N6	26	P14_DATA_N22	25
P14_DATA_P6	28	P14_DATA_P22	27
P14_DATA_N7	30	P14_DATA_N23	29
P14_DATA_P7	32	P14_DATA_P23	31
P14_DATA_N8	34	not connected	33
P14_DATA_P8	36	not connected	35
P14_DATA_N9	38	not connected	37
P14_DATA_P9	40	not connected	39
P14_DATA_N10	42	not connected	41

Option 104 PMC FPGA Pin Connections			
FPGA Signal	**PMC P14 Pin**	**FPGA Signal**	**PMC P14 Pin**
P14_DATA_P10	44	not connected	43
P14_DATA_N11	46	not connected	45
P14_DATA_P11	48	not connected	47
P14_DATA_N12	50	not connected	49
P14_DATA_P12	52	not connected	51
P14_DATA_N13	54	not connected	53
P14_DATA_P13	56	not connected	55
P14_DATA_N14	58	not connected	57
P14_DATA_P14	60	not connected	59
P14_DATA_N15	62	not connected	61
P14_DATA_P15	64	not connected	63

JTAG Connector

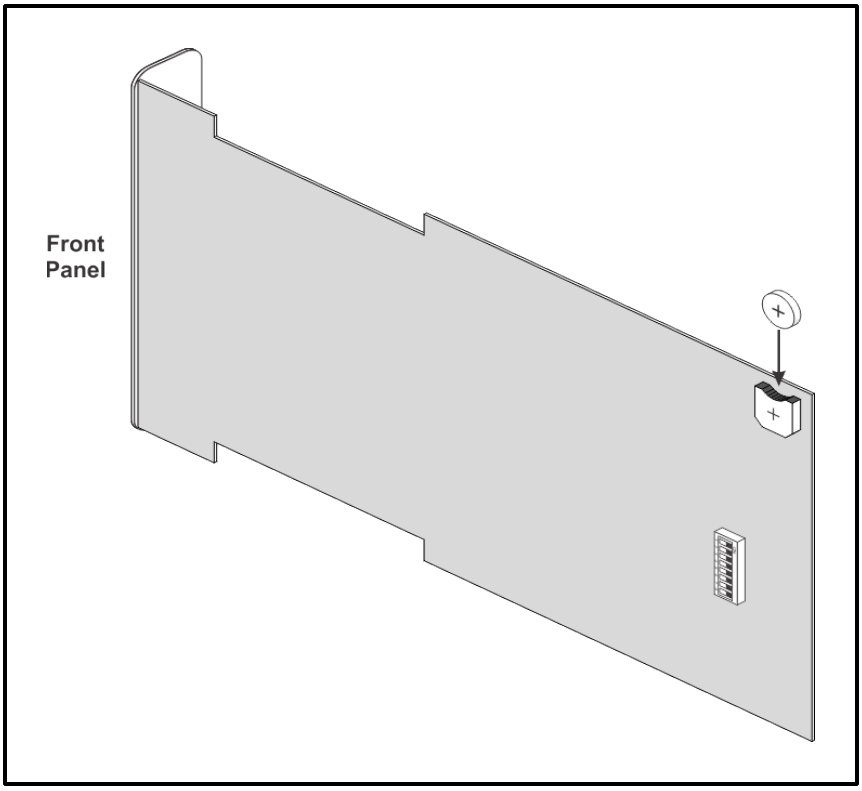
The Model 71861 PCB **J13** JTAG connector provides an interface to download programs and to perform boundary−scan tests on 71861 devices. This connector is located on the solder side of the Model 71861 main PCB (Pentek part number 320−71801 or 320−71802), as illustrated in "Main PCB, Solder Side" on page 24.

The table below gives the pinout for this 10−pin header.

Pentek JTAG J13 Connector				
Signal	**Pin Number**		**Pin Number**	**Signal**
GND	1	1 2 3 4 5 6 7 8 9 10	2	+3.3 V
GND	3		4	TMS
GND	5		6	TCK
GND	7		8	TDO
GND	9		10	TDI

Battery Installation

Your Model 71861 shipment includes a battery in a separate package, identified as part number 174.50010. If you plan to use the Kintex FPGA bitstream encryption capability, such as with Pentek's Navigator FDK, the battery must be installed on the solder side of the main PCB (part number 320−71801 or 320−71802) as shown in the drawing below. Ensure that the battery positive terminal is facing the outside of the battery holder.



Perform all assembly steps at an antistatic workstation.

Model 52861 (Model 71861 on a Pentek Model 5201 3U VPX carrier) and Model 53861(Model 71861 on a Pentek Model 5306 3U VPX carrier) are shipped with the battery already installed because the battery cannot be installed without removing the Model 71861 XMC from the VPX carrier.

Installing the XMC Module on an XMC Baseboard

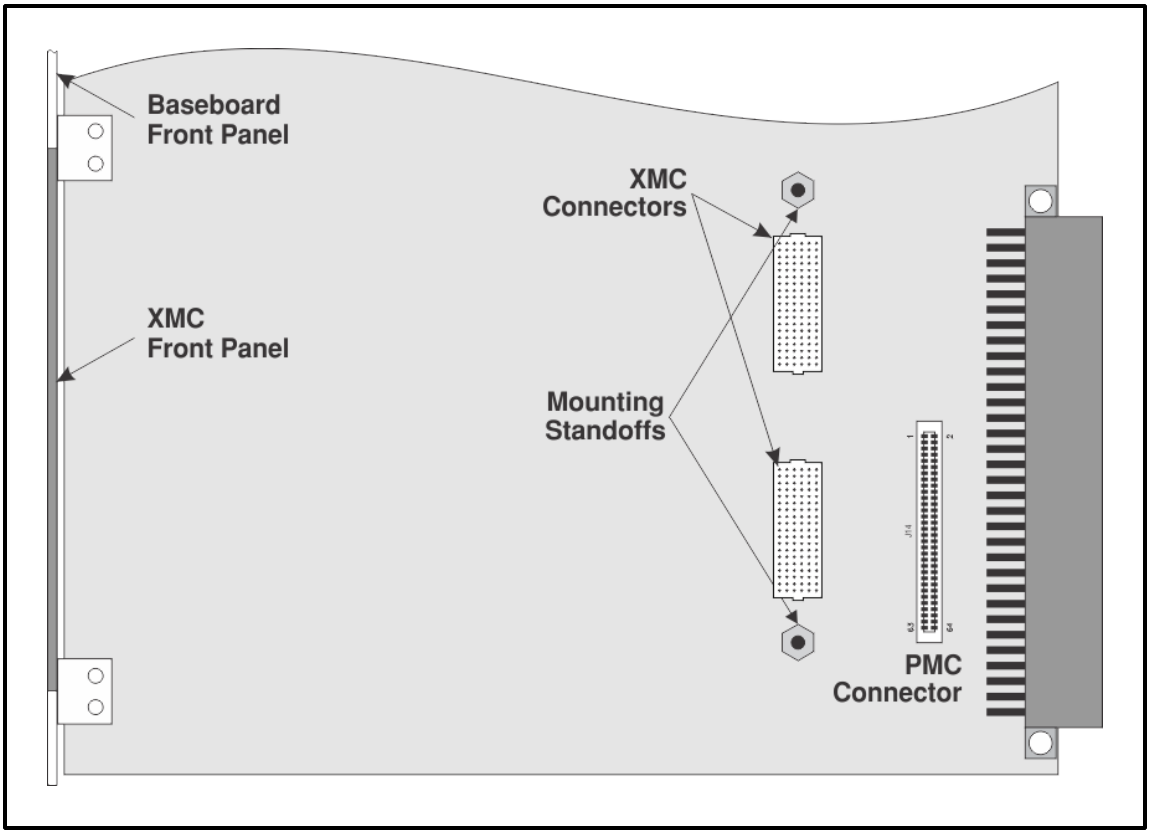
Model 71861 mounts on the connector side of an XMC baseboard or carrier. Refer to the operating manual supplied with your baseboard for any specific mounting instructions. A typical XMC baseboard is shown below.

Minimum System Requirements: The system in which you install this Pentek product should have the latest Intel® Core™ i7 processor with a minimum RAM of 8 GB. PCIe Gen 3 x8 is required.

REMOVE POWER to the XMC baseboard before installation!

The Model 71861 requires both a 3.3V and a 5V or 12V power supply (12V is recommended). Ensure that the XMC baseboard or carrier you are using has both a 3.3V and a 5V or 12V power supply.

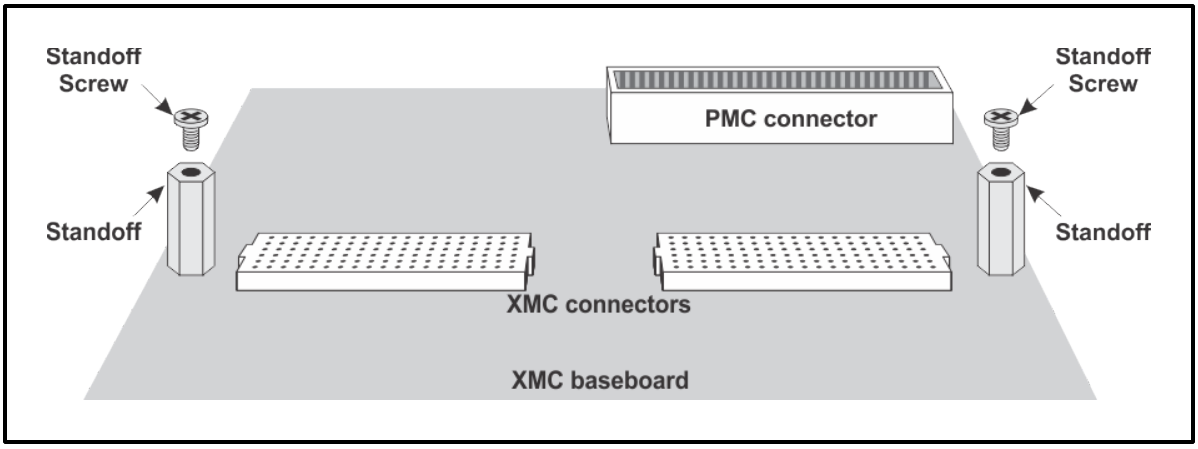
Typical XMC Baseboard



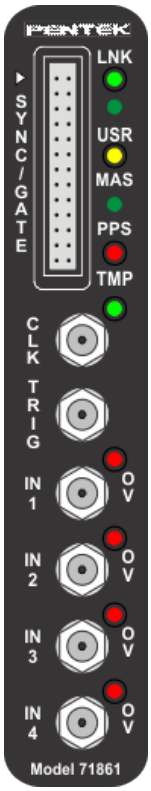
Installation Instructions

1. Attach an ESD strap to your wrist—attach the other end to a ground source. The ESD strap must be secured both to your wrist and to ground throughout the procedure.
2. Pentek XMC baseboards are supplied with module standoffs and mounting screws installed. Ensure that the standoffs on your baseboard are installed at the locations shown in the drawing below and in the Typical XMC Baseboard drawing above.
3. Remove the blank module front panel from the front panel of the XMC baseboard (see the Typical XMC Baseboard drawing, above).
4. Position the Model 71861 front panel into the opening from behind the baseboard front panel, and position the module so that the 71861 XMC connectors are over the XMC connectors on the baseboard (see the Baseboard PMC/XMC Connections drawing, below).

Baseboard PMC/XMC Connections



5. **GENTLY but firmly**, press down on the 71861 board opposite the connectors to fully seat the board's connectors into the baseboard. The connectors on the underside of the 71861 PCB should connect smoothly with the corresponding connectors on the baseboard.
6. Using two flat-head Phillips standoff screws (supplied with the 71861), secure the Model 71861 PCB, through the PCB's standoff holes, to the baseboard's standoffs (see the Baseboard PMC/XMC Connections drawing, above).



Front Panel Connections

The Model 71861 XMC front panel, shown in the drawing on the left, includes six SSMC coaxial connectors for clock, trigger, and analog input signals, and a 26- pin Sync Bus input/output connector. These connectors are described below.

The front panel also includes ten LED indicators, which are described in "Front Panel LEDs" on page 36.

Clock Input Connector

The front panel has one SSMC coaxial connector, labeled **CLK**, for input of an external sample clock. The external clock signal must be a sine wave or square wave of +0 dBm to +10 dBm, with a frequency range from 10 to 800 MHz.

This external clock input can be used as the sample clock signal for the A/D converters. The program−selected clock source is input to a CDCM7005 Clock Synthesizer that generates five separate output clocks, each programmable as sub−multiples of the input frequency. One of the CDCM7005 output clocks (Y0) provides the sample clock for the ADS5485 A/D converters.

When greater than 200 MHz, the input clock must be divided down by the CDCM7005 for the ADC sample clock.

Take care that the ADC clock output from the CDCM7005 never exceeds the ADS5485's rated clock speed during any change of frequency with the VCXO and/or the CDCM7005.

− If you are increasing the VCXO frequency, first adjust the appropriate CDC divider so that the ADS5485 clock does not exceed 200 MHz.

− If you are decreasing the VCXO frequency, do not adjust the CDC divider until the VCXO has been reprogrammed so that the ADS5485 clock does not exceed 200 MHz.

Trigger Input Connector

The front panel has one SSMC coaxial connector, labeled **TRIG**, for input of an external trigger. The external trigger signal must be an LVTTL signal.

The front panel **TRIG** input is 5V tolerant but it must NOT have any negative voltage applied. It is terminated with a 392−ohm resistor to 3.3V and a 332−ohm resistor to ground.

The trigger input can be used as a gate or trigger for A/D signal processing.

Analog Signal Input Connectors

The front panel has four SSMC coaxial connectors for analog signal inputs, labeled **IN 1**, **IN 2**, **IN 3**, and **IN 4**, one for each ADS5485 A/D converter.

Each analog input signal has a full−scale level of +8 dBm. Each input drives an RF transformer with 50−ohm input impedance.

Sync Bus Connector

The 26−pin Sync Bus front panel connector, labeled **SYNC/GATE**, provides clock, sync, and gate input/output pins for the Low−Voltage Positive Emitter−Coupled Logic (LVPECL) Sync Bus. When Model 71861 is a bus Master, these pins output LVPECL Sync Bus signals to other slave units. When Model 71861 is a bus Slave, these pins input LVPECL signals from a bus Master. This connector also accepts two Low−Voltage TTL (LVTTL) Gate/Sync inputs.

The table below shows the **SYNC/GATE** connector pin configuration. The mating 26−pin connector is Pentek part # 353.02607 (Model 2140−998).

SYNC/GATE Connector Pins

Signal	Pin		Pin	Signal
LVTTL GATE/TRIG	B1	B1 ▶ ● ● A1	A1	GND
LVTTL SYNC/PPS	B2	B2 ● ● A2	A2	GND
LVPECL GATE−	B3	B3 ● ● A3	A3	LVPECL GATE+
GND	B4	B4 ● ● A4	A4	GND
LVPECL SYNC−	B5	B5 ● ● A5	A5	LVPECL SYNC+
GND	B6	B6 ● ● A6	A6	GND
LVPECL CLK−	B7	B7 ● ● A7	A7	LVPECL CLK+
GND	B8	B8 ● ● A8	A8	GND
Spare	B9	B9 ● ● A9	A9	Spare
GND	B10	B10 ● ● A10	A10	GND
Spare	B11	B11 ● ● A11	A11	Spare
GND	B12	B12 ● ● A12	A12	GND
Spare	B13	B13 ● ● A13	A13	Spare

NOTE

When connecting LVPECL Sync Bus pins to additional Model 71861 modules, the LVPECL pins on the LAST unit must be terminated. Pentek includes a terminating board (part # 004.71504, Model # 2140−999) with your shipment for this purpose.

NOTE

The LVTTL GATE/TRIG and SYNC/PPS signals are 5V tolerant but they must NOT have any negative voltage applied. They are terminated with a 392−ohm resistor to 3.3V and a 332−ohm resistor to ground.

Front Panel LEDs

The Model 71861 XMC front panel has ten LED indicators, as shown in the drawing in "Front Panel Connections" on page 33.

Link LED

The green **LNK** LED indicates the link speed when a valid link has been established over the PCIe interface, as follows:

- Gen 1 – **LNK** LED will blink slowly (less than once per second)
- Gen 2 – **LNK** LED will blink approximate once per second
- Gen 3 – **LNK** LED will be constantly on

User LED

The green **USR** LED is for user applications.

Master LED

The yellow **MAS** LED illuminates when this 71861 is the Sync Bus Master. When only a single 71861 is used, it must be a Master.

PPS LED

The green **PPS** LED illuminates when a valid PPS signal is detected. The LED will blink at the rate of the PPS signal.

Over Temperature LED

The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the 71861 PCB.

Clock LED

The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.

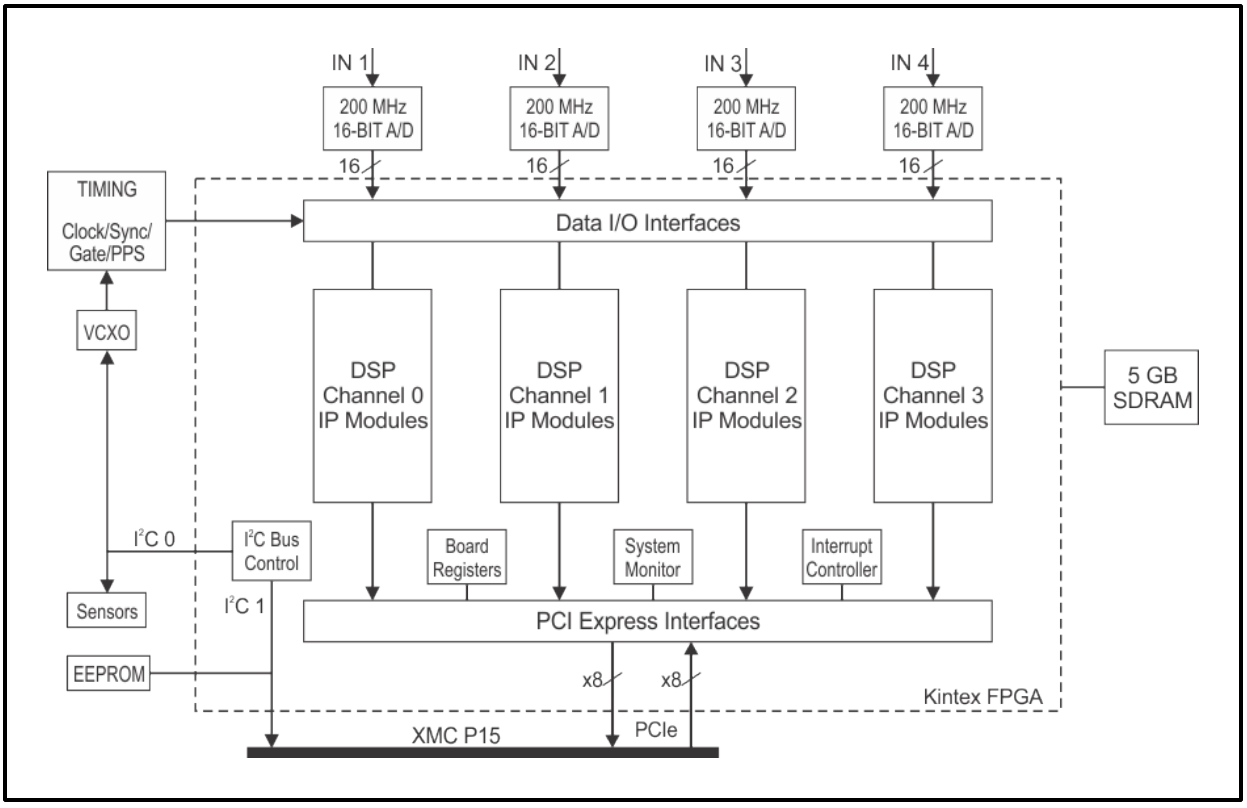
ADC Overload LEDs

There are four red **OV** LEDs, one for each A/D input. Each LED indicates either an overload detection in the associated ADS5485, or an ADC FIFO overrun.

Chapter 3: Hardware Resource Operation

Overview

This chapter describes operation of the Model 71861 hardware resources. The block diagram below shows the overall data flow of the 71861.



The functional blocks in the diagram are described in the sections that follow.

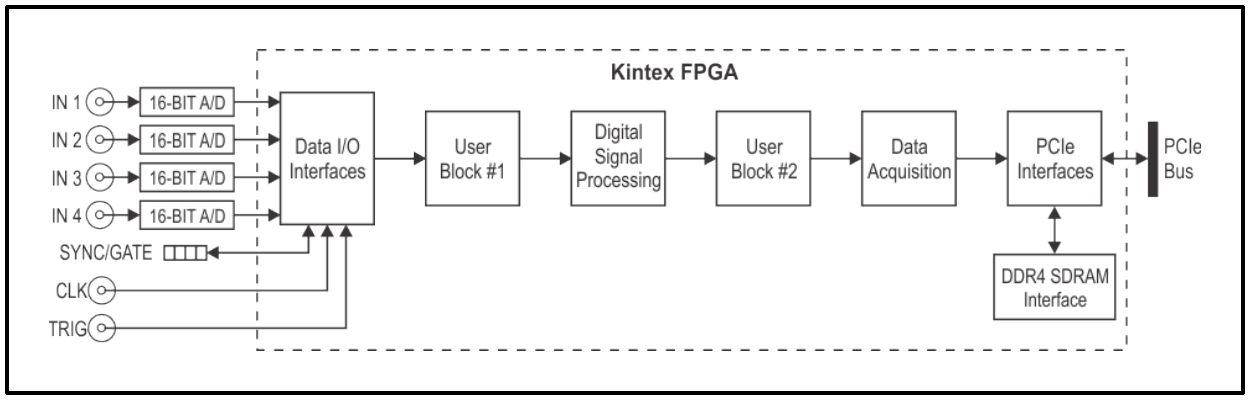
Refer to "FPGA IP Core Operation" on page 51 for a description of the FPGA IP Core modules data processing.

Analog to Digital Input

Model 71861 accepts four analog RF inputs on front panel SSMC connectors, labeled **IN 1**, **2**, **3**, and **4** (see "Front Panel Connections" on page 33). Each input is transformer coupled, digitized by a Texas Instruments ADS5485 200−MHz, 16−bit A/D converter (ADC), and then routed to the FPGA for processing by the IP Core modules.

The processed data can be read through the PCIe interface using input DMA engines.

The simplified block diagram below shows the analog to digital input data flow.



Refer to "FPGA IP Core Operation" on page 51 for a description of each of the top−level functional blocks of the FPGA IP code.

Refer to the TI ADS5485 datasheet (see "Supporting Documentation" on page 17) for a description of ADS5485 operation.

Timing and Synchronization

The Model 71861 front panel Sync Bus Connector provides clock, sync, PPS, and gate input/output signals. The front panel also has two coaxial SSMC connectors for input of an external sample clock and an external gate/trigger.

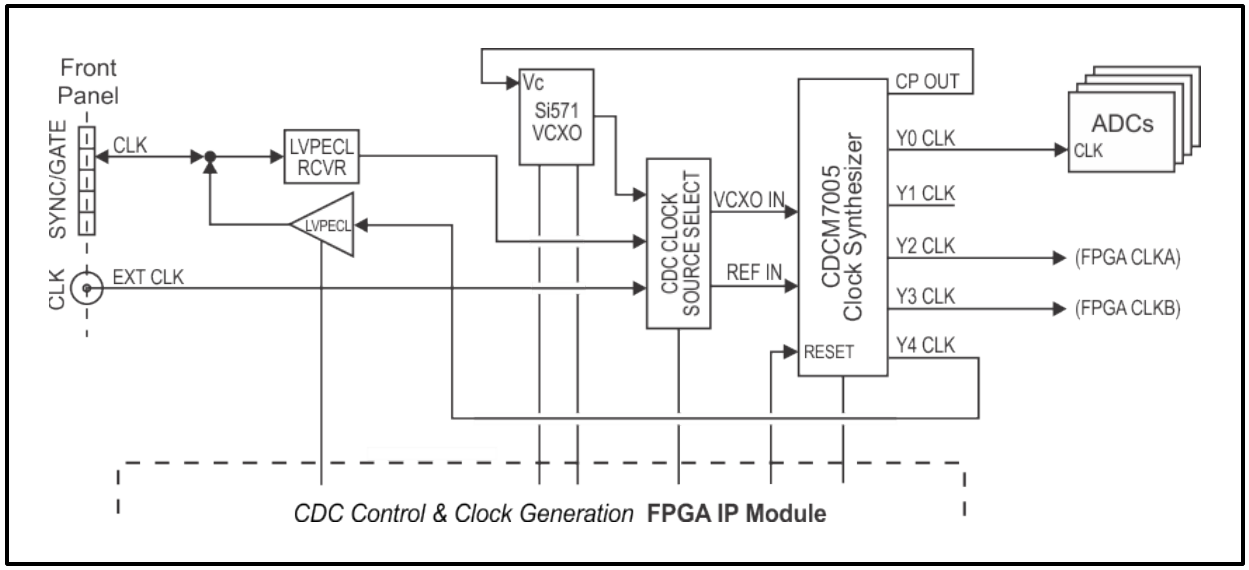
The front panel interface allows one Model 71861 to act as a Master, driving the clock, sync, and/or gate signals to the Sync Bus. Up to three Slave 71861s can be driven by the Sync Bus, supporting synchronous sampling and sync functions across all connected boards. If more than four boards need to be synchronized, Pentek's Model 7893 Clock Generator allows synchronization of up to eight boards. Note that the Model 7893 is a PCIe board.

Clocks

Model 71861 clocks can be selected from the front panel Sync Bus LVPECL CLK input (see "Front Panel Connections" on page 33), the front panel SSMC CLK input (see "Clock Input Connector" on page 33), or the onboard Si571 VCXO. The selected clock source is input to a CDCM7005 Clock Synthesizer that generates five output clocks, each independently programmable. CDCM7005 clock Y0 provides the sample clock for the four ADS5485 ADCs, and clock Y2 provides FPGA CLK for ADC data processing in the FPGA.

When the Model 71861 is a Clock Master, CDCM7005 clock Y4 is output to the CLK pins of the Sync Bus (see "Front Panel Connections" on page 33).

The drawing below illustrates the clock logic. Use the CDCM7005 Control & Clock Generation FPGA IP Core modules to control these clock signals.

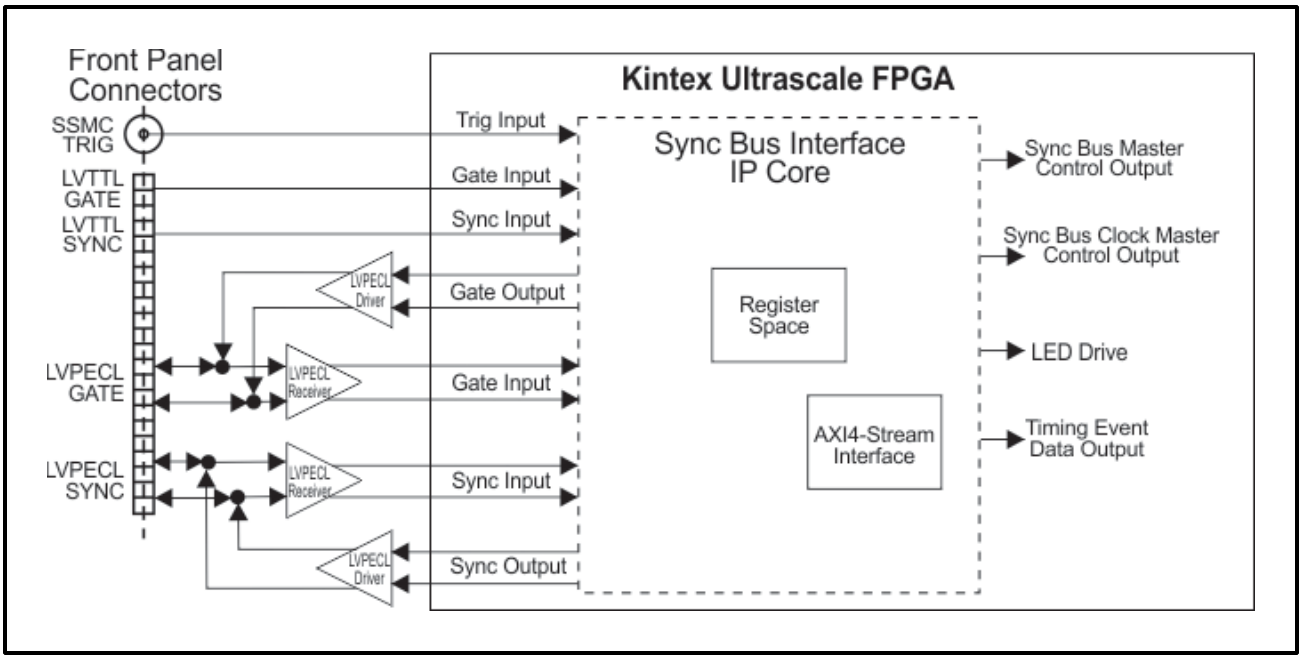


Sync Bus

Model 71861 provides SYNC, GATE, and PPS signals for ADC and user applications. These signals can be driven from the front panel Sync Bus connector LVPECL or TTL inputs (see "Front Panel Connections" on page 33), the front panel TRIG SSMC connector input (see "Trigger Input Connector" on page 33), or a Gate/Sync/PPS Generate Register write.

When Model 71861 is a Sync/Gate Master, a Generate Register write, Sync Bus TTL input, or TRIG input signal is output to the Sync Bus LVPECL SYNC or GATE pins.

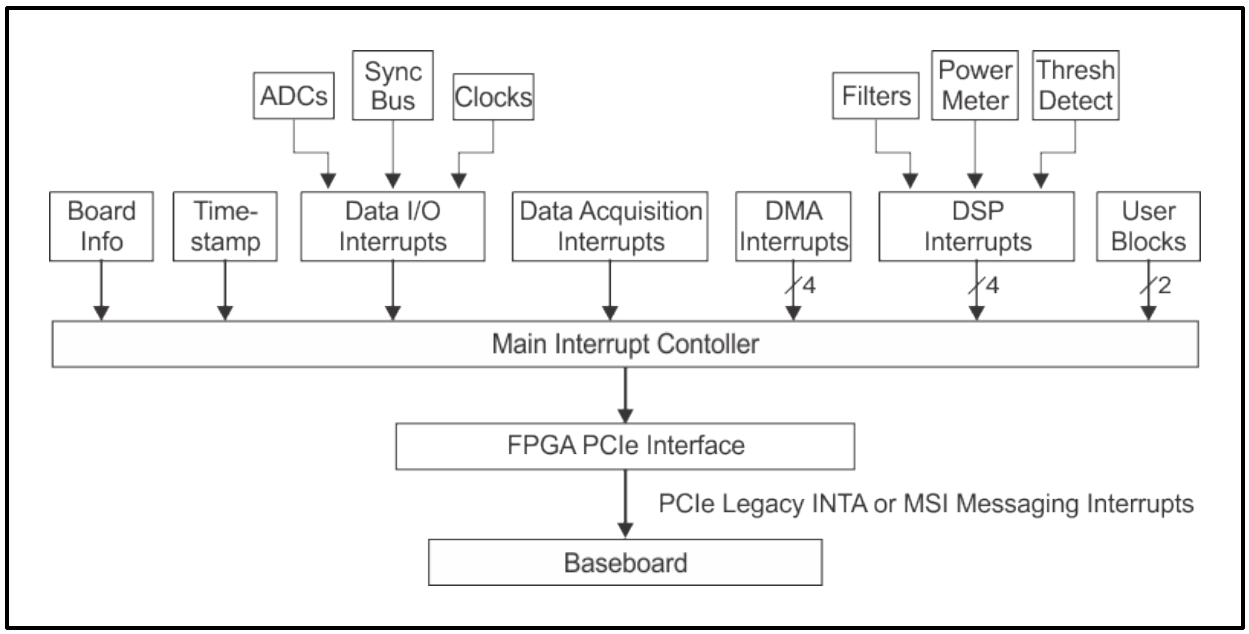
The diagram below illustrates the sync bus logic. Use the Sync Bus Interface FPGA IP Core module to control these signals.



Interrupt Operation

The Model 71861 XMC can generate INTA interrupts in legacy mode or MSI interrupts. Refer to the Operating Manual supplied with your XMC baseboard for a description of the board's interrupt response operation.

The block diagram below illustrates the interrupt signal routing on Model 71861.



Interrupt events are edge−detected and latched in second−level interrupt flag registers. In addition, the interrupt sources are also routed to dynamic interrupt status registers. The interrupt edges from various sources can be individually enabled by interrupt enable registers and then OR'ed per system module to form sources to the first−level interrupt flag register where the event is latched. Enable bits in the first−level interrupt enable register can individually enable each module's flag, which are then OR'ed together for a single level interrupt input to the PCIe interface.

Clearing an interrupt in the first−level interrupt flag register will turn off the interrupt. The sources are still latched in the second−level flag register but a new interrupt will not be asserted even if the source is still present until the second−level flag is cleared and the logic subsequently detects a new edge.

Use the Interrupt Controller FPGA IP Core module to control the FPGA PCIe interface interrupt signals.

FPGA System Monitor

The Kintex FPGA System Monitor measures several board power supplies and FPGA on-chip voltages. The "System Monitor Measurement Ports" below table below lists the parameters measured by the System Monitor measurement ports and the required multiplication factors to apply to the readings (System Monitor ports VAUX5 to VAUX7 are not used in the Model 71861).

System Monitor Measurement Ports		
Port	**Parameter Measured**	**Measurement Scaling**
VAUX0	VPWR (5 or 12V)	Voltage = VoltageReading x 14
VAUX1	3.3V	Voltage = VoltageReading x 4
VAUX2	1.2V MGT	Voltage = VoltageReading x 2
VAUX3	1.8V	Voltage = VoltageReading x 3
VAUX4	2.5V	Voltage = VoltageReading x 3
VAUX8	3.6V	Voltage = VoltageReading x 4
VAUX9	6V	Voltage = VoltageReading x 14
VAUX10	1.8V MGT	Voltage = VoltageReading x 3
VAUX11	1.0 MGT	Voltage = VoltageReading x 2
VAUX12	0.95V Core	Voltage = VoltageReading x 2

Use the System Monitor FPGA IP Core module to access these measurement ports.

I2C Bus Controllers

The Kintex FPGA provides two I^2C serial buses, described in the following subsections:

I2C Bus 0

I^2C Bus 0 is used to control several sensors and on−board clocks. Each I^2C bus device has a separate bus address, listed in the "I2C Port 0 Bus Addresses" below table below. Refer to the information identified in the table below for a description of the device's use in the 71861. Refer to a device's datasheet (see "Supporting Documentation" on page 17) for a description of the device's programmable registers. Use the I2C Port 0 FPGA IP Core module to access these devices.

I2C Port 0 Bus Addresses

Device	Address *	Information
Main PCB LM95234 Temperature Sensor	**0011000h**	Main PCB M95234 Temperature Sensor
Front Panel Module LM83 Temperature Sensor	**0011001h**	Front Panel Module LM83 Temperature Sensor
Main PCB LTC2990 Voltage Monitor	**1001100h**	Main PCB LTC2990 Voltage Monitor
Main PCB Si571 Programmable VCXO	**1100000h**	Si571 Programmable VCXO
Main PCB Silicon Labs Si5341B Clock Generator	**1110100h**	Si5341B AnyRate Clock Generator

* The bus addresses are 7−bit serial bus address, followed by the bus R/W bit **h**: 0 = Write, 1 = Read.

Main PCB M95234 Temperature Sensor

The LM95234 measures component temperatures on the 71861 main PCB, and provides an alarm when any exceeds its programmable limit. The table below lists the LM95234 sensor inputs:

Main PCB LM95234 Programmable Sensors		
Monitored Condition	**LM95234 Input**	**Navigator Limits ***
FPGA temperature	1	100° C
Power Supplies	2	60° C
Power Supplies	3	60° C
CDCM7005	4	60° C
LM95234 Local	(internal)	50° C
* These limits are programmed if you run the Pentek Navigator 71861 Hardware Monitor routines for the LM95234 using the default values.		

When any of the inputs exceeds the high setpoint limit, a red LED on the main 71861 PCB is illuminated (see "PCB LEDs" on page 26).

Front Panel Module LM83 Temperature Sensor

The LM83 measures component temperatures on the 71861 front panel module PCB, and provides an alarm when any exceeds its programmable limit. The table below lists the LM83 programmable sensor inputs:

Front Panel LM83 Programmable Sensors		
Monitored Condition	**LM83 Input**	**Navigator Limits ***
Near ADC0	1	85° C
Near ADC3	2	85° C
Near ADC1 & 2	3	85° C
LM83 Local	(internal)	85° C
* These limits are programmed if you run the Pentek Navigator 71861 Hardware Monitor routines for the LM83 using the default values.		

When any of the inputs exceeds the high setpoint limit, a red LED on the main 71861 PCB is illuminated (see "PCB LEDs" on page 26).

Main PCB LTC2990 Voltage Monitor

The Linear Technology LTC2990 voltage, current, and temperature monitor measures main PCB voltage. Two voltage inputs are required for monitoring power, so the Navigator software is configured for two inputs for 12V and two inputs for 3.3V. The table below lists the inputs on the LTC2990:

Main PCB LTC2990 Inputs		
Monitored Condition	**LTC2990 Input**	**Navigator Limits ***
12V / 5V voltage	V1	High Limit = 12.60 V / 5.25 V Low Limit = 11.40 V / 4.75 V
12V / 5V voltage	V3	
3.3V voltage	V2	High Limit = 3.465 V Low Limit = 3.135 V
3.3V voltage	V4	
* These limits are programmed if you run the Pentek Navigator 71861 Hardware Monitor routines for the LTC2990 using the default values.		

Si571 Programmable VCXO

The Silicon Labs Si571 programmable Any−Rate VCXO generates the on−board clock for the CDCM7005 Clock Synthesizer. The Si571 output frequency is determined by programming the oscillator frequency and the output dividers using onboard registers. The default VCXO frequency output is set for 200 MHz.

Take care that the ADC clock output from the CDCM7005 never exceeds the ADS5485's rated clock speed during any change of frequency with the VCXO and/or the CDCM7005.

− If you are increasing the VCXO frequency, first adjust the appropriate CDC divider so that the ADS5485 clock does not exceed 200 MHz.

− If you are decreasing the VCXO frequency, do not adjust the CDC divider until the VCXO has been reprogrammed so that the ADS5485 clock does not exceed 200 MHz.

Si5341B AnyRate Clock Generator

The Si5341B creates the FPGA Configuration clock, FPGA 200MHz Reference Clock, FPGA **P16** Gigabit IO clock, DDR4 controller reference clock, and an optional 100MHz PCIe clock when no host clock is available. The following Si5341B outputs are used in the Model 71861 (**OUT1**, **OUT3**, and **OUT6** are not used):

Clock	71861 Use	Default
OUT0	PCIe Clock	100 MHz
OUT2	DDR4 Controller Reference Clock	240.096 MHz
OUT4	FPGA Reference Clock	200 MHz
OUT5	FPGA P16 Gigabit IO clock	156.25 MHz
OUT7,8	FPGA Configuration Clock	100 MHz
OUT9	Auxiliary FPGA Clock − available for custom FPGA design	100 MHz

Only the FPGA P16 Gigabit IO clock (OUT5) or Auxiliary FPGA Clock (OUT9) should ever be changed. FPGA P16 Gigabit IO clock defaults to 156.25 MHz, used by 10GE or some Aurora frequencies.

I2C Bus 1

I^{2}C bus 1 is connected to the XMC **P15** connector **MSDA** (I^{2}C bus serial data) and **MSCL** (I^{2}C bus serial clock) pins, and provides access to the on−board serial EEPROM. The serial EEPROM is used for Jade board identification.

The serial EEPROM is connected to the XMC interface at I^{2}C address **0xAn** (binary address **0b1010nnn**). The last three bits of the EEPROM I^{2}C address (**nnn**) are determined by the XMC GA[0:2} inputs, from the **MGAn** pins. The serial EEPROM MGA address is set to binary 000.

The contents of the EEPROM are shown in the "EEPROM Format" on the next page table below, organized as 32−bit words.

- The first 32 32−bit words (addresses **0x0000** to **0x00FF**) contain XMC and PCIe information as defined by the ANSI/VITA 42.0−2008 and ANSI/VITA 42.3−2006 standards.
- The next word is a valid data flag (**0x00EECODE**).
- Following the valid data word is the Jade board model number (7186 is shown in the "EEPROM Format" on the next page table).
- Next are words containing the PCB number, revision, and options for the main 71861 PCB, for the front end I/O module, and for each memory bank installed on your product. Where options are not installed, the 16−bit Option field is set to **0xFFFF**.
- If you have ordered a Jade assembly on a Pentek−supplied PCIe or VPX carrier (such as a Model 78861 PCIe board or Model 52861 VPX board), the next three 32−bit words identify the carrier PCB number, revision, and options for the carrier.
- The last word is a checksum of all 32−bit words, calculated by Pentek.

Use the I2C Port 1 IP Core module to access the EEPROM.

Do NOT write to this EEPROM.

Pentek programs the contents of the serial EEPROM to identify the model of the board and all options installed by Pentek.

If you write to the EEPROM you risk destroying this inform−ation.

The table below shows the format of the serial EEPROM.

EEPROM Format		
EEPROM Byte Address	**Contents**	**Comments**
0x0000	**0x00000300**	Base Definition Subtype, Version ANSI/VITA 42.3, Module Size: Single Wide
0x0004	**0x00002000**	VITA 42.1, 5W @ 3.3V, 0W @ 12V, 0W @ −12W
0x0008	**0x000C5C00**	20W @ 5V (VPWR), 20W @12V (VPWR), LINK 0 Protocol, LINK 0 Protocol
0x000C	**0x0000000C**	LINK 1 Protocol, LINK 1 Protocol
0x0010 – 0x00FC	**0xFFFFFFFF**	Reserved
0x0100	**0x00EEC0DE**	Valid data word
0x0104	**0x71860000**	Model Number
0x0108	**0x01234567**	Main PCB Number
0x010C	(unsigned int) 'A'	Main Assembly Revision
0x0110	**0x00020001**	Option 2, Option 1
0x0114	**0x00040003**	Option 4, Option 3
0x0118	**0x00060005**	Option 6, Option 5
0x011C	**0x00080007**	Option 8, Option 7
0x0120	**0x000A0009**	Option 10, Option 9
0x0124	**0x01234567**	Front End PCB Number
0x0128	(unsigned int) 'A'	Front End Assembly Revision
0x012C	**0x00020001**	Option 2, Option 1
0x0130	**0x00004567**	Memory Module 1 PCB Number
0x0134	(unsigned int) 'A'	Memory Module 1 Assembly Revision
0x0138	**0x00020001**	Option 2, Option 1
0x013C	**0x00004567**	Memory Module 2 PCB Number
0x0140	(unsigned int) 'A'	Memory Module 2 Assembly Revision
0x0144	**0x00040003**	Option 2, Option 1
0x0148	**0x03456789**	Pentek Carrier PCB Number
0x014C	(unsigned int) 'A'	Pentek Carrier Assembly Revision
0x0150	**0x00020001**	Option 2, Option 1
0x0154 – 0x01F8	**0xFFFFFFFF**	Reserved
0x01FC	**0x--------**	Checksum

RAM Memory Operation

Five GigaBytes of DDR4 (Double Data Rate 4th Generation) SDRAM are available to the Model 71861 Kintex FPGA. This memory is not used by the Pentek-supplied FPGA IP Code. Custom user-installed functions within the FPGA can take advantage of the memory for many purposes.

Use the DDR4 SDRAM Access FPGA IP Core module to access this memory.

FLASH Memory Operation

A 128-MByte bank of FLASH memory is provided for processing FPGA boot code. Up to four FPGA boot configurations can be stored in FLASH, identified as Version 0, Version 1, Version 2, and Version 3. Version 0 is the Pentek-supplied default boot configuration (0 is the Gen 3 x8 PCIe code) and Versions 1, 2 and 3 are reserved for user-defined configurations.

At power-up, PCB switches **SW1-3:4** designate which one of the FPGA configurations to boot from FLASH, as indicated in "DIP Switch Settings" on page 24.

FLASH memory is write-protected using PCB switch **SW1-1**. See "DIP Switch Settings" on page 24 for these switch settings.

The table below shows the allocation of FLASH memory.

FLASH Memory Use	
FLASH Boot Code	**Default Configuration Storage**
Version 0 Boot Code	Gen 3 x8 PCIe (Pentek-supplied)
Version 1 Boot Code	Reserved
Version 2 Boot Code	Reserved
Version 3 Boot Code	Reserved
The Versions 1, 2, and 3 Boot Code storage areas are blank as shipped from the factory.	

Use the Configuration Flash Access FPGA IP Core module to access FLASH memory.

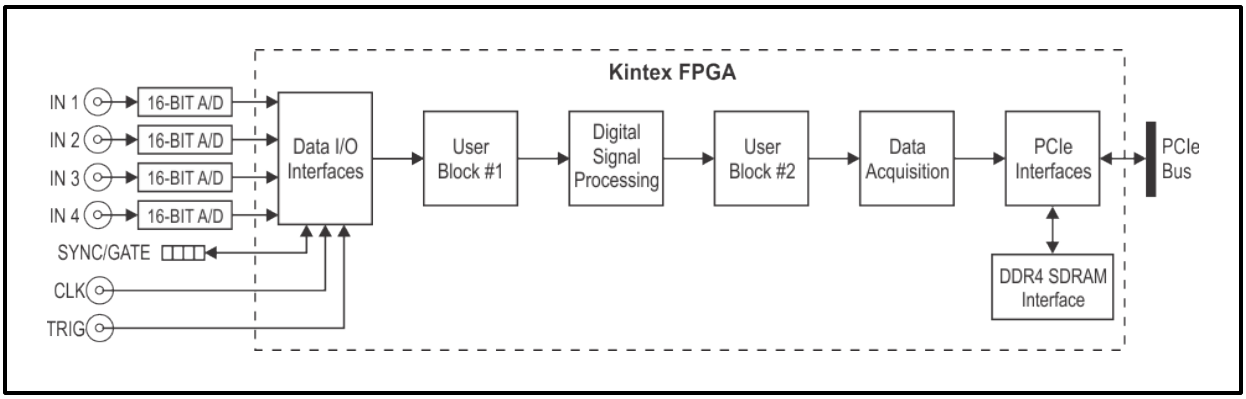
Chapter 4: FPGA IP Core Operation

Overview

The diagram and topics below describe the data flow of the Model 71861 FPGA IP code. The simplified block diagram below shows the overall data flow, the board interfaces, and the data flow from/to these interfaces with the FPGA.

For access to detailed documentation of the IP Core modules and their programmable registers, refer to the HTML help version of this user manual. You can obtain the HTML version by downloading the User Manual Library for the specific board you are using. Instructions are provided in Getting the User Manual Library.

Model 71861 FPGA Simplified Data Flow



The top-level functional blocks of the FPGA IP code are described in the following sections:

- "Data I/O Interfaces" on page 53
- "Digital Signal Processing" on page 56
- "Data Acquisition" on page 59
- "PCIe Interfaces" on page 62
- "DDR4 SDRAM Interface" on page 66
- "User Blocks" on page 67

Refer to "Default FPGA Memory Map" on page 71 for the memory map of the FPGA IP Core modules.

Channel Nomenclature

The Model 71861 has four analog inputs to the ADS5485 ADCs, identified on the front panel as **IN 1**, **IN 2**, **IN 3**, and **IN 4**. All references to the hardwired digital outputs from the ADS5485 ADCs and their signal connections to the FPGA use the numbers 1 through 4 to identify the associated input connector.

The 71861 FPGA IP code has four input interface cores (ADC Interface Cores): one for each front panel input, that are identified as ADC0 through ADC3. These are allocated to the four input signals as follows:

Front Panel Input	ADC Code Channel
IN 1	ADC0
IN 2	ADC1
IN 3	ADC2
IN 4	ADC3

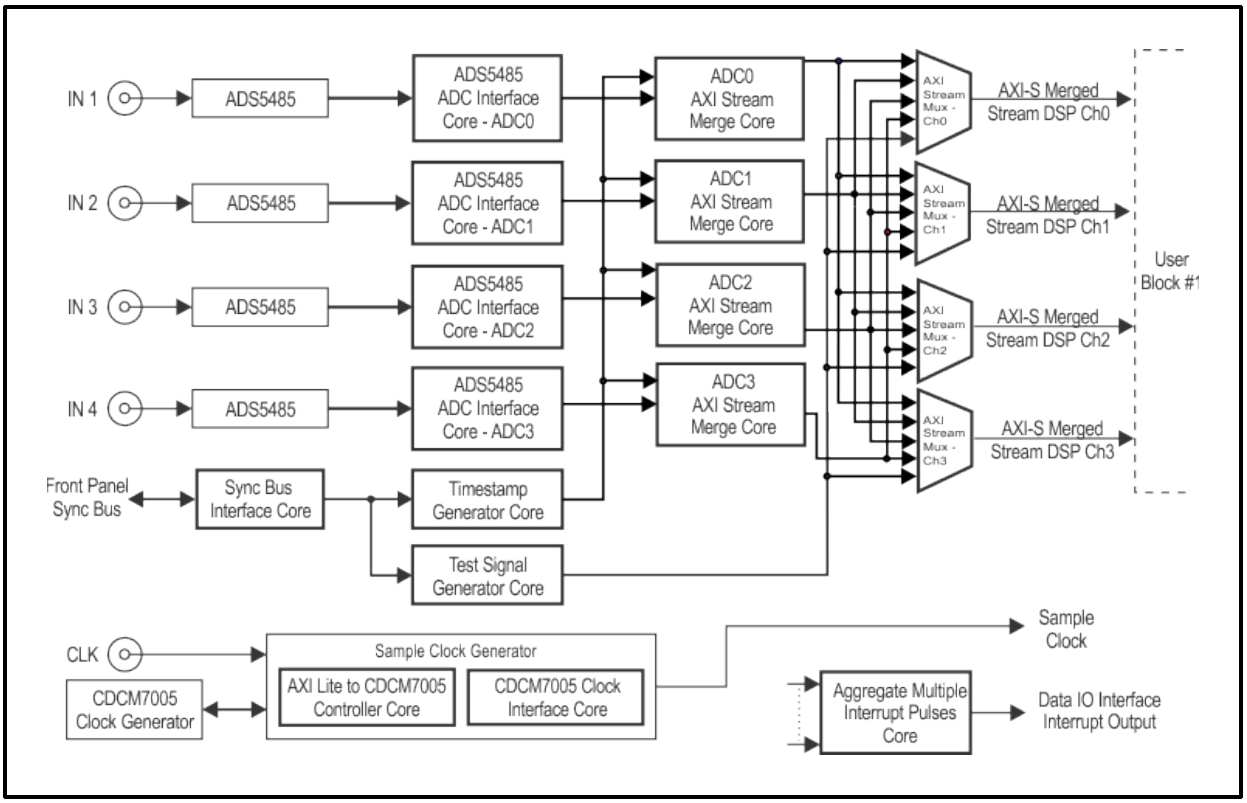
In addition, the 71861 FPGA IP code has four Digital Signal Processing channels that are identified as Ch0, Ch1, Ch2, and Ch3. These are not allocated to specific ADC Interface Core channels and must be allocated by the user (see Channel Data Source Select Cores).

In the functional descriptions of the 71861 FPGA IP code in the following sections of this chapter, whenever the signal inputs are referenced, the nomenclature is in accordance with the front panel signal input connector numbers (1 through 4), and whenever the FPGA IP code processing is referenced, the nomenclature is in accordance with the ADC interface code channel numbers (0 through 3) or the DSP channel numbers (0 through 3).

When referencing any signal inputs in the Pentek Model 71861 front panel I/O module schematic drawings or in the Pentek Model 71861 Navigator FPGA Design Kit, the nomenclature is in accordance with the ADC code channel numbers, 0 through 3.

Data I/O Interfaces

The block diagram below shows the Data I/O Interfaces data flow for one of the four ADC inputs. This block of IP Core modules provides interfaces to the four ADS5485 ADCs, the front panel Sync Bus, and the sample clock generation devices.



The memory map for these FPGA IP Core modules is provided in "Data I/O Interfaces" on page 73. For information about the corresponding support software refer to "Board Support Software: Navigator Design Suite" on page 13.

The following subsections describe the IP Cores shown in the block diagram.

ADC Interface

There is an ADC Interface Core for each front panel ADC input (ADC0, ADC1, etc. – see "Channel Nomenclature" on the previous page for ADC channel assignments). Each ADC Interface Core receives double data rate (DDR) digital inputs from the associated ADS5485 ADC. This core provides setup and hold adjustments and gain and offset adjustment of the data before being converted to AXI4–Stream output. In addition, the ADC Interface Core detects input signal overload and provides control of power–down and dither to its associated ADS5485 ADC.

Refer to the Pentek ***Navigator ADS5485 ADC Interface IP Core Manual*** for a description of this IP module.

Sync Bus Interface

The Sync Bus Interface IP Core receives and generates Gate, Sync, and PPS signals for the front panel Sync Bus, and generates timing signals for merging with the input data. The output of this core provides an AXI4−Stream timing bus consisting of the Gate, Sync, and PPS signals for use by all ADC channels.

Refer to the Pentek ***Navigator Sync Bus Interface IP Core Manual*** for a description of this IP module.

Timestamp Generate

The Timestamp Generator Interface IP Core accepts input Timing Event AXI4−Streams (Gate, Sync, and PPS) from the Sync Bus. These signals are used to control the generation of a timestamp output AXI4−Stream which provides counts of sample clock cycles and PPS events for use by all four ADC channels.

Refer to the Pentek ***Navigator Timestamp Generator IP Core Manual*** for a description of this IP module.

ADC AXI4−Stream Merge

There is an AXI4−Stream Merge Core for each ADC channel (ADC0, ADC1, etc.). Each AXI4−Stream Merge Core receives inputs from the associated ADC Interface Core (ADC0, ADC1, etc.) (see "ADC Interface" on the previous page) and from the Timestamp Generate Core (see "Timestamp Generate" above) and generates a merged AXI4−Stream output. This core merges the data and timing information into a single stream to be processed by the Channel Data Source Select Cores (see "Data Source Select" below).

Refer to the Pentek ***Navigator AXI4−Stream Merge IP Core Manual*** for a description of this IP module.

Test Signal Generate

The Test Signal Generator Interface IP Core generates either a sinewave or ramp signal and delivers an output Test Signal AXI4−Stream to be processed by the four Channel Data Source Select Cores (see "Data Source Select" below).

Refer to the Pentek ***Navigator Test Signal Generator IP Core Manual*** for a description of this IP module.

Data Source Select

There is a Channel Data Source Select Core for each Digital Signal Processing channel (Ch0, Ch1, etc.). This core selects the data stream for this DSP channel from one of the ADC AXI4−Stream Merge Cores (see "ADC AXI4−Stream Merge" above) or a Test Signal (see "Test Signal Generate" above).

The input and output data for this core are combined sample data/timestamp AXI4−Streams.

Refer to the Pentek ***Navigator AXI4−Stream Multiplexer IP Core Manual*** for a description of this IP module.

CDCM7005 Control & Clock Generation

Two IP Core modules provide control of the CDCM7005 Clock Generator and the ADC Sample Clock.

- The AXI to CDCM7005 Controller IP Core controls the CDCM7005 clock generator. This core provides the CDCM7005 interface SPI (Serial Peripheral Interface) outputs that initialize and control the CDCM7005 clock generator.

  Refer to the Pentek ***Navigator AXI to CDCM7005 Controller IP Core Manual*** for a description of this IP module.

- The CDCM7005 Clock Interface IP Core controls the interface between the CDCM7005 clock generator and other modules. This core receives a clock signal from the CDCM7005 and generates the sample clock output used by subsequent IP Core modules.

  Refer to the Pentek ***Navigator CDCM7005 Clock Interface IP Core Manual*** for a description of this IP module.

Data I/O Interrupts

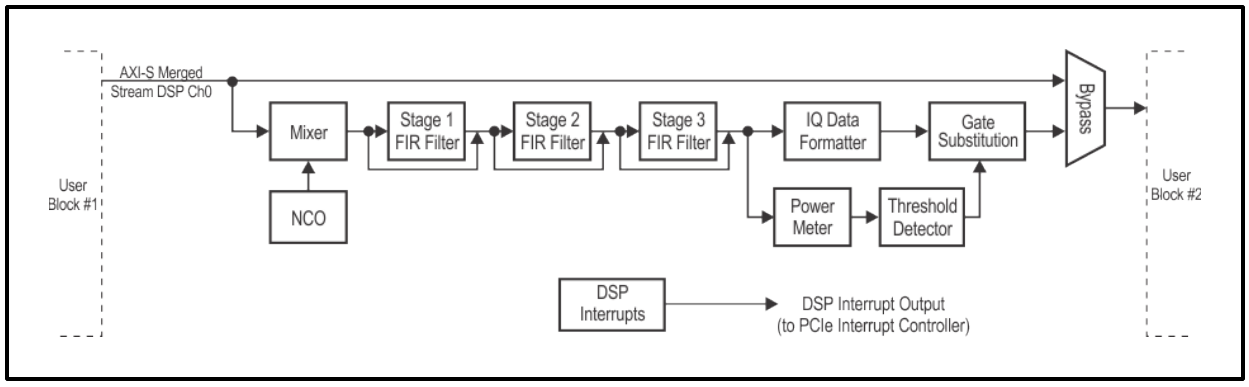
The Aggregate Multiple Interrupt Pulses Core combines edge−type interrupt inputs from several Data I/O sources and generates a single interrupt output. The following Data I/O interrupt sources are included:

CDCM7005 Controller Interrupt
CDCM7005 Interface Interrupt
Sync Bus A Interrupt
Test Signal Generator Interrupt
ADC0 Interrupt
ADC1 Interrupt
ADC2 Interrupt
ADC3 Interrupt

Refer to the Pentek ***Navigator Aggregate Multiple Interrupt Pulses IP Core Manual*** for a description of this IP module.

Digital Signal Processing

The block diagram below shows the Digital Signal Processing data flow for one of the four DSP channels. This block of IP Core modules performs a digital downconversion of each DSP channel's input data stream.



The memory map for these FPGA IP Core modules is provided in "Digital Signal Processing" on page 74. For information about the corresponding support software, refer to "Board Support Software: Navigator Design Suite" on page 13.

The following subsections describe the IP Cores shown in the Digital Signal Processing Data flow.

NCO

The Numerically Controlled Oscillator (NCO) IP Core generates a complex sinusoidal tuning frequency waveform for the digital mixer (see "Mixer" below).

Refer to the Pentek ***Navigator AXI4-Stream Numerically Controlled Oscillator IP Core Manual*** for a description of this IP module.

Mixer

The Mixer IP Core performs a complex multiplication of the input sample data/timestamp AXI4-Stream (see "Data Source Select" on page 54) and the sine and cosine output of the NCO (see "NCO" above). This results in a down-converted AXI4-Stream output, which is sent to the first FIR filter stage (see "Stage 1 FIR Filter" below).

Refer to the Pentek ***Navigator AXI4-Stream Mixer IP Core Manual*** for a description of this IP module.

Stage 1 FIR Filter

The Folded Symmetrical Decimation FIR Filter IP Core performs the first stage of filtering and decimation on the down-converted AXI4-Stream output from the mixer (see "Mixer" above). This core implements an FIR Filter with a decimation factor of any integer from 2 to 32. The 18-bit FIR filter coefficients and the gain of the filter output are user-programmable. A default set of filter coefficients is provided by Pentek.

Refer to the Pentek ***Navigator AXI4-Stream Folded Symmetrical Decimation FIR Filter IP Core Manual*** for a description of this IP module.

Stage 2 FIR Filter

The Stage 2 Decimation FIR Filter performs the second stage of filtering and decimation with a decimation factor of any integer from 2 to 32, and can be bypassed. See "Stage 1 FIR Filter" on the previous page for a description of this core.

Stage 3 FIR Filter

The Stage 3 Decimation FIR Filter performs the third stage of filtering and decimation with a decimation factor of any integer from 2 to 32, and can be bypassed. See "Stage 1 FIR Filter" on the previous page for a description of this core.

Any Stage FIR Filter can be bypassed. However, only Stage 3 has 24−bit output, so if you are packetizing the output in 24−bit format, do not bypass Stage 3.

IQ Data Formatter

The IQ Data Format IP Core generates output data that optionally has inverted spectrum and/or offset spectrum of the filtered data stream.

Refer to the Pentek ***Navigator AXI4−Stream IQ Data Format IP Core Manual*** for a description of this IP module.

Power Meter

The Power Meter IP Core performs a power calculation (I2+Q2) on every data sample, calculates average power over a programmable number of samples, and outputs an AXI4−Stream of average magnitude (square root).

Refer to the Pentek ***Navigator AXI4−Stream Power Meter IP Core Manual*** for a description of this IP module.

Threshold Detector

The Threshold Detector IP Core generates a detection signal when the magnitude (see "Power Meter" above) is greater than a programmable threshold, and clears that signal when the magnitude value falls below a programmable hysteresis value (threshold − hysteresis below threshold). This detection signal can be used as a gate in the DSP output (see "DSP Gate Substitution" below).

Refer to the Pentek ***Navigator AXI4−Stream Threshold Detector IP Core Manual*** for a description of this IP module.

DSP Gate Substitution

The DSP Gate Substitution IP Core provides optional gate substitution of the gate bits within the DSP output stream with a gate defined by the threshold detector signal (see "Threshold Detector" above). Alternately, the gate bits in the DSP output stream can be ANDed with the gate defined by the threshold detector signal.

Refer to the Pentek ***Navigator AXI4-Stream Gate Substitution IP Core Manual*** for a description of this IP module.

DSP Bypass Mux

The DDC Bypass function uses the Multiplexer IP Core to either select or bypass the DSP output data stream.

Refer to the Pentek ***Navigator AXI4-Stream Multiplexer IP Core Manual*** for a description of this IP module.

DSP Interrupts

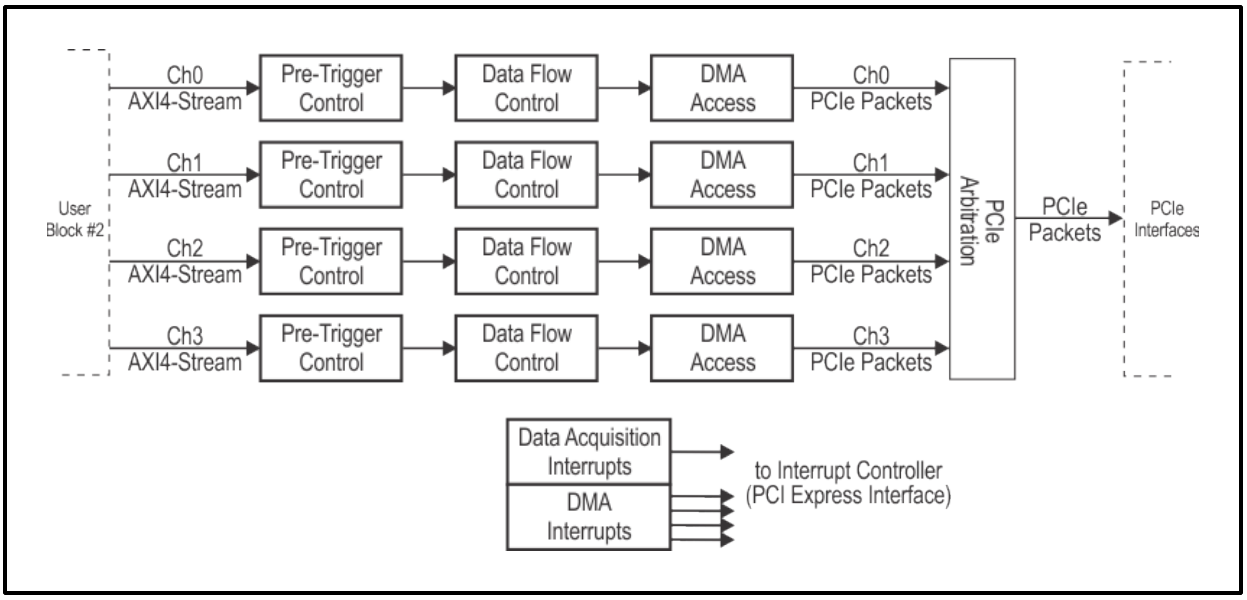
The Aggregate Multiple Interrupt Pulses IP Core combines the edge-type interrupt inputs and generates a single interrupt output for each DSP channel. The DSP interrupts include the following:

Stage 1 FIR Saturation
Stage 2 FIR Saturation
Stage 3 FIR Saturation
Power Meter
Threshold Detect

Refer to the Pentek ***Navigator Aggregate Multiple Interrupt Pulses IP Core Manual*** for a description of this IP module.

Data Acquisition

The diagram below shows the Data Acquisition data flow for the four DSP channels. This block of IP Core modules delays and packetizes the AXI4−Stream data for output, and transmits the data to the PCIe interface using DMA.



The memory map for these FPGA IP Core modules is provided in "Default FPGA Memory Map" on page 71. For information about the corresponding support software, refer to "Board Support Software: Navigator Design Suite" on page 13.

Except for the Data Acquisition Interrupts Core, there are four copies of each IP Core described in the following subsections: one for each Digital Signal Processing channel (Ch0, Ch1, Ch2, and Ch3).

Pre−Trigger Control

The Pre−Trigger Control Core for each channel delays the combined data/timestamp AXI4−Stream data relative to the Gate/Sync/PPS events to allow the use of data captured prior to the trigger (pre−trigger data).

Refer to the Pentek ***Navigator AXI4−Stream Advance IP Core Manual*** for a description of this IP module.

The Pre−Trigger delay delays the data with respect to the trigger or gate by a programmable number of data samples. When data is DDC data it is in terms of DDC samples. The granularity of the delay depends on the samples/cycle of the product and the data mode.

Note also that when trying to pre−trigger, you should set post trigger delay to zero or it will negate it.

Raw Data Mode:

Delay Setting = desired number of pre−trig samples/1

Max Delay = 1*1023

DDC Mode:

Delay Setting = desired number of pre-trig DDC samples/1

Max Delay = 1*1023

Data Flow Control

The Data Flow Control and Packetizer Core for each channel accepts the AXI4-Stream data from Pre-Trigger Control, and generates a packed output AXI4-Stream, where the start and end of packet are controlled by either a gate signal, a trigger signal, or a timestamp range.

Refer to the Pentek ***Navigator AXI4-Stream Data Flow Control and Packetizer Type-1 IP Core Manual*** for a description of this IP module.

The following are the data packing formats for each 32-bit output word (selected by registers in this core):

Data Packing Formats			
Real Data			
Bit	**31 - 16**	**15 - 0**	
Value	16-bit sample[15:0] at (t+1)	16-bit sample[15:0] at time (t)	
Packed I/Q Data			
Bit	**31 - 16**	**15 - 0**	
Value	16-bit Q sample[15:0]	16-bit I sample[15:0]	
Unpacked I/Q Data			
Bit	**31 - 8**		**7 - 0**
Value	24-bit I sample[23:0] (next 32-bit word contains 24-bit Q value)		00000000

DMA

The PCIe DMA Core for each channel moves the packetized AXI4-Stream (see "Data Flow Control" above) to the PCIe interface (see "AXI4-Stream Traffic Meter" on page 62) using a linked-list DMA methodology. This core also transmits meta data which includes information about the data being moved such as timestamp, transfer length, and start and end of data acquisition markers.

There are two separate memory map addresses for this IP Core (see "Data Acquisition" on page 72): one for the core control registers and one for the Linked List Descriptor RAM.

Refer to the Pentek ***Navigator AXI4-Stream to PCI Express (PCIe) Direct Memory Access (DMA) IP Core Manual*** for a description of this IP module.

Data Acquisition Interrupts

The Aggregate Multiple Interrupt Pulses IP Core combines edge−type interrupt inputs and generates a single interrupt output for all four DSP channels. The Data Acquisition interrupts include the following:

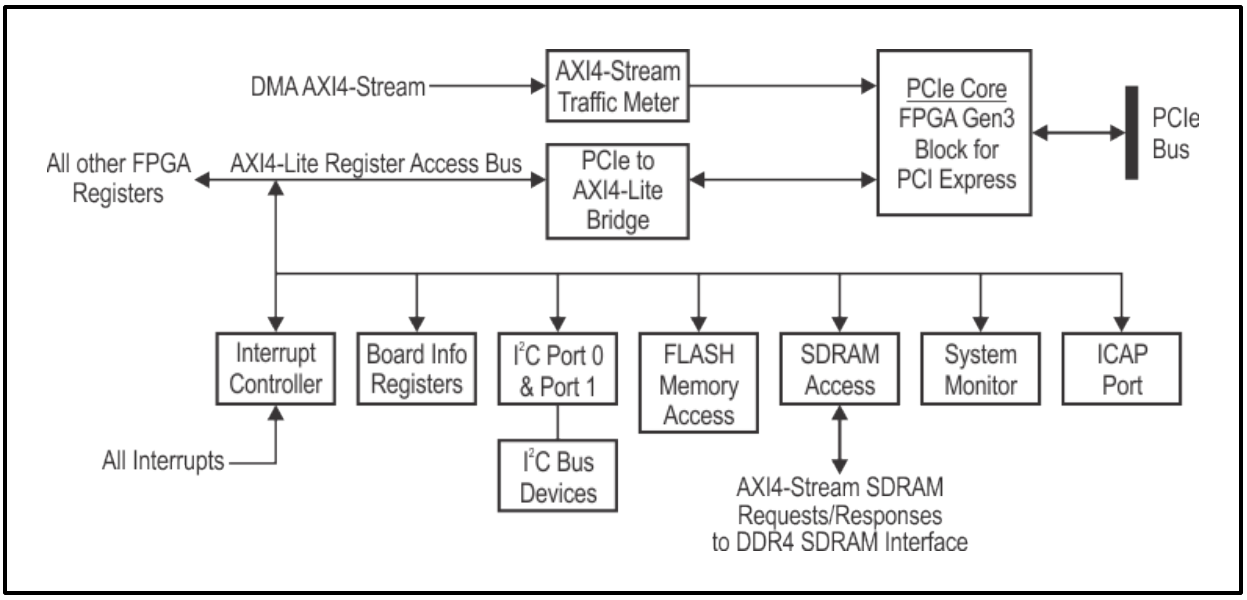
Ch0 Interrupt
Ch1 Interrupt
Ch2 Interrupt
Ch3 Interrupt

Note that these Data Acquisition interrupts do not include DMA interrupts from the PCIe DMA Core (see "DMA" on the previous page). DMA interrupts are routed separately to the PCI Express Interrupt Controller Core (see "Interrupt Controller" on page 63).

Refer to the Pentek ***Navigator Aggregate Multiple Interrupt Pulses IP Core Manual*** for a description of this IP module.

PCIe Interfaces

The block diagram below shows the PCIe Interfaces data flow. This block of IP Core modules controls all data I/O for the board's PCI Express interface and provides access to the board's I2C devices, Flash memory, and SDRAM memory.



The memory map for these FPGA IP Core modules is provided in "PCI Express Interfaces" on page 71. For information about the corresponding support software, refer to "Board Support Software: Navigator Design Suite" on page 13.

The following subsections describe the IP Cores shown in the block diagram.

AXI4−Stream Traffic Meter

The AXI Stream Bus Traffic Meter IP Core accepts packetized AXI4−Streams from Data Acquisition DMA Core requests (see "DMA" on page 60) and measures the DMA traffic in bytes per second. The packetized DMA AXI4−Stream is passed to the FPGA Gen3 PCIe Core.

Refer to the Pentek ***Navigator AXI4−Stream Bus Traffic Meter IP Core Manual*** for a description of this IP module.

FPGA Gen3 PCIe Core

The FPGA Gen3 PCIe Core provides the AXI4−Stream interface to the FPGA GTH transceivers for PCI Express using the Xilinx Vivado Design Suite LogiCORE IP Core: *ultrascale_pcie_gen3*.

Refer to the Xilinx ***UltraScale Architecture Gen3 Integrated Block for PCI Express LogiCORE IP Core Manual*** for a description of this IP module.

PCIe To AXI4−Lite Bridge

The PCIe to AXI4−Lite Bridge Core provides the interface between all FPGA control/status registers and the FPGA Gen3 PCIe Core.

Refer to the Pentek ***Navigator PCI Express to AXI4-Lite Bridge IP Core Manual*** for a description of this IP module.

Most other IP core modules include control/status registers that apply to the core's operation. Refer to the Pentek IP Core Manual listed in each core's description for the control/status registers defined for that core.

Interrupt Controller

The PCI Express Interrupt Controller IP Core combines all interrupts from the other modules and generates MSI (Message-Signaled Interrupt) or Legacy configuration interface interrupt signals. This core also has an output status signal to indicate the Interrupt Request operation mode (Legacy or MSI) of the core.

The PCI Express interrupts include the following:

Board Monitoring Interrupts
Timestamp Interrupt
Data I/O Interrupts
Data Acq Interrupts
DMA 0 Interrupt
DMA 1 Interrupt
DMA 2 Interrupt
DMA 3 Interrupt
DSP Ch 0 Interrupts
DSP Ch 1 Interrupts
DSP Ch 2 Interrupts
DSP Ch 3 Interrupts
User Block #1 Interrupt0
User Block #1 Interrupt1
User Block #2 Interrupt0
User Block #2 Interrupt1

Refer to the Pentek ***Navigator PCI Express Interrupt Controller IP Core Manual*** for a description of this IP module.

Board Information Registers

The Board Information Registers IP Core provides board status information such as: board type, FPGA code type, FPGA revision and date, front panel IO type, and PCIe link status.

This core also provides a byte swap register, LED control registers, and interrupt control registers.

Refer to the Pentek ***Navigator Board Information Registers IP Core Manual*** for a description of this IP module.

I2C Port 0

The I^2C Port 0 function uses the AXI I2C Bus Interface IP Core – Port 1 to access devices connected to I^2C Port 0. The devices on this bus include the LM83 Temperature Sensor on the front panel interface module, and the Si571 Any-Rate VCXO, LM95234 Temperature Sensor, LTC2990 Temperature Monitor, and Si5341B AnyRate Clock Generator on the main PCB (refer to "I2C Bus 0" on page 43 for descriptions of these devices).

Refer to the Pentek ***Navigator AXI I2C Bus Interface IP Core Manual*** for a description of this IP module.

I2C Port 1

The I^2C Port 1 function uses the AXI I2C Bus Interface IP Core – Port 2 to access devices connected to I^2C Port 1. The devices on this bus include the Serial EEPROM and the XMC connector I^2C port (refer to "I2C Bus 1" on page 48 for descriptions of these devices).

Refer to the Pentek ***Navigator AXI I2C Bus Interface IP Core Manual*** for a description of this IP module.

Configuration Flash Access

The AXI4-Lite to NOR Flash Interface IP Core provides the data interface to the configuration Flash Memory. This core performs direct PCIe read/write operations to Flash Memory.

Refer to the Pentek ***Navigator AXI4-Lite to 16-bit Parallel NOR Flash Interface IP Core Manual*** for a description of this IP module.

DDR4 SDRAM Access

The AXI4-Lite to DDR4 SDRAM Bridge IP Core provides access to the DDR4 SDRAM memory control logic. This core accepts AXI4-Lite DDR4 memory read/write requests and converts these to DDR4 SDRAM AXI4-Stream requests to and responses from the DDR4 SDRAM Interface block.

Refer to the Pentek ***Navigator AXI4-Lite to DDR4 SDRAM Bridge IP Core Manual*** for a description of this IP module.

System Monitor

The System Monitor Core monitors FPGA voltages and temperatures using the Xilinx Vivado Design Suite LogiCORE IP Core: *system_management_wiz*.

Refer to the Xilinx ***System Management Wizard LogiCORE IP Core Manual*** for a description of this IP module.

ICAP Port

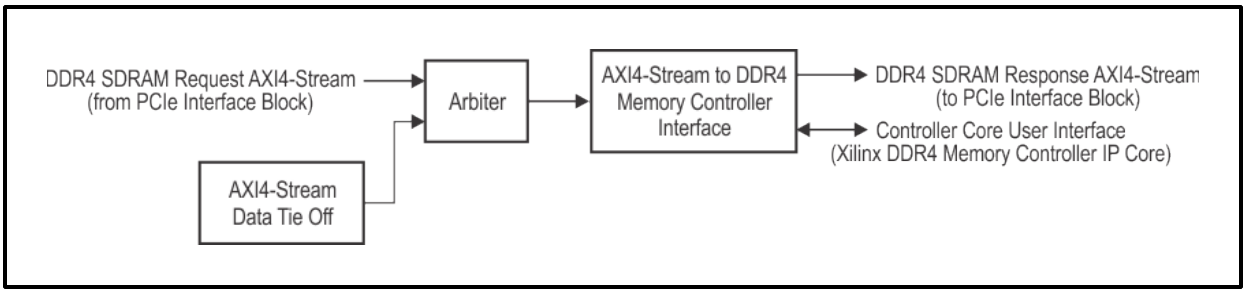
The ICAP Port Core allows the user to read and write the FPGA configuration memory through the Internal Configuration Access Port (ICAP) using the Xilinx Vivado Design Suite LogiCORE IP Core: *axi_hwicap*.

Only advanced users who have FPGA reconfiguration experience should use the ICAP port.

Refer to the Xilinx ***AXI HWICAP LogiCORE IP Core Manual*** for a description of this IP module.

DDR4 SDRAM Interface

The block diagram below shows the DDR4 SDRAM Interface data flow. This block of IP Core modules provides control and data interfaces to the DDR4 SDRAM.



The memory map for these FPGA IP Core modules is provided in "PCI Express Interfaces" on page 71. For information about the corresponding support software, refer to "Board Support Software: Navigator Design Suite" on page 13.

The following subsections provide information about the block diagram.

DDR4 Memory Controller Interface

The AXI4-Stream to DDR4 Memory Controller Interface IP Core provides a control interface to the Xilinx DDR4 SDRAM Memory Controller.

The core receives DDR4 Memory read/write request AXI4-Streams from the PCIe Interface SDRAM Access core (see "DDR4 SDRAM Access" on page 64) and converts them into control signals to the Xilinx DDR4 Memory Controller IP Core. The core also accepts responses from the Xilinx DDR4 Memory Controller IP Core and converts them into AXI4-Stream responses to the PCIe Interface SDRAM Access core.

Refer to the Pentek ***Navigator AXI4-Stream to DDR4 Memory Controller Interface IP Core Manual*** for a description of this IP module.

Refer to the Xilinx ***UltraScale Architecture-Based FPGAs Memory IP Core Manual*** for a description of the Xilinx DDR4 Memory Controller IP module.

AXI4-Stream Data Tie Off

AXI4-Stream Data Tie Off IP Core provides a data interface to the DDR4 SDRAM Memory Controller. This core provides all AXI4-Stream interface signals that can be used for user--defined SDRAM access.

Refer to the Pentek ***Navigator AXI4-Stream Data Tie Off IP Core Manual*** for a description of this IP module.

User Blocks

The FPGA provides two IP Core modules for user custom processing: User Block 1 and User Block 2. See "Model 71861 FPGA Simplified Data Flow" on page 51 for the location of these User Blocks in the overall data flow.

In the default FPGA configuration, these User Blocks contain no data processing and are just pass−through functions. You can use the Navigator FPGA Design Kit (FDK) to create custom user IP code for these blocks. (The Navigator FDK provides the complete IP code for the 71861 Jade board. You can access every component of the Pentek design, replacing or modifying blocks, such as the User Blocks, as needed for your application. See "Board Support Software: Navigator Design Suite" on page 13 for further description of the Navigator FDK.)

In addition, the FPGA reserves two blocks of PCI memory for user registers or data storage by the User Blocks. The memory map for the User Blocks' register/storage space is provided in "User Block Address Space" on page 77.

Chapter 5: Navigator Board Support Package

The Navigator Board Support Package (BSP) provides C−callable software routines for accessing and controlling the Model 71861 Jade board. The BSP is a layered architecture, having four "layers."

- Application Layer
- High Level API Layer
- Board−Specific / PCIe Support / Utility Layer
- IP Block / Hardware Layer

User programs are Application layer code. These programs call routines in the High Level API library. High Level API library routines call routines the Board−specific, PCIe Driver, and Utility libraries. These libraries consist of routines that call the lowest level library routines that interface to the FPGA IP core module or hardware devices.

The four layers are discussed below, from the bottom (nearest the hardware) and up.

The *Navigator BSP User's Guide* describes how to install and use the BSP software.

The *API Reference Guide for the Navigator BSP* describes the source and include files in the BSP and is available in both HTML and PDF format (**API_Reference.html** and **API_Reference.pdf**). The *API Reference Guide* is available in the following location:

Windows:

C:\Pentek\BSP\BSP_X.Y\docs (where **X.Y** is the version number)

or

%NAVBSP%\docs

Linux:

/home/username/Pentek/BSP/BSP_X.Y/docs (where **X.Y** is the version number)

or

$NAVBSP/docs

IP Block / Hardware Layer

This layer consists of two components: the IP block library and the hardware library.

IP block library: This library provides the software interface to the IP core modules and communicates directly with them. It is tightly integrated with the IP core modules and provides a single source and single header file to support each module. All files are compiled into a single IP core dynamic−link library. Functions in this DLL are accessed only via board−specific layer functions.

Hardware library: This library communicates with hardware devices that are external to the FPGA. Currently, there are no memory−mapped hardware devices. There are hardware

devices outside the FPGA, such as the Si571 VCXO and the CDCM7005 clock divider, but these are not memory mapped. They are accessed via IP core modules, such as an I2C interface. Any functions in a DLL for future memory mapped devices would be accessed only from board−specific layer functions.

Board−Specific / PCIe Support / Utility Layer

This layer consists of three components: board−specific libraries, PCIe support library, and utility library.

- **Board−specific libraries** are single DLLs tailored for each XMC board model family. For example, there is a Model 71861 board family DLL, a 71851−family DLL, etc. Routines in the DLLs are built around calls to routines in the IP block/hardware libraries. Hardware debugging routines, such as register dumps, are included in these libraries. Board−specific libraries also include routines to access hardware devices on the board that are external to the FPGA but accessed via IP core modules. For example, the ADC12D1800 ADC is programmed via the **`px_ADC12D1800intrfc`** IP core module.
- **PCIe support library:** Single DLLs are provided for PCIe support. The PCIe driver interfaces to the PCIe bus and does not call external BSP DLLs.
- **Utility library:** This library provides operating system routines for file I/O, printing, command line parsing, etc. The utility library also contains files that support the Signal Viewer. The command line utility and Signal Viewer are described in the *Navigator BSP User's Guide*.

High Level API Layer

The High Level API Layer provides routines called by user or example programs to program and control a Pentek Jade family board. These routines are generic in nature, calling board−specific routines via function pointers. There will be no direct communication to the IP core or hardware library routines.

This layer provides a wrapper to isolate the user from the board−specific details.

Application Layer

The Application layer is the code the customer develops for his desired application. General purpose examples will be provided with the BSP.

Chapter 6: Model 71861 Memory Maps

Overview

This chapter describes access to the Model 71861 IP Core module resources from an external (off−board) PCIe Bus Master, such as an XMC baseboard processor. Memory maps to these resources are given from the baseboard processor's viewpoint.

The Model 71861 is controlled from the XMC baseboard through a PCIe Bus interface. All 71861 resources are configured to be available in PCI Address Space, relative to PCI Base Address Register 0 as listed in the "Model 71861 PCI Memory Map" below table. See PCI Configuration Space Registers for a summary of the PCI Configuration Space Registers.

Model 71861 PCI Memory Map	
PCI Bus Address *	**Modules**
0x0000_0000	PCI Express Interfaces
0x0080_0000	Data Acquisition
0x0100_0000	Data I/O Interfaces
0x0200_0000	Digital Signal Processing
0x0300_0000	User Block Address Space
* All addresses are relative to PCI Base Address Register 0. Refer to the operating manual supplied with your XMC baseboard or carrier for the PCI Base Address settings.	

Default FPGA Memory Map

The following is the memory map of the default FPGA IP Core module resources accessible from an XMC baseboard processor, and a reference to the definition of each module in "FPGA IP Core Operation" on page 51.

For access to detailed documentation of the IP Core modules and their programmable registers, refer to the HTML help version of this user manual.

PCI Express Interfaces

Base Address	Module	Description	Reference
0x0000_0000	Board Information	Board Information Registers	Board Information Registers
0x0000_1000	Interrupt Controller	Main Interrupt Controller	Interrupt Controller
0x0000_2000	PCIe Tx Traffic Meter	Monitors current PCIe Tx bytes/sec	AXI4−Stream Traffic Meter
0x0000_3000	−	Reserved	−
0x0000_4000	System Monitor	Monitoring of Voltages and FPGA Temperature	System Monitor
0x0000_5000	Config Flash Access	Read/Write Access to Configuration Flash	Configuration Flash Access
0x0000_6000	DDR4 RAM Access	Read/Write Access to DDR4 RAM	DDR4 SDRAM Access
0x0000_7000	DDR4 Controller	DDR4 RAM Controller Initialization and Status	DDR4 Memory Controller Interface
0x0000_8000	I2C Port 0	No MGA	I2C Port 0
0x0000_9000	I2C Port 1	Has MGA	I2C Port 1
0x0000_A000	ICAP Port	Internal Configuration Port Access	ICAP Port

Data Acquisition

Base Address	Module	Description	Reference
0x0080_0000	Ch0 Data Acquisition	Outputs Ch0 Data to DMA based on Gate Events	Data Flow Control
0x0080_1000	Ch1 Data Acquisition	Outputs Ch1 Data to DMA based on Gate Events	
0x0080_2000	Ch2 Data Acquisition	Outputs Ch2 Data to DMA based on Gate Events	
0x0080_3000	Ch3 Data Acquisition	Outputs Ch3 Data to DMA based on Gate Events	
	–	Reserved	–
0x0080_8000	Ch0 Pre−Trigger Control	Delays Ch0 Data relative to Gate	Pre−Trigger Control
0x0080_9000	Ch1 Pre−Trigger Control	Delays Ch1 Data relative to Gate	
0x0080_A000	Ch2 Pre−Trigger Control	Delays Ch2 Data relative to Gate	
0x0080_B000	Ch3 Pre−Trigger Control	Delays Ch3 Data relative to Gate	
	–	Reserved	–
0x0090_0000	Ch0 DMA	Channel 0 DMA Control Registers	DMA
0x0092_0000		Channel 0 DMA Linked List Descriptor RAM	
0x0094_0000	Ch1 DMA	Channel 1 DMA Control Registers	
0x0096_0000		Channel 1 DMA Linked List Descriptor RAM	
0x0098_0000	Ch2 DMA	Channel 2 DMA Control Registers	
0x009A_0000		Channel 2 DMA Linked List Descriptor RAM	
0x009C_0000	Ch3 DMA	Channel 3 DMA Control Registers	
0x009E_0000		Channel 3 DMA Linked List Descriptor RAM	
0x00D0_0000	Data Acq Interrupts	Interrupt Registers for Data Acquisition	Data Acquisition Interrupts

Data I/O Interfaces

Base Address	Module	Description	Reference
0x0100_0000	Data I/O Interrupts	Interrupt Registers associated with I/O Interfaces	Data I/O Interrupts
0x0100_1000	CDC SPI Control	CDCM7005 SPI Control Interface	CDCM7005 Control & Clock Generation
0x0100_2000	CDC Clock Generation	CLK ADC Sample Clock Generation	CDCM7005 Control & Clock Generation
0x0100_3000	–	Reserved	–
0x0100_4000	Sync Bus Control	Sync Bus Control	Sync Bus Interface
0x0100_5000	–	Reserved	–
0x0100_6000	Timestamp Generate	Timestamp Generation	Timestamp Generate
0x0100_7000	–	Reserved	–
0x0100_8000	Test Signal Generate	Test Signal Generation	Test Signal Generate
0x0101_0000	ADC 0 Interface Control	ADC 0 ADS5485 ADC Control	ADC Interface
0x0101_1000	Ch0 Data Source Select	DSP Channel 0 Data Source Selection	Data Source Select
0x0102_0000	ADC 1 Interface Control	ADC 1 ADS5485 ADC Control	ADC Interface
0x0102_1000	Ch1 Data Source Select	DSP Channel 1 Data Source Selection	Data Source Select
0x0103_0000	ADC 2 Interface Control	ADC 2 ADS5485 ADC Control	ADC Interface
0x0103_1000	Ch2 Data Source Select	DSP Channel 2 Data Source Selection	Data Source Select
0x0104_0000	ADC 3 Interface Control	ADC 3 ADS5485 ADC Control	ADC Interface
0x0104_1000	Ch3 Data Source Select	DSP Channel 3 Data Source Selection	Data Source Select

Digital Signal Processing

Base Address	Module	Description	Reference
0x0200_0000	Ch0 DSP Interrupts	Interrupt Registers for DSP Ch0	DSP Interrupts
0x0200_1000	Ch0 DDC Mixer	Ch0 DDC Mixer Control	Mixer
0x0200_2000	Ch0 DDC NCO	Ch0 DDC NCO Control	NCO
0x0200_3000	–	Reserved	–
0x0200_4000	Ch0 DDC Stage 1 Filter	Ch0 DDC Stage 1 Filter (Dec = 2 to 32)	Stage 1 FIR Filter
0x0200_6000	Ch0 DDC Stage 2 Filter	Ch0 DDC Stage 2 Filter (Dec = 2 to 32)	Stage 2 FIR Filter
0x0200_8000	Ch0 DDC Stage 3 Filter	Ch0 DDC Stage 3 Filter (Dec = 2 to 32)	Stage 3 FIR Filter
0x0200_9000	–	Reserved	–
0x0200_A000	Ch0 DDC Output Formatter	Ch0 DDC Output Formatter	IQ Data Formatter
0x0200_B000	Ch0 DDC Bypass Mux	Ch0 DDC Bypass Mux	DSP Bypass Mux
0x0200_C000	–	Reserved	–
0x0200_D000	–	Reserved	–
0x0200_E000	–	Reserved	–
0x0200_F000	–	Reserved	–
0x0201_0000	Ch0 DDC Power Meter	Ch0 DDC Power Meter	Power Meter
0x0201_1000	Ch0 DDC Threshold Detect	Ch0 DDC Threshold Detection	Threshold Detector
0x0201_2000	Ch0 DDC Threshold Gating	Ch0 DDC Threshold Gating	DSP Gate Substitution
0x0210_0000	Ch1 DSP Interrupts	Interrupt Registers for DSP Ch1	DSP Interrupts
0x0210_1000	Ch1 DDC Mixer	Ch1 DDC Mixer Control	Mixer
0x0210_2000	Ch1 DDC NCO	Ch1 DDC NCO Control	NCO
0x0210_3000	–	Reserved	–
0x0210_4000	Ch1 DDC Stage 1 Filter	Ch1 DDC Stage 1 Filter (Dec = 2 to 32)	Stage 1 FIR Filter
0x0210_6000	Ch1 DDC Stage 2 Filter	Ch1 DDC Stage 2 Filter (Dec = 2 to 32)	Stage 2 FIR Filter
0x0210_8000	Ch1 DDC Stage 3 Filter	Ch1 DDC Stage 3 Filter (Dec = 2 to 32)	Stage 3 FIR Filter
0x0210_9000	–	Reserved	–

Base Address	Module	Description	Reference
0x0210_A000	Ch1 DDC Output Formatter	Ch1 DDC Output Formatter	IQ Data Formatter
0x0210_B000	Ch1 DDC Bypass Mux	Ch1 DDC Bypass Mux	DSP Bypass Mux
0x0210_C000	–	Reserved	–
0x0210_D000	–	Reserved	–
0x0210_E000	–	Reserved	–
0x0210_F000	–	Reserved	–
0x0211_0000	Ch1 DDC Power Meter	Ch1 DDC Power Meter	Power Meter
0x0211_1000	Ch1 DDC Threshold Detect	Ch1 DDC Threshold Detection	Threshold Detector
0x0211_2000	Ch1 DDC Threshold Gating	Ch1 DDC Threshold Gating	DSP Gate Substitution
0x0220_0000	Ch2 DSP Interrupts	Interrupt Registers for DSP Ch2	DSP Interrupts
0x0220_1000	Ch2 DDC Mixer	Ch2 DDC Mixer Control	Mixer
0x0220_2000	Ch2 DDC NCO	Ch2 DDC NCO Control	NCO
0x0220_3000	–	Reserved	–
0x0220_4000	Ch2 DDC Stage 1 Filter	Ch2 DDC Stage 1 Filter (Dec = 2 to 32)	Stage 1 FIR Filter
0x0220_6000	Ch2 DDC Stage 2 Filter	Ch2 DDC Stage 2 Filter (Dec = 2 to 32)	Stage 2 FIR Filter
0x0220_8000	Ch2 DDC Stage 3 Filter	Ch2 DDC Stage 3 Filter (Dec = 2 to 32)	Stage 3 FIR Filter
0x0220_9000	–	Reserved	–
0x0220_A000	Ch2 DDC Output Formatter	Ch2 DDC Output Formatter	IQ Data Formatter
0x0220_B000	Ch2 DDC Bypass Mux	Ch2 DDC Bypass Mux	DSP Bypass Mux
0x0220_C000	–	Reserved	–
0x0220_D000	–	Reserved	–
0x0220_E000	–	Reserved	–
0x0220_F000	–	Reserved	–
0x0221_0000	Ch2 DDC Power Meter	Ch2 DDC Power Meter	Power Meter
0x0221_1000	Ch2 DDC Threshold Detect	Ch2 DDC Threshold Detection	Threshold Detector
0x0221_2000	Ch2 DDC Threshold Gating	Ch2 DDC Threshold Gating	DSP Gate Substitution
0x0230_0000	Ch3 DSP Interrupts	Interrupt Registers for DSP Ch3	DSP Interrupts

Base Address	Module	Description	Reference
0x0230_1000	Ch3 DDC Mixer	Ch3 DDC Mixer Control	Mixer
0x0230_2000	Ch3 DDC NCO	Ch3 DDC NCO Control	NCO
0x0230_3000	–	Reserved	–
0x0230_4000	Ch3 DDC Stage 1 Filter	Ch3 DDC Stage 1 Filter (Dec = 2 to 32)	Stage 1 FIR Filter
0x0230_6000	Ch3 DDC Stage 2 Filter	Ch3 DDC Stage 2 Filter (Dec = 2 to 32)	Stage 2 FIR Filter
0x0230_8000	Ch3 DDC Stage 3 Filter	Ch3 DDC Stage 3 Filter (Dec = 2 to 32)	Stage 3 FIR Filter
0x0230_9000	–	Reserved	–
0x0230_A000	Ch3 DDC Output Formatter	Ch3 DDC Output Formatter	IQ Data Formatter
0x0230_B000	Ch3 DDC Bypass Mux	Ch3 DDC Bypass Mux	DSP Bypass Mux
0x0230_C000	–	Reserved	–
0x0230_D000	–	Reserved	–
0x0230_E000	–	Reserved	–
0x0230_F000	–	Reserved	–
0x0231_0000	Ch3 DDC Power Meter	Ch3 DDC Power Meter	Power Meter
0x0231_1000	Ch3 DDC Threshold Detect	Ch3 DDC Threshold Detection	Threshold Detector
0x0231_2000	Ch3 DDC Threshold Gating	Ch3 DDC Threshold Gating	DSP Gate Substitution

User Block Address Space

The FPGA reserves a block of addresses for user registers/storage for custom processing of data by the User Blocks. In the default FPGA configuration these addresses perform no functions, but are available as read/write temporary storage. You can read and write any type of data to each address.

Base Address	Module	Description	Reference
0x0300_0000	User Block 1	User Register Space	User Blocks
0x0380_0000	User Block 2	User Register Space	

PCI Configuration Space Registers

The PCI Configuration Space consists of fields that uniquely identify the device and allow the device to be generically controlled. The first 16 Bytes (four words) are defined the same for all types of PCI devices. The remaining words can have different layouts depending on the base function that the device supports. The PCI interface on the Model 71861 uses Header Type 00h, which has the layout shown in the table below. This table lists the PCI Configuration Space registers, their functions, and their base address in Configuration Space.

PCI Configuration Space Header (Type 00h)				
Address	**Register Function**			
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	BIST	Header Type	Latency Timer	Cache Line Size
0x10	Base Address Register 0 (BAR0)			
0x14	Base Address Register 1 (BAR1)			
0x18	Base Address Register 2 (BAR2)			
0x1C	Base Address Register 3 (BAR3)			
0x20	Base Address Register 4 (BAR4)			
0x24	Base Address Register 5 (BAR5)			
0x28	Cardbus CIS Pointer			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	Expansion ROM Base Address			
0x34	Reserved			
0x38	Reserved			
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

In the Model 71861, only the first Base Address Register of PCI Configuration Space, BAR0, is used to configure the memory maps of board resources and registers.