Subject: DDS Parallel Controller Software Requirements
File : DDSCTRL.WRI
Date : February 6, 1998
Revision 5

I. IOSelA Write

Table 1 : Data Word Description

Bits	Description
15	Set to 1 to identify Data Word
14,13	Device Selection 0 : 32-bit IPP Counter, IPP=(N+1)*40ns 1 : DDS1 (PlanetaryDownConverter LO/Xmitter Freq.) 48-bit STEL-1273 DDS, f=50MHz*N/(2e48) 2 : DDS2(SincFilter Clock/Xmit PN Code Generator) 48-bit STEL-1273 DDS, f=50MHz*N/(2e48) 3 : Transfer Relay Control
12	Set to 1 on last DDS data word.(+)
11	Unassigned
10..8	Address : IPP registers : Address 0-3 DDS delta-phase register : Address 0-5 Transfer Relay Control : (don't care)
7..0	Data Byte for IPP Counter, DDS1, and DDS2 Data Bit for Transfer Relay Control 0 : DDS's to Receiver, Fixed 20MHz to Transmitter 1 : DDS's to Transmitter, Fixed 20MHz to Receiver

(+) Use Bit 12 in conjuction with the Data Ready Flag and Data Error Flag.
Bit 12 sets Data Ready HI. The frequency update sets Data Ready LO.
If the frequency update occurs before Data Ready is set HI, Data Error is set HI.
The Data Error Flag is cleared by the Command Word. The Command Word also clears the Data Ready Flag.

Table 2 : Command Word Bit Assignments

Bits	Description
15	Set to 0 to identify Command Word
14,13,12	0 : Exit IPP Mode and Clear Flags 1 : Clear DDS's 2 : Update Immediate 3 : Update on tick 4 : Update on tick and then on every IPP 5.. 7 : Unassigned
11-0	Unassigned

II. IOSelA Read

Table 3 : Read Status

Bits	Description
15	Data Error Flag (+)
14	Data Ready Flag (+)
13	Updates on IPP enabled.
12	50 MHz Clock not present
11	1s Tick not present
10	Chassis Power / Cable not present

III. IPACK Interrupts

IntReq0 : Frequency Update Vector = 0xFF

IntReq1 : 1s Tick Vector = 0xFE

DDS levels without filter

Freq.	Level	Freq.(Image)	Level(Image)
19MHz	-3.7dBm	31MHz	-8.4dBm
20	-4.1	30	-7.7
21	-4.4	29	-7.4