RDBE Setup and Operations

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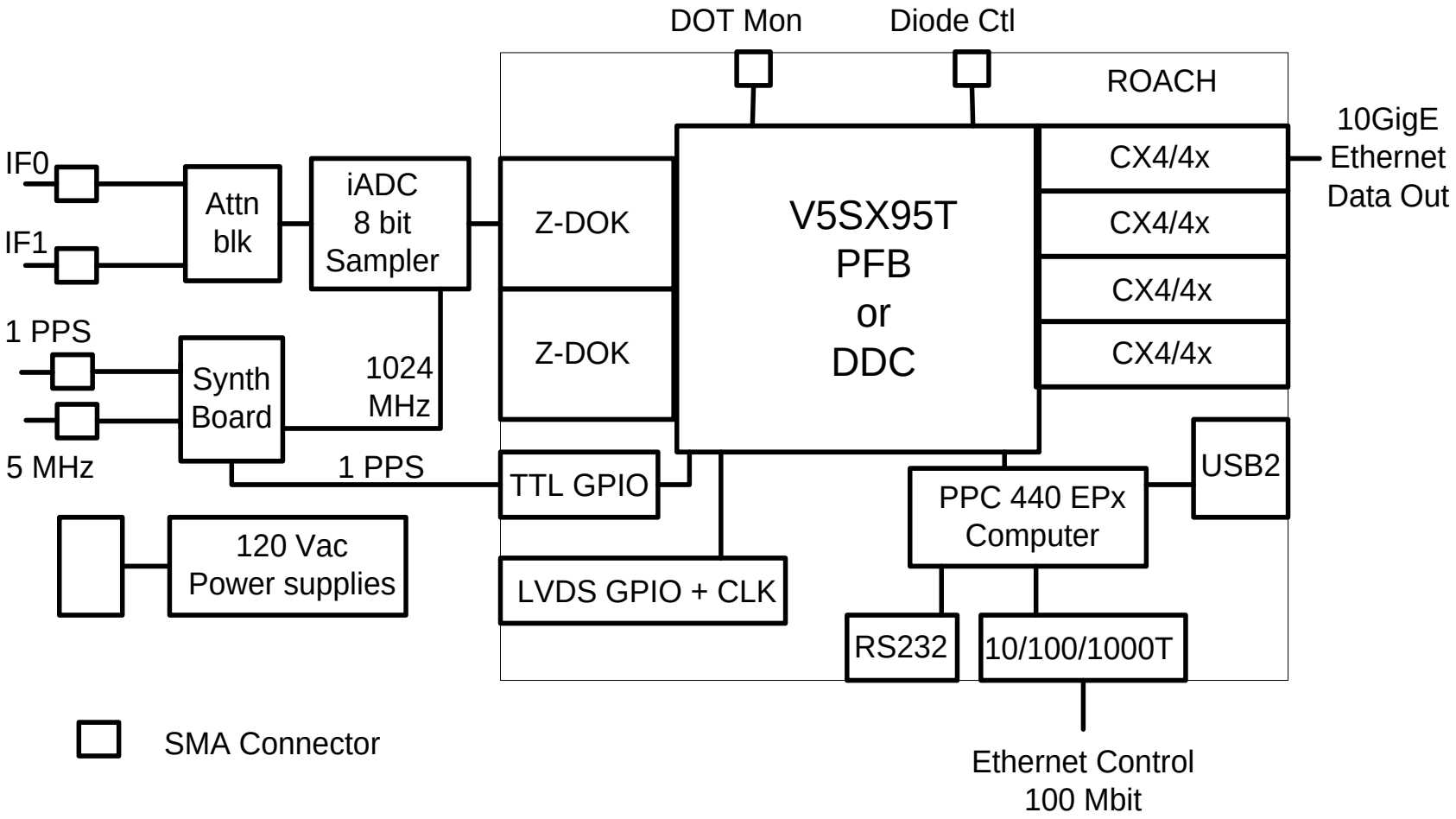
Agenda

- System overview
  - Hardware components
  - Firmware components
  - Software components
- Features
- Command set
- Basic operation
- Next Generation
- Demonstration

System Overview

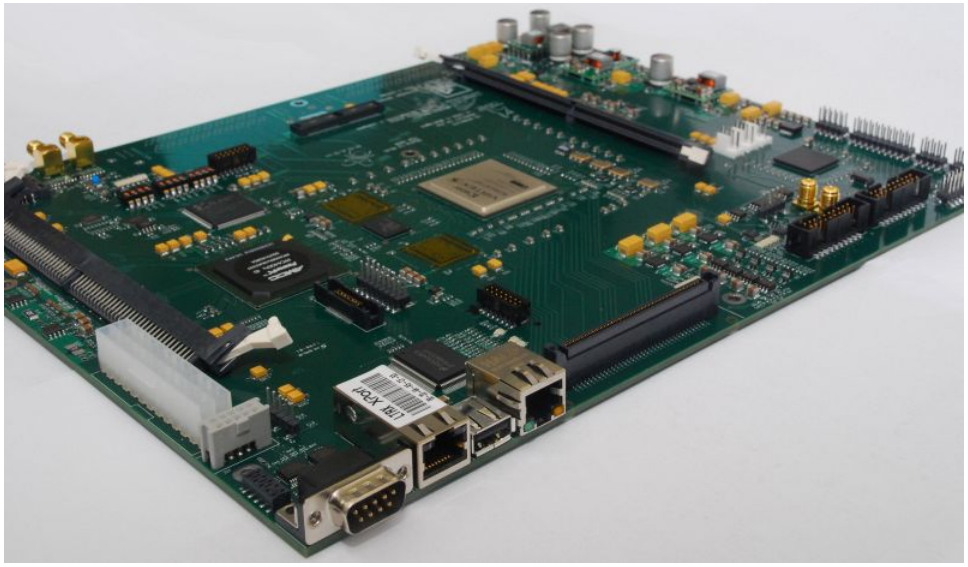
- RDBE – ROACH Digital Backend System
  - Originally a joint collaboration between NRAO and Haystack
  - Name is assigned to a specific base system
    - Specific hardware components
    - Can be ordered from Digicom
  - Variations are expected
    - Represented by hyphenating the name **RDBE-X**
      - **X** represents the hardware components of the RDBE
    - Presently there are RDBE-H, RDBE-S, RDBE-G
    - This overview covers the new RDBE-G

RDBE-X Block Diagram



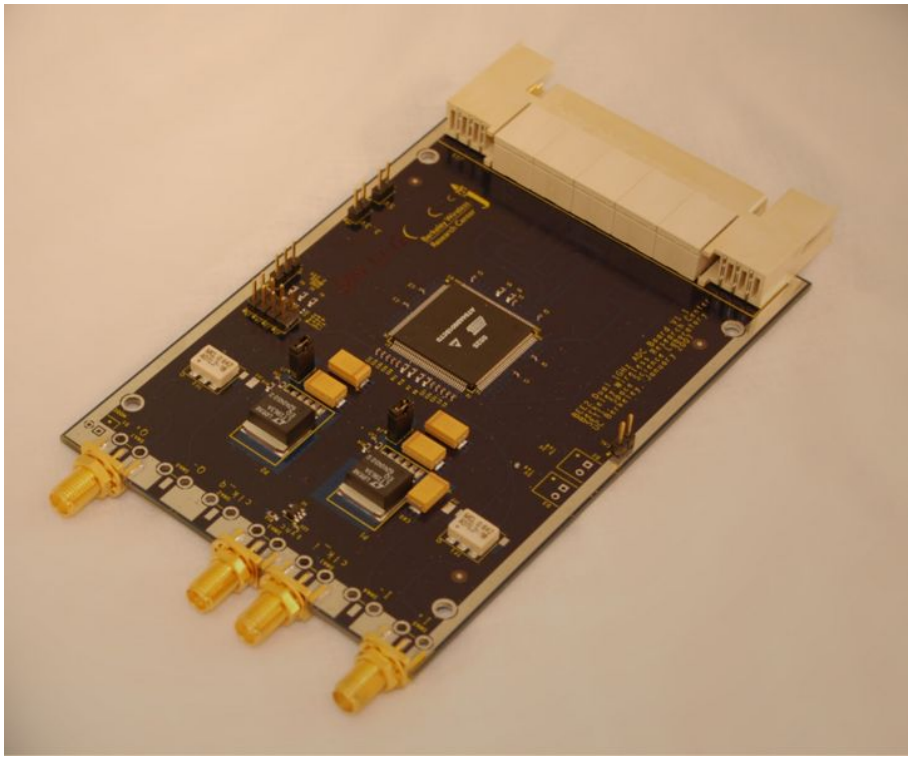
RDBE Hardware Components

- ROACH Board
  - **R**econfigurable **O**pen **A**rchitecture **C**omputing **H**ardware
  - Developed by the CASPER group at Berkeley / NRAO / KAT
- Virtex 5 FPGA
- 440 PPC processor
- 2G RAM
- 2 ZDOK connectors
  - iADC
- RS232 interface
- 1G / 100M Ethernet
- 4 CX4 10G Ethernet ports
- 1 XPORT interface



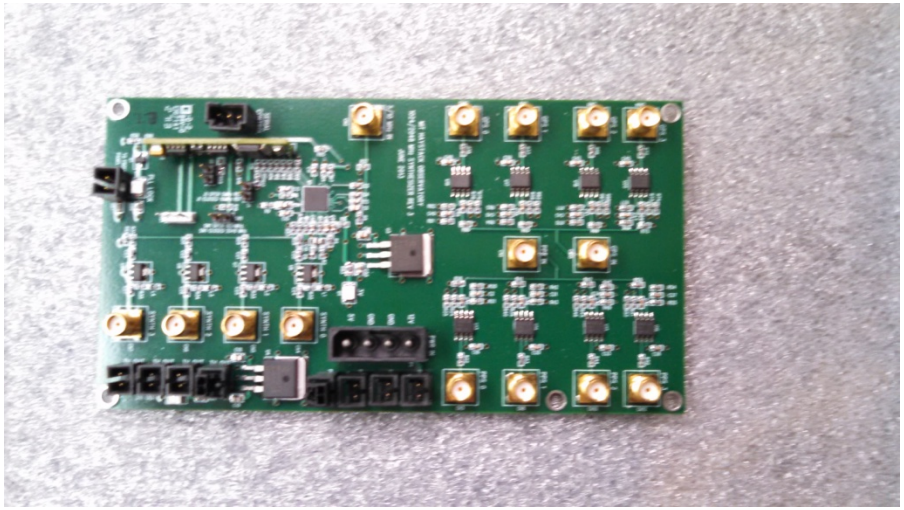
RDBE Hardware Components

- iADC
  - Analog to Digital Converter (sampler board)
    - Developed by the CASPER group
  - 2GHz bandwidth
  - 1 Giga sample / sec
  - 8 bits / sample
- 2 iADC cards supported per ROACH



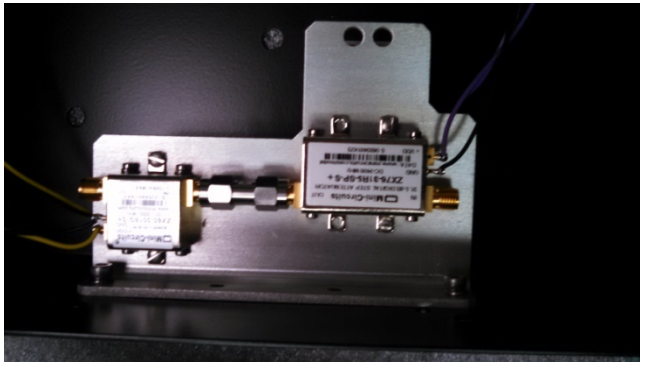
RDBE Hardware Components

- Synthesizer / timing board
  - Developed AEER
  - Inputs
    - 5MHz
    - 1pps
  - Outputs
    - 1pps
      - four SMA's
    - 1024 MHz
      - four SMA's



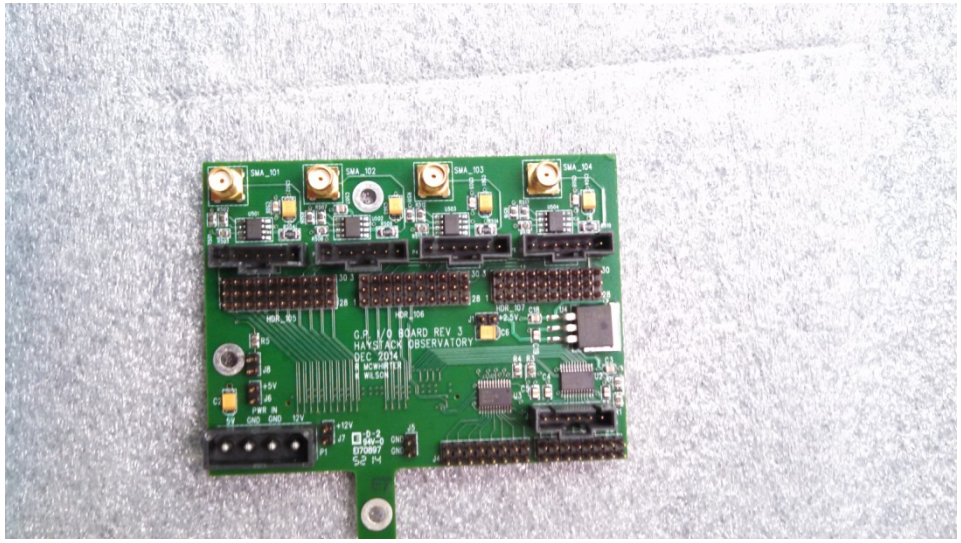
RDBE Hardware Components

- Attenuators
  - Analog level control
  - Off the shelf
    - Mini-circuits
  - 1 IFs in / 1IFs out
    - Two boards per system
  - 0-31.5 dB attenuator
    - 0.5dB steps
  - No 20dB solar attenuation



RDBE Hardware Components

- GPIO Board
  - Mated to high speed differential connector on ROACH Board
  - LCD front panel control
  - Diode control
  - Attenuator control



RDBE Hardware Components

- Miscellaneous
  - Power supply
    - 90 ~ 132 VAC or 180 ~ 264 VAC auto sensing
  - 1pps LED
    - Indicates 1pps internal to FPGA code (DOT Clock)
  - 5MHz lock LED
  - Power LED
  - 4 SMA connectors front
    - Output
  - 8 SMA connectors back
    - Inputs + Diode ctrl out

RDBE-G Front Panel

RDBE-G Back Panel

RDBE Firmware

- 4 Personality types (FPGA code)
  - Polyphase filter bank-geodesy (PFBG) Ver. 3.0
    - Input is two 512MHz IFs
    - Standard output is sixteen of 32 possible 32-MHz channels (2Gbps)
      - Mode of all thirty-two 32 MHz channels available (4Gbps)
    - Output is a 8224 byte VDIF data format (next slide)
      - Complex Data
      - Standard 32 byte header
    - eVLBI VTP protocol available

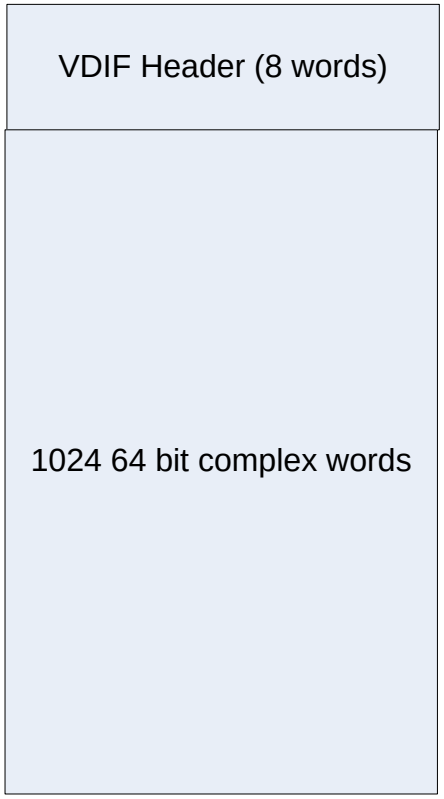
RDBE Firmware

- Original Polyphase filter bank-geodesy (PFBG) Ver. 1.4
  - Input is two 512MHz IFs
  - Output is sixteen of 32 possible 32-MHz channels
  - Output is a 5008 byte Mark5B data format
- Polyphase filter bank-astronomy (PFBA) Ver. 1.5
  - Input is four 512 MHz IFs
  - Output uses two of the four 10Gbps CX4 interfaces
    - 2-bit quantized
    - 4Gbps / interface
    - 8224 byte packets using the VDIF format.

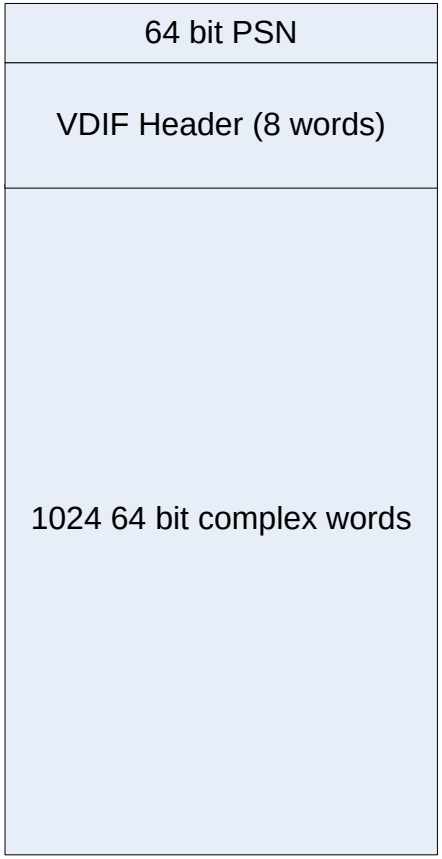
RDBE Firmware

- Digital down converter (DDC)
  - Input is two 512MHz IFs
  - Output is four tunable channels
  - Bandwidths 128 / 64 / ◦◦◦ / 1 MHz (same for all 4 channels)
    - Data rate proportional to bandwidth
  - Tunable in 15.625 kHz quanta (testing incomplete)
  - Output is in 5008 byte Mark5B format 2 bits / sample
  - 250-kHz common quantum with 10-kHz on legacy systems

VDIF Payload Options

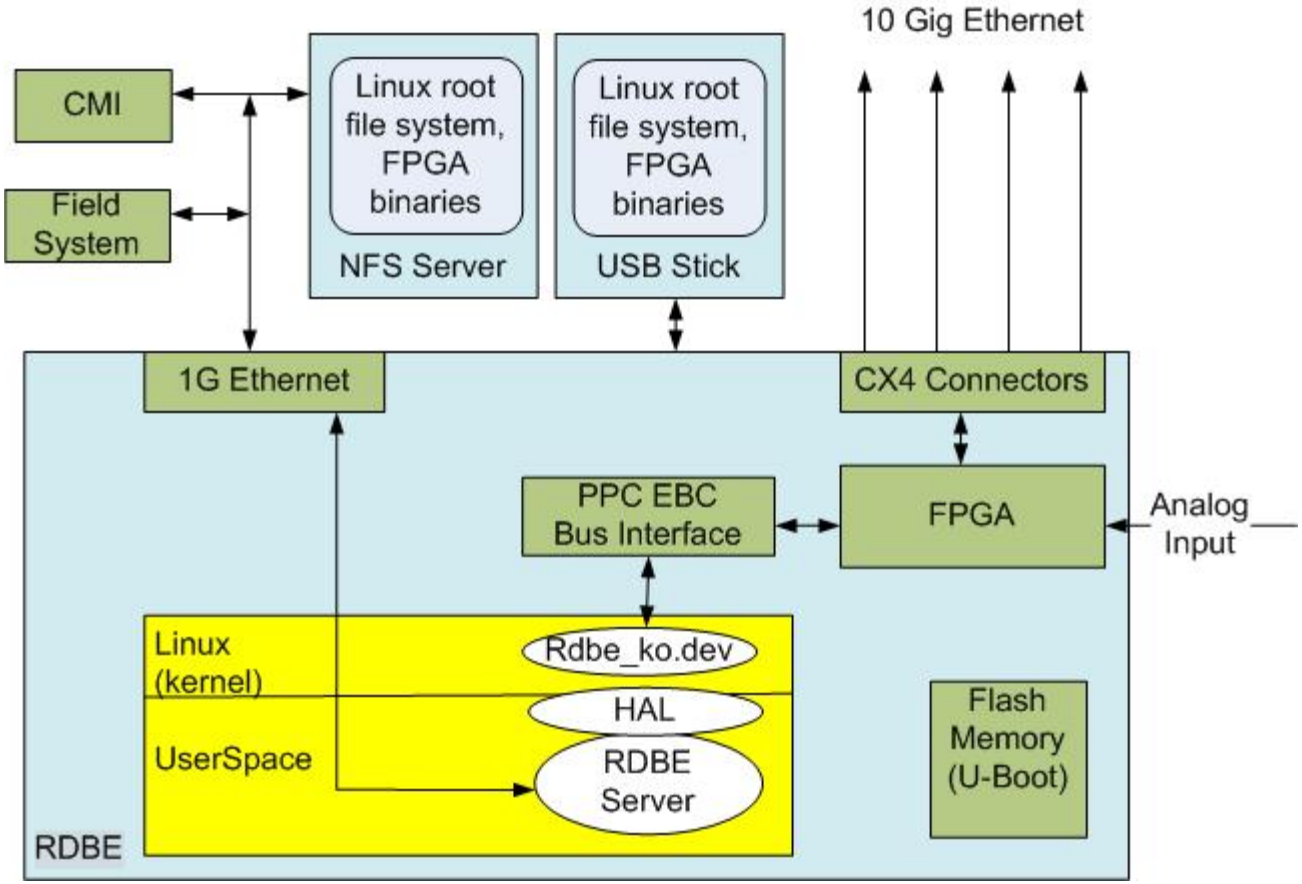


Standard VDIF Payload



VTP Compliant Payload

RDBE Software



RDBE Software

- rdbe_dev.ko
  - Linux kernel device driver
  - Allows the application to read / write to the FPGA personality
- rdbe_server
  - Version 3.0 will be required for operation with FS
  - Accepts VSI-S commands
  - Verifies and takes actions on valid commands
  - Specified in the RDBE command set version 3.0
  - Not backward compatible with 1.4/1.5/DDC

Ver. 3.0 RDBE Command Set

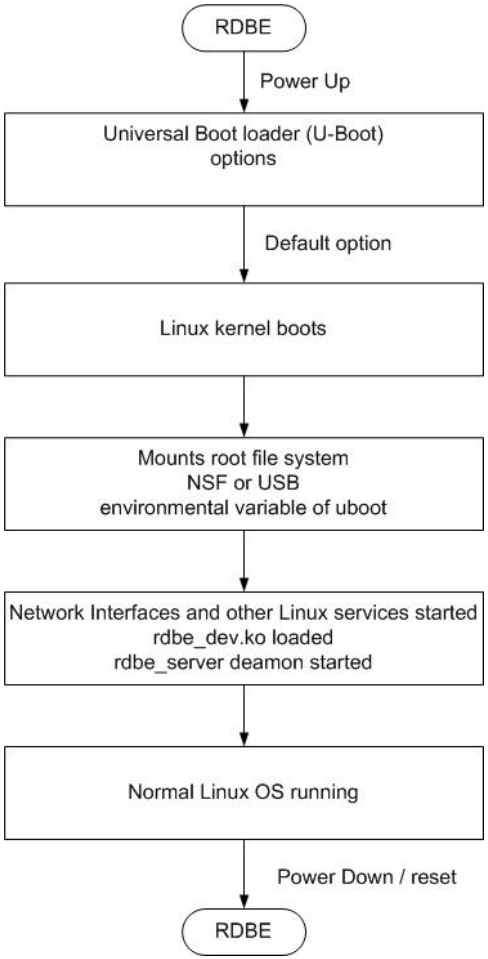
- Standard VSI-S command format

dbe_1pps_mon	Set the 1pps monitoring broadcast state
dbe_atten	Set / get the attenuator setting for INPUT 0/1
dbe_bstate?	Quantizer state counts in percent for all channels
dbe_chsel	Set / get the input to output channel assignments
dbe_chsel_en	Set / get the data rate (2/4Gbps), chsel enabled/disabled, psn enabled / disabled
dbe_arp	Set / get the IP to MAC address resolution
dbe_data_connect	Set / get the destination IP the data is being sent
dbe_data_send	Transmit a data stream out of the DBE 10G interface
dbe_diode	Set ./ get diode control frequency and blank time in micro-seconds
dbe_dot	Set / get the Data Observable Time (DOT) clock information
dbe_dot_inc	Increment the DOT clock, default is 1 second
dbe_gps_offset?	Get the GPS offset in mico-seconds to 1pps DOT clock
dbe_hw_version?	Get the hardware version information from the DBE
dbe_ifconfig	Set / get DBE 10G network interface configuration
dbe_init	Resets FPGA sampler, clocks and enables PPS interrupt
dbe_mac	Set / get the 10 CX4 port MAC address
dbe_ntpdate	Set / get the NTP server's IP address to synchronize to
dbe_option	Set / get formatting options (spaces, long time format - fractional seconds)
dbe_pcal	Set / get phase cal frequency in hertz (default is 0 Hz)
dbe_personality	Set / get the RDBE FPGA bit code personality
dbe_pps_mon	Set / get the once per second multicast data IP address and port.
dbe_pps_offset?	Get the pps offset to the incoming MASER pps signal
dbe_quantize	Set / get present channel quantization data
dbe_raw?	Get 100 raw samples for an interface from the DBE
dbe_reboot	Set the number of seconds before the DBE reboots
dbe_status?	Get system status (query only)
dbe_sw_version?	Get the software version information from the DBE
dbe_tsys?	Get 16 Tsys on values followed by 16 off values normalized to 1000000

Basic Operations

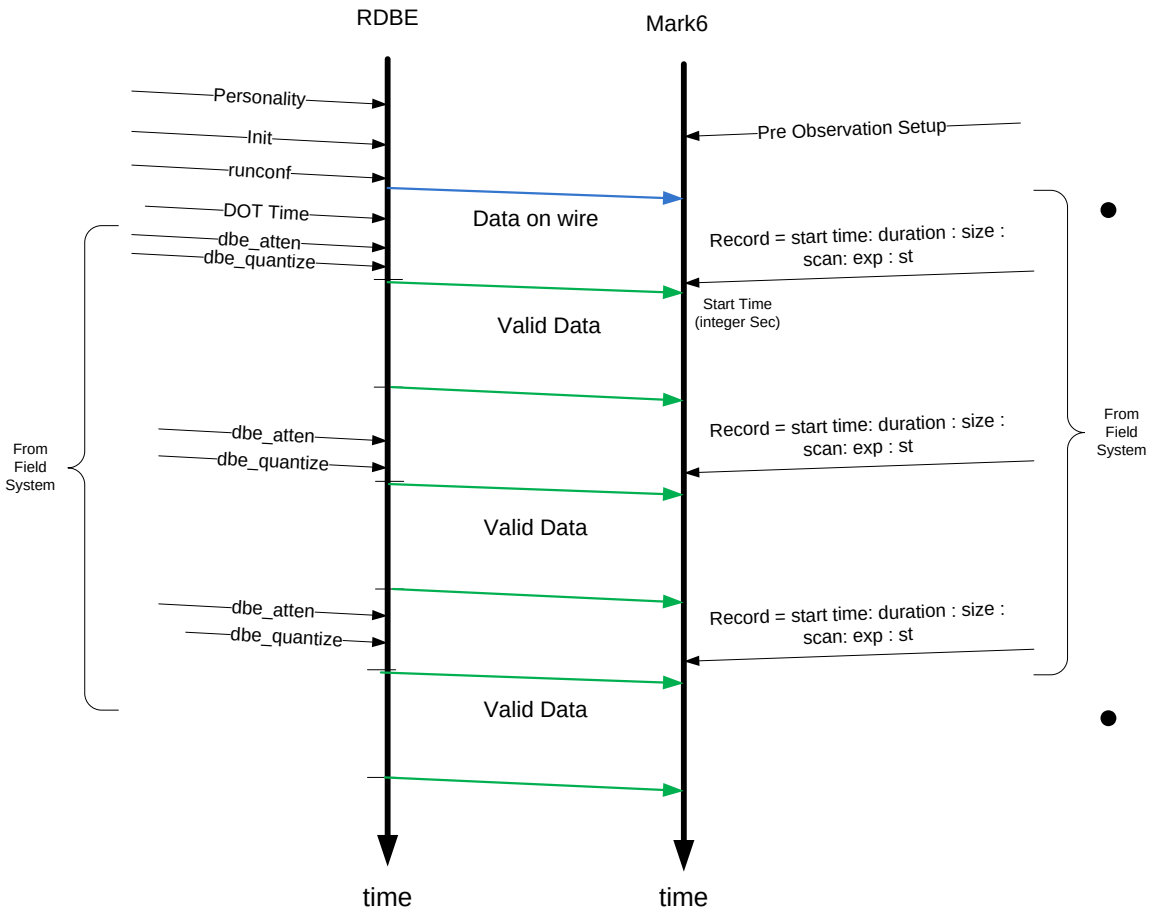
- Topics addressed on the following slides
  - Boot Up
  - rdbe_server daemon communication
    - dbe_data_send operational modes
    - monitoring capabilities
      - 1pps
      - tsys
      - pcal
      - raw capture mode
      - PPS / GPS offsets
  - Software utilities

Boot Up



- U-Boot options
  - Environment variables defining what the boot loader will execute
    - location of the kernel in flash (address)
    - location of the root file system
      - USB
      - NFS
      - SDRAM
      - bootp
    - Network configuration
      - Static
      - Dynamic
  - Details are beyond the scope of this talk
    - Detail documentation available if needed

rdbe_server



- Loading the FPGA personality
  - Located where the root file system is mounted
  - /home/roach/personalities
- Initialization
  - Setting the FPGA registers
  - Setting the DOT time
    - system time
    - manually
  - Quantization
    - Formats the filter bank channels at 2 bits / sample
  - Monitoring capabilities
- Set for normal operations
  - Transmitting data out CX4 interface
  - Status / etc.

IO Channel Selection

- Capability to set the input output channel assignment for the VLBI Payload
  - Feature for PFBG personality only
    - Input is two 512MHz IFs
    - Output is 8 out of 16 per IF possible 32-MHz channels
    - Version 1.4/1.5 has any possible combination
      - Version 3.0 does not
  - The command
    - dbe_chsel = <input>:<channel(s)>;
    - input
      - 0 or 1 for IF0 or IF1
    - channel(s)
      - individual channels

Configuration

- Initialization of static information
  - e.g. 10G IP, MAC, ARP entry, etc.
  - Handled with command
    - run_conffile=/path/filename
    - /home/roach/personalities/conf/filename
      - See next page for example / explanation
- The channel ordering
  - The present geodetic personality
    - The default dbe_chsel? {0,1} returns
      - dbe_chsel ? 0: 0 : 1 : 3 : 5 : 7 : 9 : 11 : 13: 15 ;
      - dbe_chsel ? 0: 1 : 1 : 3 : 5 : 7 : 9 : 11 : 13: 15 ;

Static Configuration File

Command Executed	Comments
ifconfig= up : 9000 : 4 : 192.168.1.102 : 1	10G Network setup = State : payload size : TCP : Source IP : Network Interface Source IP Address
mac=00.00.11.22.33.42	MAC Address of the 10G, made up unique for each RDBE
chsel_en=2 : chsel_enable : psn_enable	# 2 Gbps data rate, with Channel select and PSN enabled
arp= 192.168.1.3 : 00.60.dd.44.9f.81	ARP entry for destination Mark6 IP address and MAC Address
data_connect=192.168.1.3 : 9002 : 0xBdC : 1	# Set the configuration for IP / UDP / VDIF header. destination IP address : UDP port : Station / RDBE Identifier : Thread ID
pps_mon=disable	Disable previous initialized multicast transmission
pps_mon=enable : 239.0.5.50 : 20055	Multicast enabled : Unique Multicast IP, unique Port. Set these to RDBE IP address
pcal=1.4e6	Set pcal for UDC factional portion
data_send=on	Start transmitting data over 10G interface
option=time_long	Use fractional time long format when replying to requests

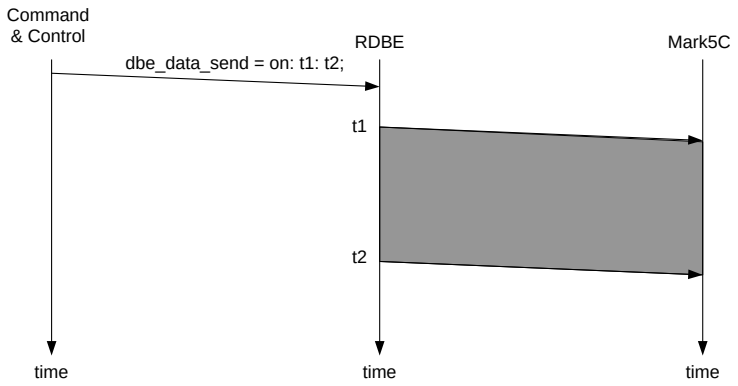
Data Transmission

- In the past data were always available and the gating function was performed on the recording device
  - Record = on / off commands
  - Supported with dbe_data_send=on
- One can also gate at the source and destination for transmission over WANs:
  - To gate at the RDBE
    - Since the start and end time are known a priori
      - use the dbe_data_send to gate the output on the 10G

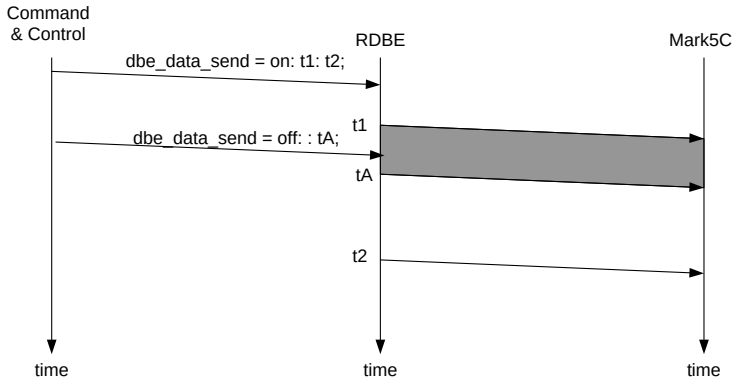
Design Philosophy

- start time <= present DOT time < end time
  - Personality will transmit valid packets
  - Times are specified as integer seconds
- Start and end times are programmed into the FPGA using the command:
  - dbe_data_send
  - command format
    - dbe_data_send = < state > : [< ts >] : [<te>] : [<delta>];
      - state - either “on” or “off”
      - start and end times (ts, te) are of the format YYYYDDDHHMMSS
      - delta - specified in integer seconds.

dbe_data_send options



- Specify start / end time
  - YYYYDDDHHMMSS
- Or specify start and delta time
  - t2 is generated as t1 + delta
  - delta is integer seconds



- Ability to abort an active transmission
  - send the off state with
    - a specified time
    - no time - meaning next integer second

Monitoring Capabilities

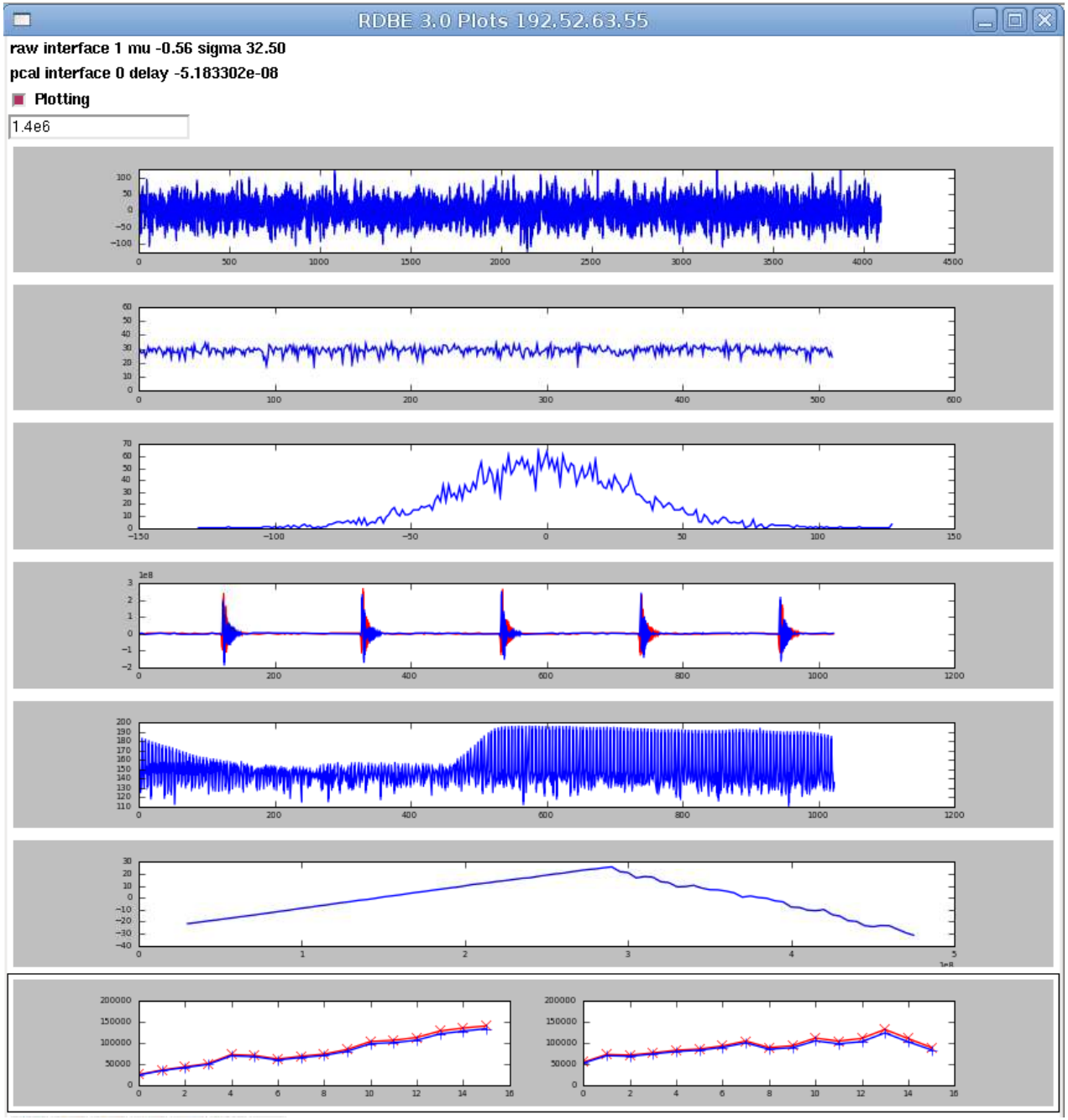
- 1pps monitoring
  - dbe_1pps_mon = <enable> : <multicast IP address> : <port>;
  - Use rdbe_mon.py on a system attached to same network to receive multicast data
  - Tsys monitoring
    - System temperature measurement
    - On power / off power of the receive chain
    - tsys data is summed every second
  - Raw Capture Mode
    - Provides ability to see the incoming signal from the iADC before it is processed by the FPGA personality
    - 32000 samples are captured

Input signal

Histogram

FFT of pulse cal

Power of IFX channels (on / off)



FFT of input signal

Pulse cal extraction

phase of pulse cal tones

Software Utilities

- *rbde_client -h <machine>*
  - Command line interface to RDBE
  - *-h <machine>* is the target RDBE systems IP address (defaults to localhost).
  - *rdbe_server* must be running on *<machine>*
- *rdbe30_mon.py -h <multicast addr> -p <port> -H <RDBE addr> -P <rdbe_server port>*
  - *Graphical command and monitoring application*
  - *Sends commands / displays multicast output graphically*
  - *Very CPU intensive, to be used only for snap shot of RDBE*

RDBE Next Generation Development

- Plans:
  - ROACH 2 board
    - Vertex 6
    - 4 SFP+ Connectors
      - Fiber or Copper
    - Leveraging FPGA code from Event Horizon Telescope
      - Code must be ported, extended for Geodetic filter bank features
    - Existing server code must be ported to new platform
  - 1 ADC
    - 2G Samples
  - New GPIO interface board
- Expected at a store near you by Christmas 2016
  - Provided the project is funded

DEMONSTRATION

TIME PERMITTING